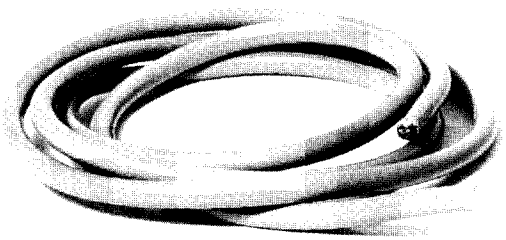
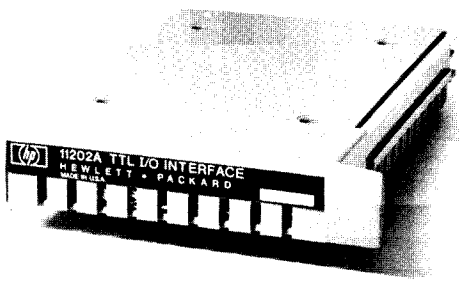
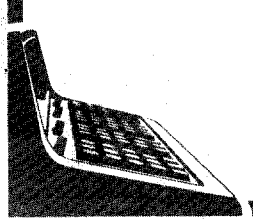
INSTALLATION and SERVICE MANUAL

11202A I/O INTERFACE







HEWLETT–PACKARD CALCULATOR PRODUCTS DIVISION
P.O. Box 301, Loveland, Colorado 80537, Tel. (303) 667-5000
(For World-wide Sales and Service Offices see rear of manual.)

Copyright by Hewlett–Packard Company 1974

TABLE OF CONTENTS

CHAPTER 1: GENERAL INFORMATION

INTRODUCTION 1-1
The Peripheral Control Block 1-1
Hardware Description 1-1
Technical Specifications 1-1
AVAILABLE OPTIONS 1-3
INSTALLATION CONSIDERATIONS 1-3
Select Code 1-3
Input Data Stability 1-5
Recommended Receiving Circuits 1-5
Recommended Transmitting Circuits 1-6

CHAPTER 2: APPLICATIONS

DATA OUTPUT 2-1
DATA INPUT 2-2
HANDSHAKE MODE 2-2
EXTERNAL RELAY CONTROL 2-3

CHAPTER 3: SERVICE

Calculator I/O Lines 3-1
THEORY OF OPERATION 3-2
Data Output Sequence 3-3
Data Input Sequence 3-4
Handshake Mode 3-5
Additional Theory 3-5
TROUBLESHOOTING AND REPAIR 3-6
Broken Trace Repair 3-6
Equipment Required 3-7
Equipment Setup 3-7
Preliminary Check 3-8
Troubleshooting Hints 3-9

REPLACEABLE PARTS 3-10
COMPONENT LOCATOR } foldout
CIRCUIT DIAGRAM }

APPENDIX: I/O Characters and Equivalent ASCII Forms

Chapter 1

GENERAL INFORMATION

INTRODUCTION

The HP 11202A I/O Interface is general-purpose card which provides 8-bit data exchange between a 9800-Series calculator and a peripheral device. The interface transfers data in a 'half-duplex' mode. That is, it can either input or output data, but not both at the same time. The interface provides storage of each input or output data character and also has a device control line and a device ready (flag) line. All data and control lines are compatible with standard TTL levels.

This manual describes how to install and service the 11202A Interface. Also, some typical interface applications are described in Chapter 2.

THE PERIPHERAL CONTROL BLOCK

In general, each calculator must have an appropriate peripheral control block when using this interface. The manual supplied with the block describes how to control and exchange data with peripheral equipment. Contact your nearest HP Sales and Service Office for information on the correct peripheral control block for your calculator system; office locations are listed at the back of this manual.

The 9830A Calculator does not need a peripheral control block if the peripheral is used as a printer only. See Appendix F in the 9830A Operating and Programming Manual for instructions on operating a 'primary printer'.

HARDWARE DESCRIPTION

The interface consists of a circuit board inside a case which plugs into any calculator I/O connector, and a 1.82 metre (6 foot) shielded cable. One end of the cable is connected to the circuit board and the other end is unterminated (see 'Available Options').

TECHNICAL SPECIFICATIONS

I/O Format

The interface sends and receives information in 8-bit-parallel, character-serial fashion. All usable ASCII-coded* characters are listed in the Appendix.

Although the calculator handles only ASCII-coded information, the interface can transfer data in any 8-bit binary code.

Data Input Lines

Eight input lines, each with a low-power 74L04 TTL load and a resistive divider consisting of 1.8KΩ to +5V and 2.7KΩ to ground are available.

*American Standard Code for Information Interchange.

INTRODUCTION
(continued)

Data Output Lines

Eight output lines with open-collector 7406 TTL inverters are available.

Control Lines

- Device Control ($\overline{CTL}$) – High-to-low transition indicates that the interface is ready to input data or has data to output.
- Device Ready ($\overline{FLG}$) – Peripheral device indicates 'data accepted' or 'data valid' by forcing line low. The $\overline{FLG}$ signal must be greater than 500ns.
- I/O Status (I/O) – Tells device whether calculator has started an input operation (high) or an output operation (low).
- Stop ($\overline{STP}$) – $\overline{STP}$ is low whenever the calculator STOP key is held down.
- Enable Handshake (ECH) – When ECH is connected to ground, the interface cannot drive $\overline{CTL}$ low until the peripheral device forces $\overline{FLG}$ high to indicate 'ready'. When ECH is left open, the interface does not check the $\overline{FLG}$ line before driving $\overline{CTL}$ low.

Signal Levels

All data and control lines use 'negative-true logic' (i.e., $<.7V$ indicates 'low' or logic '1' or 'true', and $>2.4V$ indicates 'high' or logic '0' or 'false'). A bar above each line name (e.g., $\overline{CTL}$ and $\overline{FLG}$) indicates that the line goes low when pulsed '1'. All other lines go high when pulsed '1'.

Temperature Range

5°C to 45°C Ambient.

Power

Provided by the calculator.

Dimensions

Case: 12.06cm (4¾ inches) x 15.87cm (6¼ inches).

Cable: 1.82m (6 feet).

AVAILABLE OPTIONS

Each of the optional interfaces listed below consists of a standard 11202A which is wired for use with a specific HP instrument. A wiring diagram of the added connector and operating instructions are furnished with each optional interface.

11202A–	Interfaces with a:
Option A01	2748A/B Tape Reader
Option A02	2895A/B Tape Punch
Option A04	3482A or 3484A Plug-in Unit*
Option A05	3485A Scanner Unit*

*These units are part of a 3480A/B Digital Voltmeter. An 11203A BCD Interface is also needed to transfer data samples from the DVM to the calculator.

INSTALLATION CONSIDERATIONS

SELECT CODE

Since all peripheral devices are connected to the calculator in a party-line fashion, each device must have a unique address so that the calculator can specify which device must respond to each operation. This address, or 'select code', consists of a one or two-digit number and is preset on the interface.

Although the 11202A Interface is set to respond to select code 2 when supplied[1], you can set any one of eight other select codes by following this procedure:

1. Switch the calculator and the peripheral device off.

2. Disconnect the interface from the calculator. Remove the four screws located on the top of the card assembly. Then turn the card over and lift-off the bottom cover.

[1]Some optional interfaces are preset to select code 1. See their accompanying operating notes.

INSTALLATION CONSIDERATIONS
(continued)

3. Raise the hinged cover on the select code switch (see Figure 1-1). Using a small, flat-blade screwdriver, *carefully rotate* the selector tab until it is positioned at the desired select code number. Numbers are printed on the side and on the cover of the switch (switch position '0' is not usable). Before closing the cover, be sure that the slot in the selector tab is at a right angle to the length of the switch.

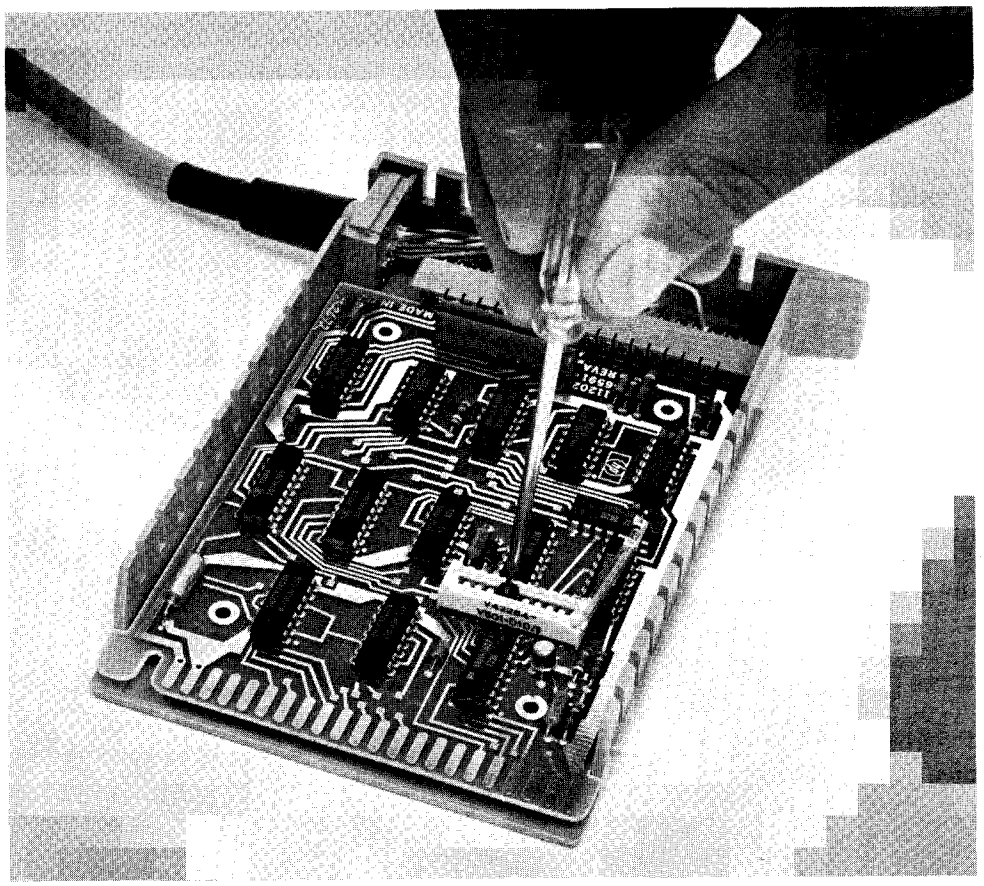


Figure 1-1. Setting the Select Code

4. Close the switch cover and replace the interface bottom cover. Secure the cover with the four screws previously removed.

5. Place a select code label on the peripheral device or on the interface case to indicate the new select code. A package of labels is supplied with the interface.

6. Reconnect the interface to the calculator, and turn the calculator and the device on. Verify that the desired select code is set by executing an I/O operation (or running a program) which specifies the new select code.

INPUT DATA STABILITY

Each data item placed on the interface input lines must be settled *before* the 'data ready' signal ($\overline{FLG}$ line) is transmitted. Then the data must be held stable for at least 500ns.

RECOMMENDED RECEIVING CIRCUITS

Each output signal from the interface is transmitted from an SN7406 TTL inverter, which has an open-collector output. The current-sinking capability of each inverter is 40mA and the breakdown voltage is 30V.

Here are typical specifications:

$$V_{ol} \begin{cases} @\ (I_{ol} = 16ma) = 0.4V\ max. \\ @\ (I_{ol} = 40ma) = 0.7V\ max. \end{cases}$$

V_{oh} (Open Collector) = 30V max.

I_{ol} = 40 mA max.

I_{oh} @ (V_{oh} max.) = 250 μA

Since each transmitter has an open collector, the peripheral receiving circuit must have a positive pull-up voltage (not to exceed 30V) and must be restricted to sourcing (back to the transmitter) less than 40mA. Recommended receiving circuits are shown in Figure 1-2.

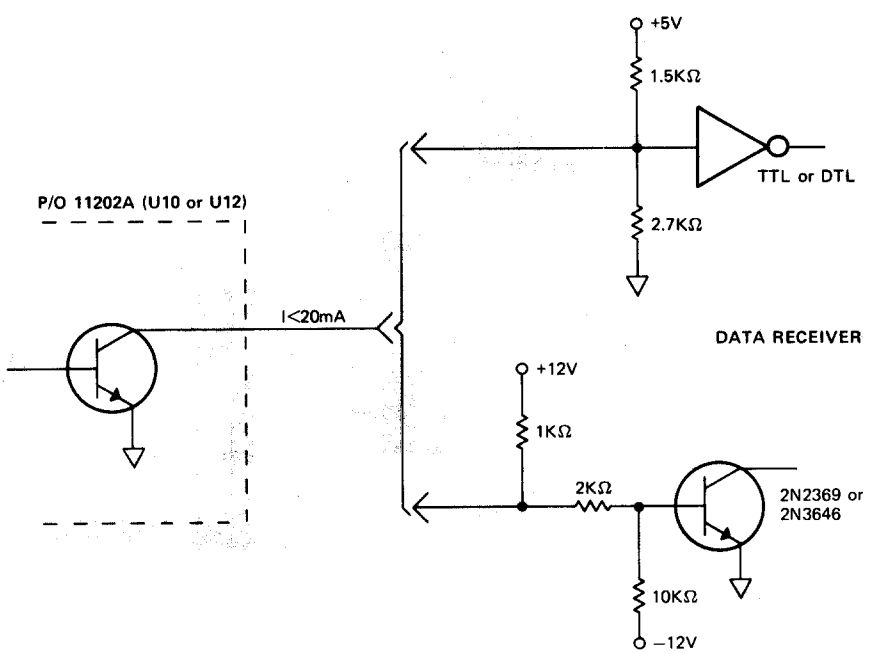


Figure 1-2. Recommended Peripheral Receiver Circuits

INSTALLATION CONSIDERATIONS

(continued)

RECOMMEDED TRANSMITTING CIRCUITS

Each data-input line on the interface (except $\overline{FLG}$) contains an SN74L04 low-power inverter. A resistive divider connected to each input line holds the voltage at about 3V when the cable is disconnected. The input voltage must not exceed 5.5V.

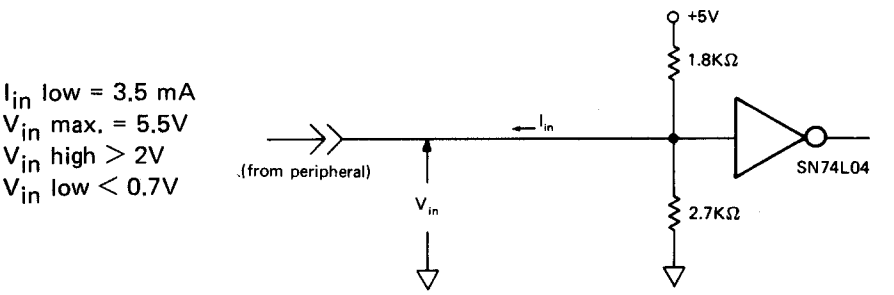


Figure 1-3. Interface Data Receiver Circuit

Recommended peripheral transmitting circuits are shown below.

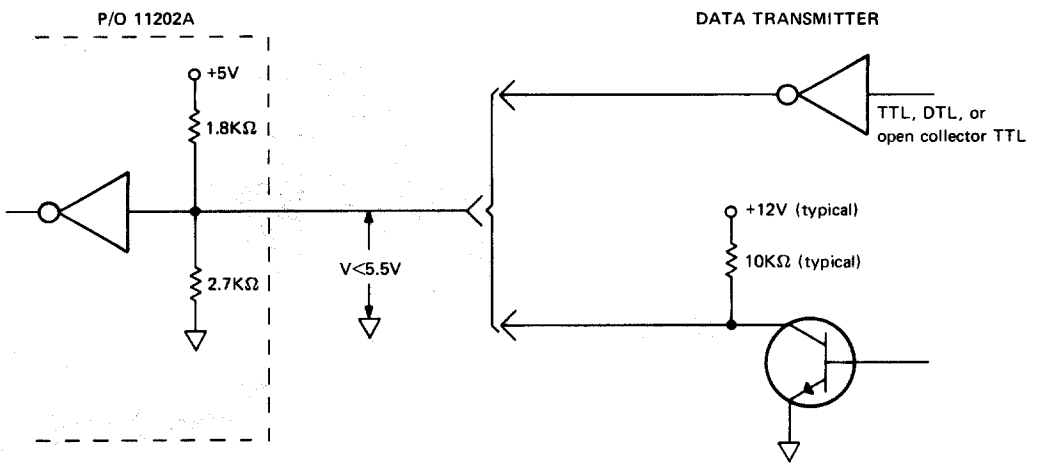


Figure 1-4. Recommended Transmitting Circuits

The device ready signal ($\overline{FLG}$) is received by an SN 7413 Schmitt trigger circuit. This circuit accepts signals with slow rise and fall times, and provides good noise margins. Although the voltage on the flag line must not exceed 5.5V, there is no restriction on the input rise and fall time. Either of the transmitting circuits shown in Figure 1-4 may also be used as a flag transmitter.

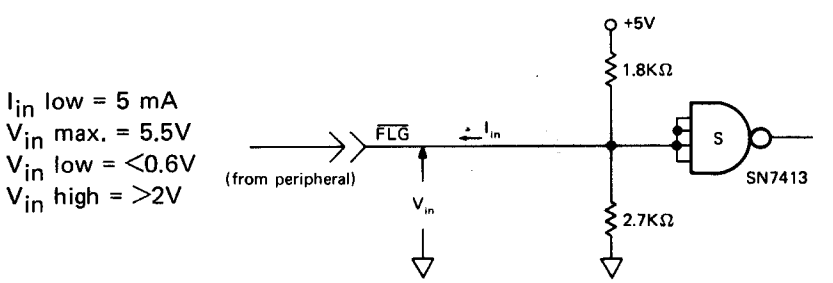


Figure 1-5. Interface Flag Receiver Circuit

Chapter 2

APPLICATIONS

This chapter describes some typical applications of the 11202A I/O Interface. Although your application may be quite different from those shown here, the interfacing requirements and I/O routine will be similar.

DATA OUTPUT

A popular application for the 11202A is as an interface to the HP Model 2895B/8100A Option 004 Tape Punch. Figure 2-1 shows a simplified functional diagram of the tape punch and the interface.

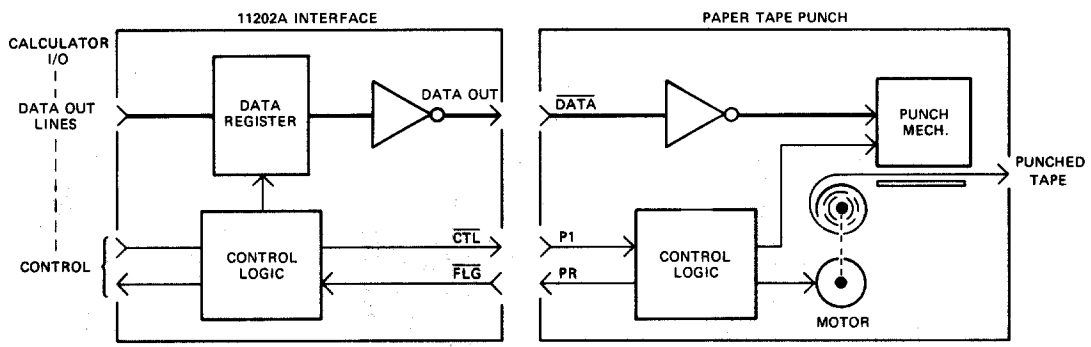


Figure 2-1. Diagram of a Tape Punch and Interface

After the tape punch is readied with a blank tape, this sequence occurs to output and punch data:

1) A DATA OUTPUT or WRITE operation is executed from the calculator. The specified format determines how many characters are output with each data item.
2) After the calculator outputs the first character to the interface, the interface latches the data onto its output lines and sends a P1 ($\overline{CTL}$) signal to the tape punch. The P1 signal causes the tape punch to decode and punch the data. Then the motor advances the paper and the tape punch outputs a PR($\overline{FLG}$) signal, indicating that it is ready for more data.
3) The $\overline{FLG}$ signal returns the interface to its ready state and outputs an SIØ signal to the calculator.
4) If the calculator has more characters to output, the sequence is repeated (see step 2).

DATA INPUT

Another popular application for the I/O Interface is as an interface to a high-speed paper tape reader, such as the HP Model 2748B Tape Reader. A simplified functional diagram of that system is shown in the next figure.

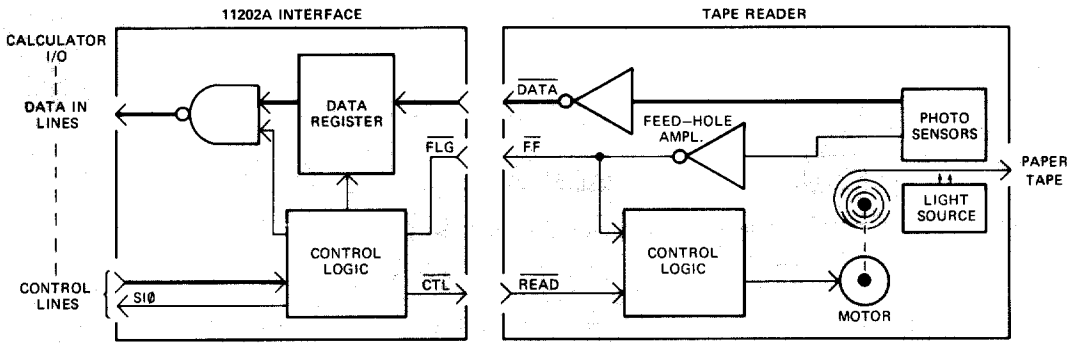


Figure 2-2. Diagram of a Tape Reader and Interface

After the tape reader has been readied with a tape, this sequence occurs to read the information:

1) A DATA INPUT or READ operation is executed from the calculator. The specified format and the sequence of data on the paper tape determine how many characters are read during each operation.
2) The interface outputs a READ($\overline{CTL}$) signal, which causes the tape reader motor to advance the tape. When a feed hole is detected on the tape, the motor stops and the data character is read. After the data is output on the DATA lines, a $\overline{FF}$($\overline{FLG}$) signal is output.
3) Upon receiving the $\overline{FLG}$ signal, the interface transfers the data character to the calculator.
4) After the calculator reads the data, it either stores the data and requests more (return to step 2) or it terminates the input operation.

HANDSHAKE MODE

As described in the previous sections, the interface normally interacts with the peripheral in a 'handshake' fashion - each device waits for the other to be ready before sending or receiving data. This section describes an alternate method of interface/peripheral control called the 'Handshake Mode'.

The Handshake mode is enabled by grounding the ECH line (see Figure 3-1). The term 'handshake' refers to the interface-peripheral interaction occuring on the $\overline{CTL}$ and $\overline{FLG}$ lines (see Figure 3-4).

When in the Handshake mode, the interface waits for a high $\overline{FLG}$ line before transferring each successive data character. (Normally, the interface resumes data transfer immediately after the $\overline{FLG}$ line goes low.)

The calculator can be programmed to detect the interface busy state by executing a Status Check or Read Status operation* *before* beginning an I/O operation. If the interface is found to be busy, the calculator can then branch to do other operations while periodically checking interface status. Once a Status Check operation indicates that the interface is ready, the calculator can begin the I/O operation.

See your PC 2 Block or Extended I/O ROM Operating Manual for information on using the Status Check operation.

EXTERNAL RELAY CONTROL

Figure 2-3 shows a scheme for using the 11202A as a relay-driver card. Up to eight relays can be controlled independently with any 9800-Series calculator**.

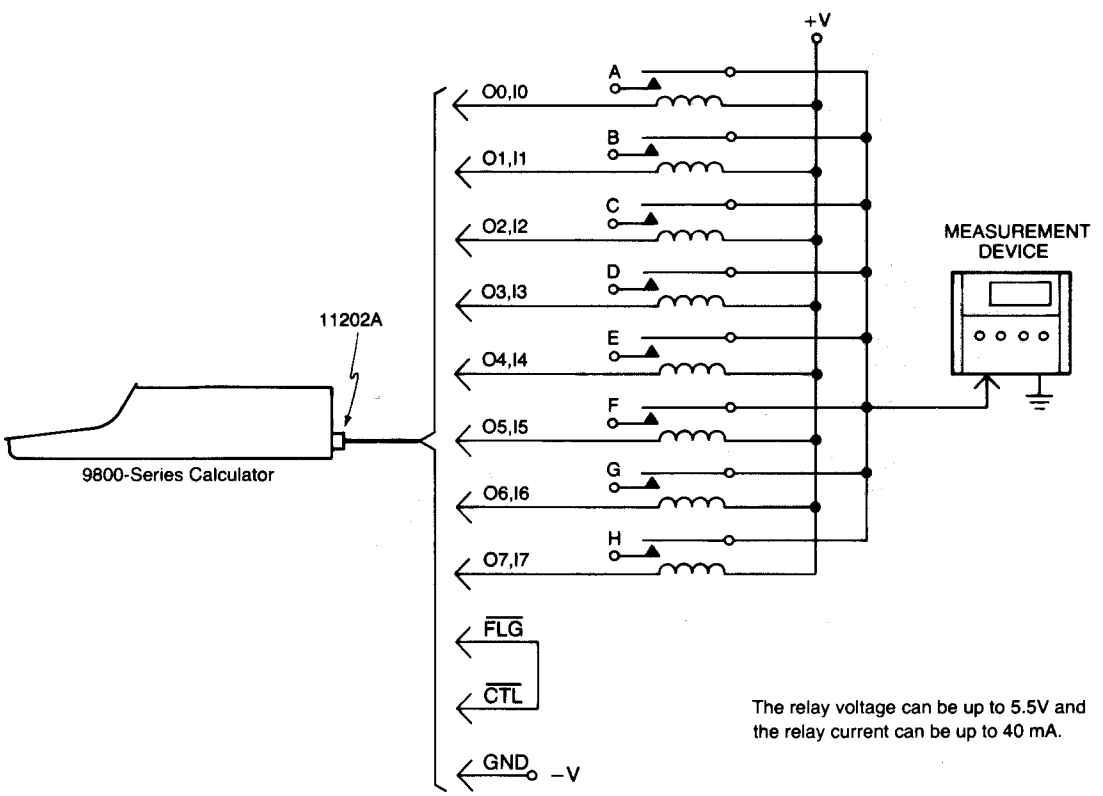


Figure 2-3. Relay Control Application

*Available only with a PC 2 Block (Model 9810A, 9820A or 9821A) or an Extended I/O ROM (Model 9830A).

**With a 9820A or 9821A Calculator, only six lines can be independently controlled unless the WRITE BYTE statement (PC2 Block) is used.

EXTERNAL RELAY CONTROL

(continued)

To select an input to the device, the calculator must output an ASCII character that causes all output lines to remain high except one — the low output causes current flow through the selected relay. Since the interface data-output lines are connected to the data-input lines, the output character will remain valid (holding the selected relay closed) until the next character is output.

Here is a list of usable ASCII output characters*:

To select this input:	Output this ASCII character:		or WRITE BYTE:
A	SOH	(00000001)	1
B	STX	(00000010)	2
C	EOT	(00000100)	4
D	FE_0	(00001000)	8
E	DC_0	(00010000)	16
F	space	(00100000)	32
G	@	(01000000)	64
H	———	———	128
(no input)	NULL	(00000000)	0

For example, to select input G, the appropriate line below could be executed (select code 1 is assumed):

Model 10:

FMT 4 1 FMT ↑ ROLL @ FMT

or 6 4 FMT 6 1 x→( ) (PC 2 only)

Model 20 or 21:

```
FMT "@",2;WRT 1⊢
```

or `WTB 1,64⊢` (PC 2 only)

Model 30:

```
10 FORMAT B
20 WRITE (1,10)"@";
```

After the character '@' is output, its binary equivalent form is held on the interface output lines as shown on the next page ('0'=high, '1'=low).

*Also, see the list of ASCII characters at the back of this manual.

Output line:	State:	Relay (condition):
OØ	0	A(open)
O1	0	B(open)
O2	0	C(open)
O3	0	D(open)
O4	0	E(open)
O5	0	F(open)
O6	1	G(closed)
O7	0	H(open)

An application of the relay controller scheme just described is shown in Figure 2-4. The system is used to measure and plot diode V-I characteristics.

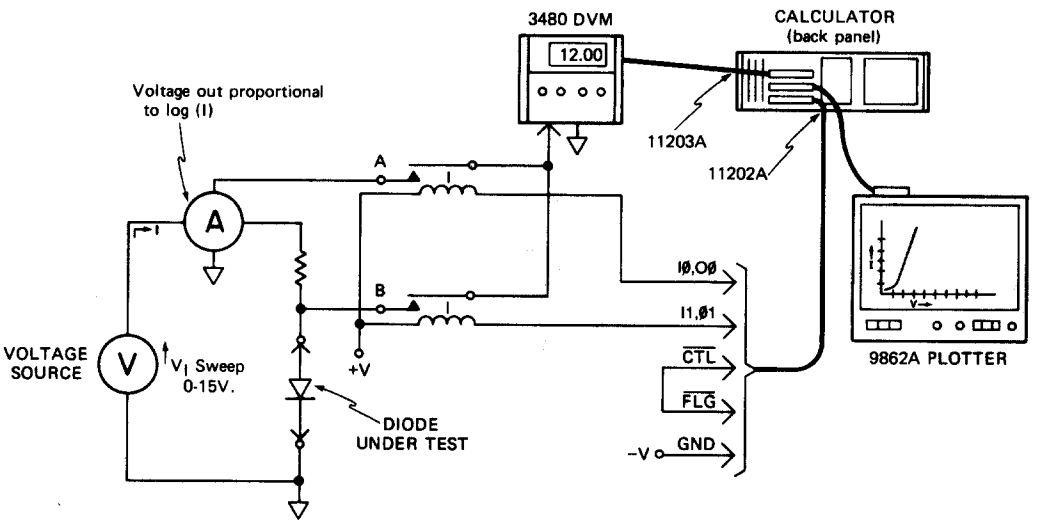
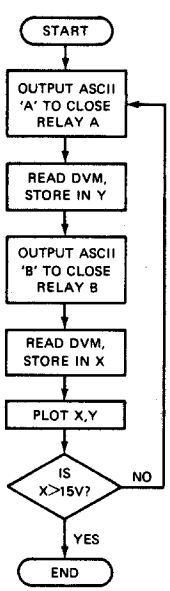


Figure 2-4. Sample Application

To operate the system, a program is used to alternately output two ASCII characters and then take readings from the DVM's BCD output using an 11203A BCD Interface. The program could either plot sets of V-I readings as they are taken (see the flowchart), or store a series of readings and plot them later. The plotting method used depends upon the voltage sweep time, the program execution time, and the number of V-I readings (sample density) required.



Chapter 3

SERVICE

This chapter contains a brief description of interface operation and instructions to help you troubleshoot and repair the interface. A complete circuit diagram and a list of replaceable parts are at the back of this chapter.

If you have difficulty repairing the interface or if you would rather have HP repair it, contact the nearest Sales and Service Office for assistance; office locations are listed at the back of this manual.

When ordering a replacement circuit board, specify HP Part No. 11202-66591.

CALCULATOR I/O LINES

Here is a definition of each calculator interface line used with the 11202A Interface:

> **NOTE**
>
> A bar above each line name indicates that the line goes low (<0.7V) when pulsed '1'. All other lines go high (>2.4V) when pulsed '1'.

CO∅, CO1, CO2, CO3 — **Peripheral Address lines** — used to address the correct device.

$\overline{CEO}$ — **Control Enable line** — provides the correct timing for interface operations.

$\overline{DI∅}$, $\overline{DI1}$, $\overline{DI2}$, $\overline{DI3}$, $\overline{DI4}$, $\overline{DI5}$, $\overline{DI6}$, $\overline{DI7}$ — **Calculator Data Input lines** — data is transferred in bit-parallel, character-serial, ASCII code.

DO∅, DO1, DO2, DO3, DO4, DO5, DO6, DO7 — **Calculator Data Output lines** — same I/O format as Data Input lines.

(continued)

SIØ — **Service Interrupt line** — indicates when the interface is busy (high) or ready (low).

$\overline{SIH}$ — **Calculator Service Inhibit line** — indicates when the calculator permits the interface to place data on the calculator input lines.

SO3 — **Calculator Status line** — indicates when the calculator is starting an input operation (high) or an output operation (low).

$\overline{STP}$ — **Calculator Stop line** — indicates when the STOP key is pressed. A $\overline{STP}$ signal terminates any I/O operation.

THEORY OF OPERATION

In general, the 11202A is an 8-bit, bi-directional data buffer. Although the interface has separate input and output lines, it handles data in only one direction at a time. The SO3 signal determines whether the input or output mode is set.

A simplified block diagram of the interface is shown below.

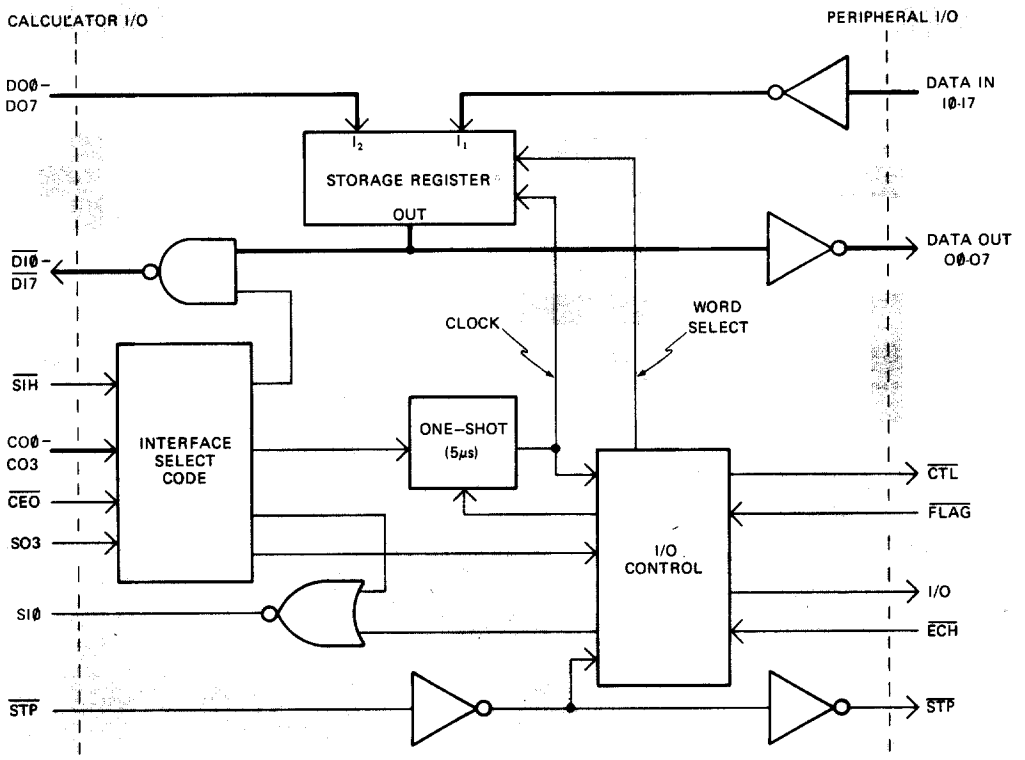


Figure 3-1. Simplified Block Diagram

DATA OUTPUT SEQUENCE (see Figure 3-2)

This sequence occurs for each output character:

1. After an appropriate OUTPUT Command or WRITE Statement is executed from the calculator, a Select Code signal is output.

2. The calculator checks interface status on the SIØ line. If the interface is not busy, data is held on the calculator output lines (DOØ-DO7) and an SO3 signal sets the I/O line low to indicate that a data-output operation has started.

3. A $\overline{CEO}$ and a Select Code signal are output. If the Select Code signal corresponds to the setting of S1, data is transferred to the interface output lines. 5μs later, the $\overline{CTL}$ line is forced low.

4. Data is held on the output lines until the peripheral device indicates 'done' by forcing $\overline{FLG}$ low. Then data on the interface input lines is loaded into the storage register and onto the output lines.

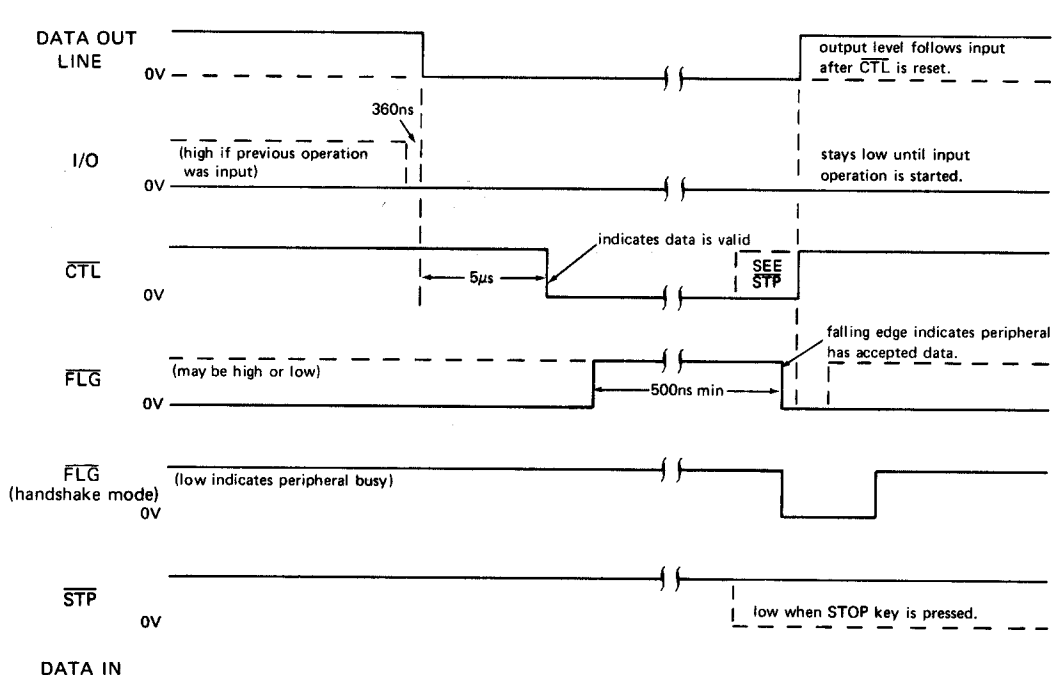


Figure 3-2. Data -Output Timing Diagram

(11202A peripheral I/O lines are shown)

THEORY OF OPERATION
(continued)

DATA INPUT SEQUENCE (see Figure 3-3)

This sequence occurs for each input character:

1. After an INPUT command or READ statement is executed from the calculator, a Select Code signal is output.

2. The calculator checks interface status on the SIØ line. If the interface is not busy, an SO3 signal sets the I/O line high to indicate that a data-input operation has started.

3. The calculator outputs $\overline{CEO}$ and Select Code signals. If the Select Code signal corresponds to the setting of S1, the $\overline{CTL}$ line is forced low. Now the calculator monitors the SIØ line, waiting until the peripheral device has output data and indicated 'done' by forcing the $\overline{FLG}$ line low. 300ns later, data is loaded into the interface and transferred to its output lines.

4. The interface then forces the SIØ line low and the calculator inputs the data on the next $\overline{SIH}$ pulse.

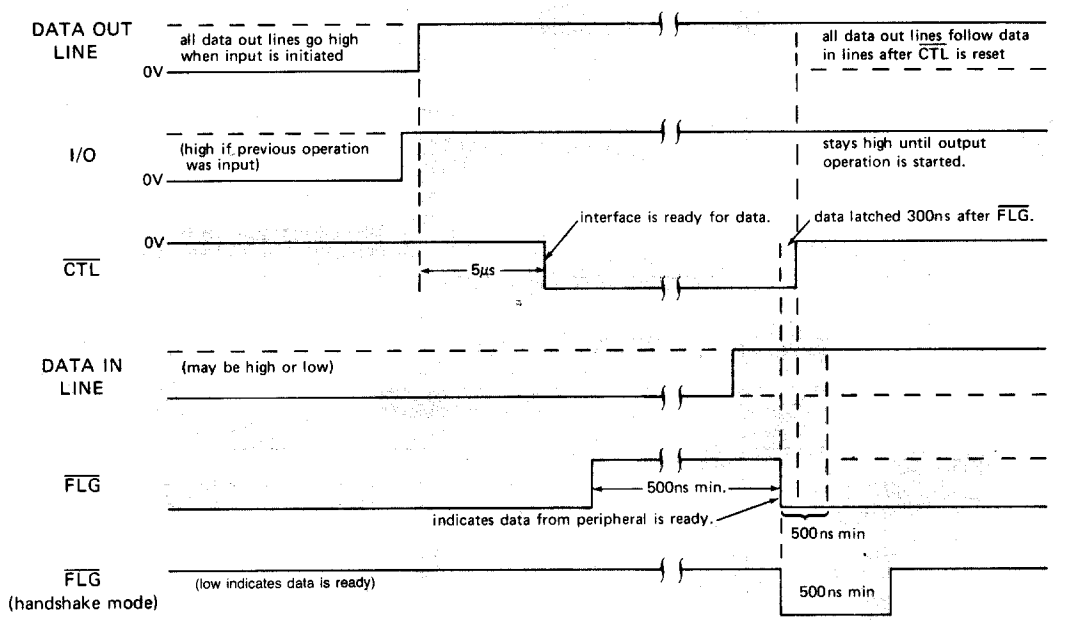
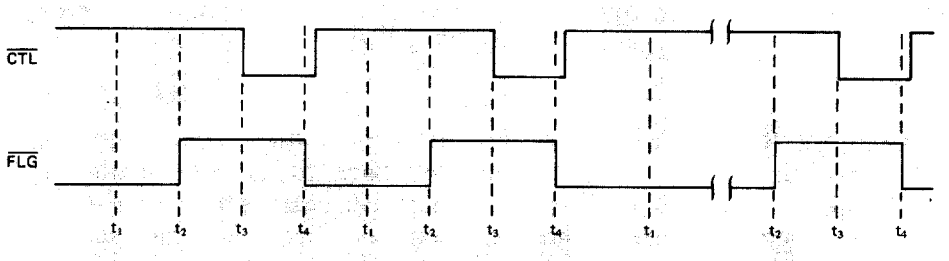


Figure 3-3. Data-Input Timing Diagram
(11202A peripheral I/O lines are shown)

HANDSHAKE MODE

Grounding the ECH line enables the interface to operate in the Handshake Mode ('handshake' refers to the interface-peripheral interaction which occurs on the $\overline{CTL}$ and $\overline{FLG}$ lines). When the Handshake Mode is enabled, the interface checks for a high $\overline{FLG}$ line before continuing the I/O operation. Whenever $\overline{FLG}$ is found to be low, the interface stays in a busy state until the peripheral forces $\overline{FLG}$ high.

Figure 3-4 shows the 'handshake' interaction between $\overline{CTL}$ and $\overline{FLG}$ lines.



t_1 – peripheral holds intefrace 'busy' by holding FLG low.

t_2 – peripheral forces FLG high to continue I/O operation.

t_3 – interface forces CTL low to indicate 'ready to accept data' or 'output data is valid'.

t_4 – peripheral forces FLG low to indicate 'data ready' or 'data accepted'. Interface will again wait until FLG is returned high.

Figure 3-4. Handshake Mode Timing Diagram

ADDITIONAL THEORY

Refer to the fold-out circuit diagram while reading the following sections.

Interface Select Logic

U1 is a 4-line to 10-line decoder which converts the BCD select code signal to a decimal output. The setting of S1 allows the interface to respond to a preset select code.

U4D outputs a 'clock' signal whenever a $\overline{CEO}$ signal and a decoded select code signal are present. U4B outputs a signal to enable the data-input gates whenever a decoded select code signal and the $\overline{SIH}$ signal permits the interface to place data on the calculator data-input lines.

One-Shot

U5 is an SN74121 monostable multivibrator which outputs a 5μs pulse whenever inputs A_1 and A_2 go low and B is high. Another pulse is output when A_1 and A_2 are low and a flag signal (via U9A) forces input B high.

THEORY OF OPERATION
(continued)

Control Logic

At the beginning of each I/O sequence, Control flip-flop U6B is preset (Q=1, Q=0) and the $\overline{CTL}$ line is high. The leading-edge of the 5μs pulse from U5 clocks U6B (Q=0,Q=1). The low Q output and the rising-edge of the clock pulse cause $\overline{CTL}$ to go low 5μs after U6B is clocked.

When the output of U4D fires one-shot U5, it also clocks I/O flip-flop U6A. When U6A is clocked, it follows the state of the SO3 line. If SO3 is low, the I/O line goes low to signal the start of an output operation. If SO3 is high, the I/O line goes high to indicate the start of an input operation.

U9A and U9B are Schmitt triggers which respond to the following-edge of the $\overline{FLG}$ signal. U9A fires one-shot U5, which clocks U6B back to its preset state and forces the $\overline{CTL}$ line high. Returning U6B to its preset state also enables the interface to force SIØ low, to indicate 'interface ready' when the calculator checks interface status. When ECH is grounded, however, SIØ is not forced low until $\overline{FLG}$ goes low and then is forced high. See Figure 3-4.

Control flip-flop U6B is immediately clocked to its preset state when a $\overline{STP}$ signal is received.

Storage Register

Four-bit registers U7 and U8 are combined to form an 8-bit data register.

The WS (word select) signal determines whether the register selects the I_2 inputs (calculator data output) or the I_1 inputs (interface data input). The $\overline{CLK}$ signal transfers the selected 8-bit word to the output lines.

When one-shot U5 is triggered the first time, the I_2 inputs will be selected since WS is high. The I_2 data is stored and output on the first $\overline{CLK}$ signal. When the one-shot is triggered the second time WS is low, causing the I_1 inputs to be selected, stored and output when the second $\overline{CLK}$ signal is seen.

TROUBLESHOOTING AND REPAIR

The following procedures assume that the calculator, ROM block(s) and peripheral device are operating correctly. If necessary, disconnect the interface from the calculator and perform all other applicable test procedures before assuming that the interface is defective.

BROKEN TRACE REPAIR

If one or more internal traces are open or have high resistance, the trace should be bridged using insulated wire, on the back of the board whenever possible.

CAUTION

TO HELP PREVENT DAMAGE TO THE CIRCUIT BOARD, USE A LOW-TEMPERATURE SOLDERING IRON WHEN REPLACING PARTS.

EQUIPEMENT REQUIRED

1) An HP 180A Oscilloscope (or equivalent), or
2) An HP 10525A Logic Probe (or equivalent).
3) The Calculator:
   - A Model 9810A with an 11264A (or equivalent) PC Block, or
   - A Model 9820A with an 11220A or 11224A PC Block, or
   - A Model 9821A with an 11220A or 11224A PC Block, or
   - A Model 9830A.
4) A test connector (see Figure 3-7) HP Part Number 11202-66592.
5) An HP 5061-0726 Board Extender (optional).

EQUIPMENT SETUP

Switch the calculator off, remove the covers from the circuit board and cable, and remove the calculator top cover. Then set up the equipment as shown in Figure 3-5. Be sure that the circuit board is installed with the circuit side *up* and is *not connected* to a peripheral device.

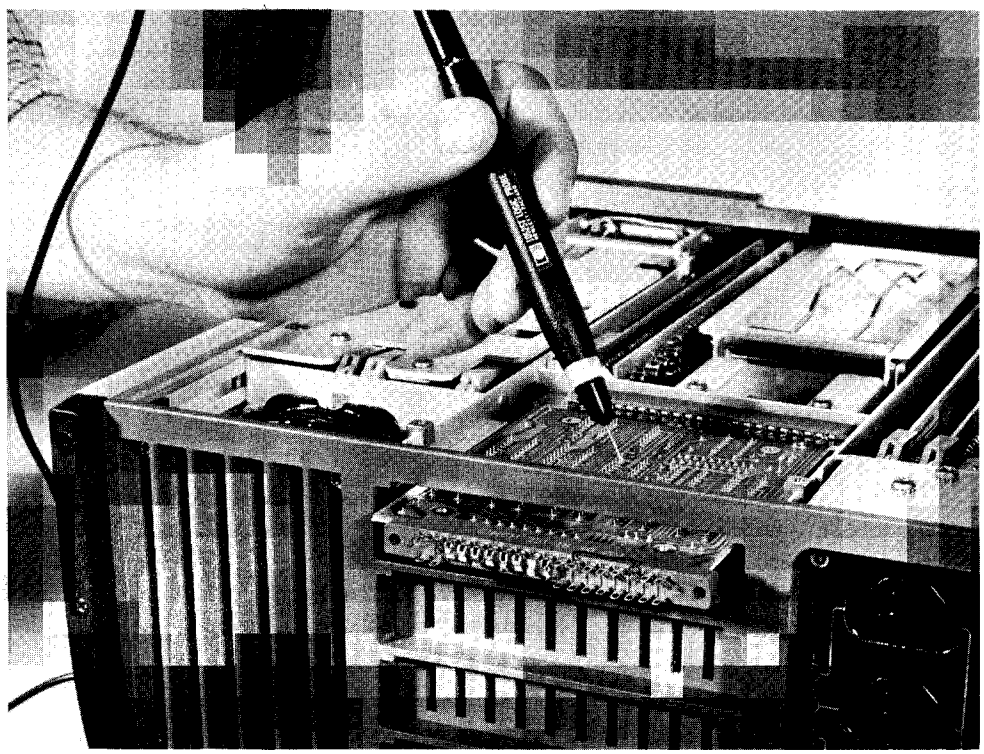


Figure 3-5. Troubleshooting the Interface

TROUBLESHOOTING AND REPAIR
(continued)

If the board extender is available, remove the covers from the circuit board and cable. Then plug the board into the board extender as shown in Figure 3-6. Be sure that the board is installed with the circuit side *out* and is *not connected* to a peripheral device.

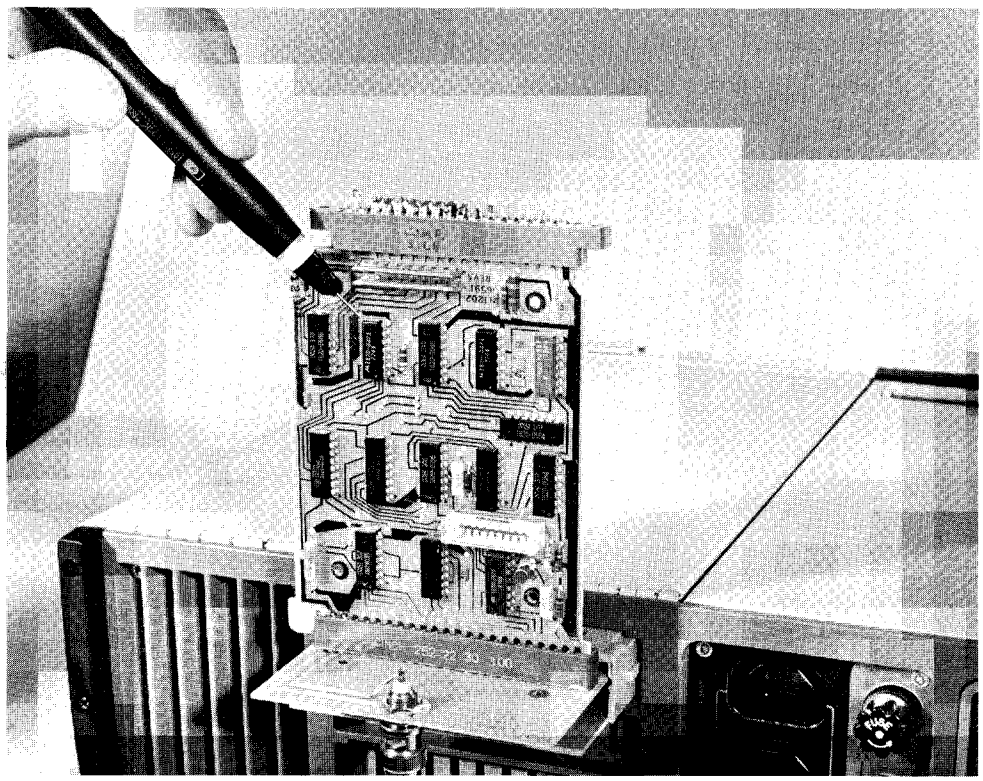


Figure 3-6. Troubleshooting with the Board Extender

PRELIMINARY CHECK

1) Install a test connector onto the circuit board, as shown in Figure 3-5 or 3-6. A wiring diagram of the connector is shown in Figure 3-7.

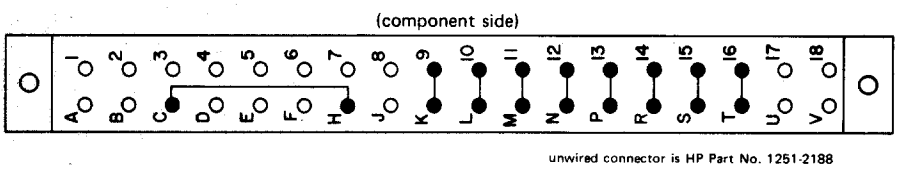


Figure 3-7. Test Connector Wiring Diagram

This connector hard-wires the interface input and output lines together, to provide storage of each output character.

2) Switch the calculator on. Then execute the appropriate key sequence or line shown below. Be sure the select code switch is set to '1'.

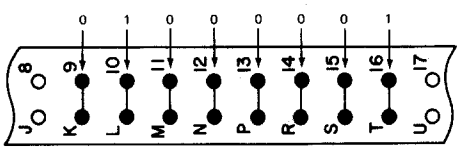
Model 10:

Model 20 or 21:
```
FMT "A";Z;WRT 1⊢
```
or
```
WTB 1,65⊢
```
(PC 2 only)

Model 30:
```
10 FORMAT B
20 WRITE (1,10) "A";
```

If the display does not return after executing the command, press STOP and CLEAR; then repeat the operation. If the display does not return after repeated attempts, see 'Troubleshooting Hints'.

3) Now check test connector pins K through T with the 'scope or logic probe to verify that binary 01000001 is present (0=high, 1=low):



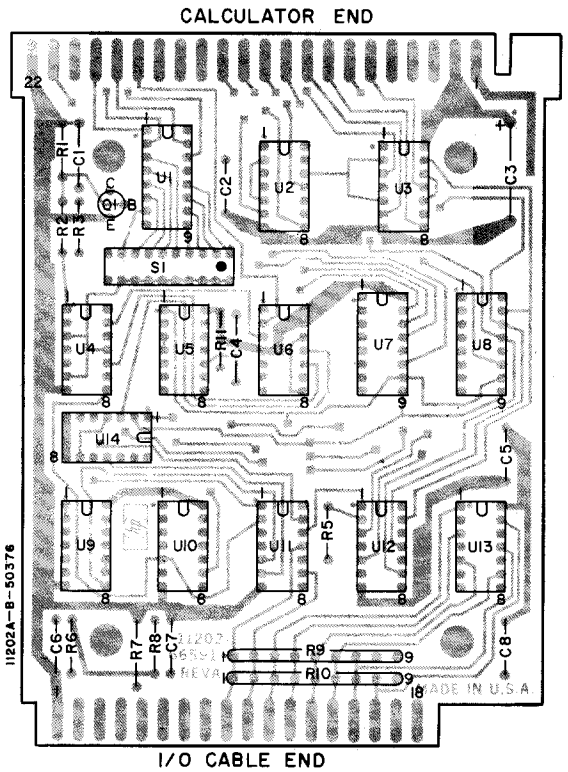
4) If the character 'A' was output correctly, output other characters (see the ASCII table in the Appendix) to further verify interface operation.

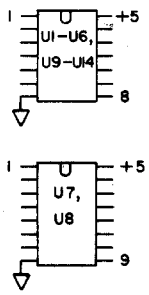
TROUBLESHOOTING HINTS

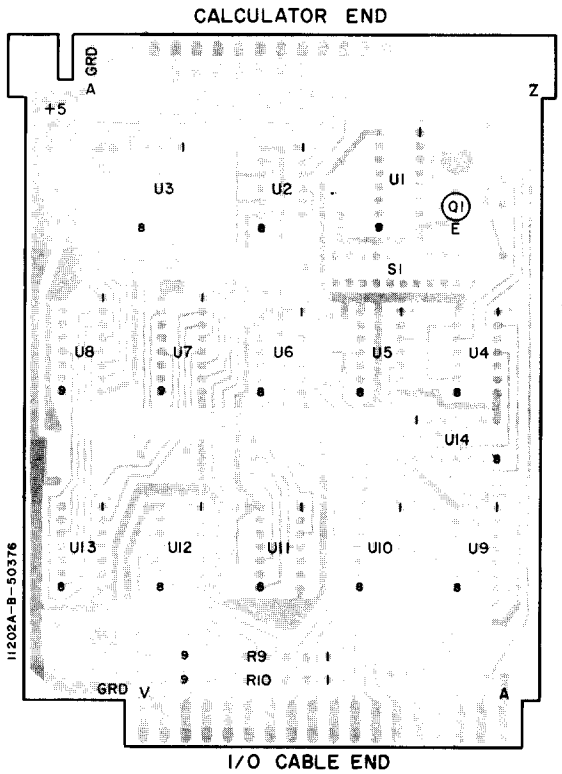
1) If the display does not return after each command is executed, press STOP and check the select code switch setting (the previous instructions specify select code 1). Also, rotate the selector-tab back and forth to ensure proper switch contact.
2) If the display returns but the data output is not correct:
   a) Check the calculator I/O lines — each line should change states as each character is output.
   b) Check the interface input and output inverters (U10, U11, U12, and U13).
   c) Verify that both Clock ($\overline{CLK}$) and Word Select (WS) pulses are present as each character is output. If not, go to step 3.
   d) Check and replace register U7 and/or U8.
3) If the display does not return after each command is executed (except when STOP is pressed):
   a) Check U1, U4B and U4D.
   b) Execute the command and check the output of U5.
   c) Execute the command and check flip-flops U6A and U6B.
   d) Check the remaining control logic.
4) If the interface outputs characters correctly but does not input data when used with a peripheral device:
   a) Check the interface cable wiring and the peripheral I/O circuits.
   b) Check NAND gates U2 and U3. Then check U4B, U11F, and U12A.

REPLACEABLE PARTS LIST

	REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION	MFR.
		11202-66591	1	P.C. Assembly	
	C1,C4	0160-0153	2	Cap: fixed, .001μF,200V,10%	
	C2,C5-C8	0160-3847	5	Cap: fixed, .01μF,25V.	
	C3	0180-0228	1	Cap: fixed, 22μF, 15V.	
	R1,R2	0684-2721	2	Res: fixed, 2.7KΩ,10%,¼w.	
	R3	0684-4721	2	Res: fixed, 4.7KΩ,10%,¼w.	
	R5	0684-3921	1	Res: fixed, 3.9KΩ,10%,¼w.	
	R7	0687-2721	1	Res: fixed, 2.7KΩ, 10%,¼w.	
	R8	0684-1521	1	Res: fixed, 1.5KΩ,10%,¼w.	
	R9	1810-0076	1	Res: network, encap, 8 resistors, 1.8KΩ each.	
	R10	1810-0041	1	Res: network,encap,8 resistors,2.7KΩ each.	
	R11	0698-4473	1	Res: fixed,8.06KΩ,1%,1/8w.	
	Q1	1854-0019	1	XSTR: Si,NPN,Similar to 2N2369.	
	S1	3101-1677	1	Switch-programming, 10 position.	
	U1	1820-0627	1	IC: Digital, One-of-ten Decoder, SL 16900	
	U2,U3	1820-0269	2	IC: Digital, Quad 2-Input NAND gate with open collectors, SN12785	
	U4,U14	1820-0584	2	IC: Digital, Quad 2-Input NOR gate, DM74L02N	
	U5	1820-0261	1	IC: Digital, Monostable Multivibrator, SN74I21N	
	U6	1820-0596	1	IC: Digital, Dual D Flip-Flop, DM74L74N	
	U7,U8	1820-0656	2	IC: Digital, Low Power 4-bit Data Selector/ Storage Register	
	U9	1820-0537	1	IC: Digital, Dual 4-Input NAND gate Schmitt Trigger, SN21158	
	U10,U12	1820-0471	2	IC: Digital, Hex Inverter/Driver, SN19235.	
	U11,U13	1820-0586	2	IC: Digital Hex Inverter, DM74L04N.	
		11200-04101	1	Cover, metal	
		5040-5911	1	Cover, plastic	
	W1	11202-61601	1	I/O Cable Assy. with connector	
	XA1	1251-2188	1	Connector, P.C.	
		7120-2940	1	Select Code Labels, package.	
		11202-90000	1	Installation and Service Manual	







A1 COMPONENT SIDE

A1 CIRCUIT SIDE

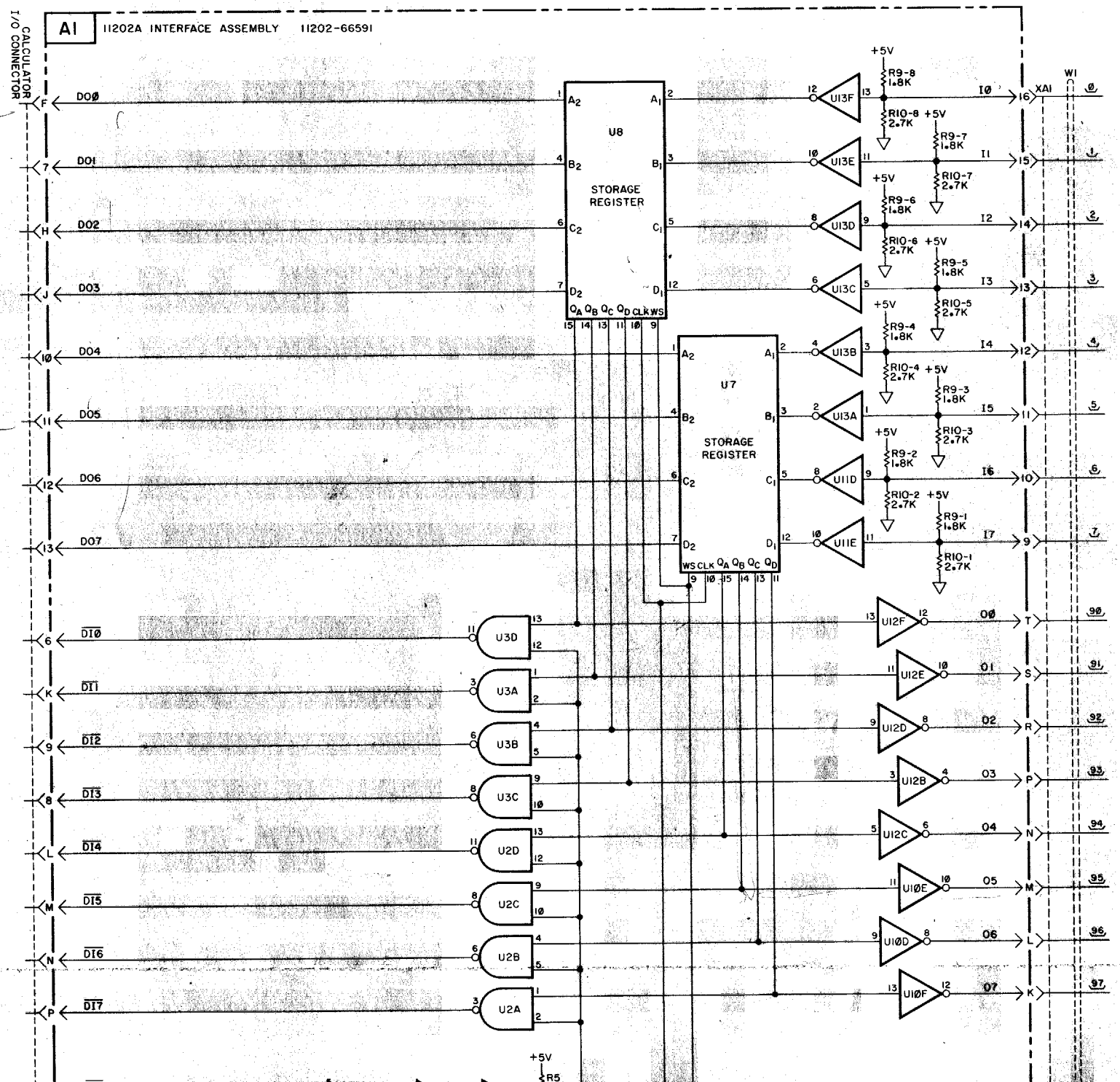
SCHEMATIC NOTES:

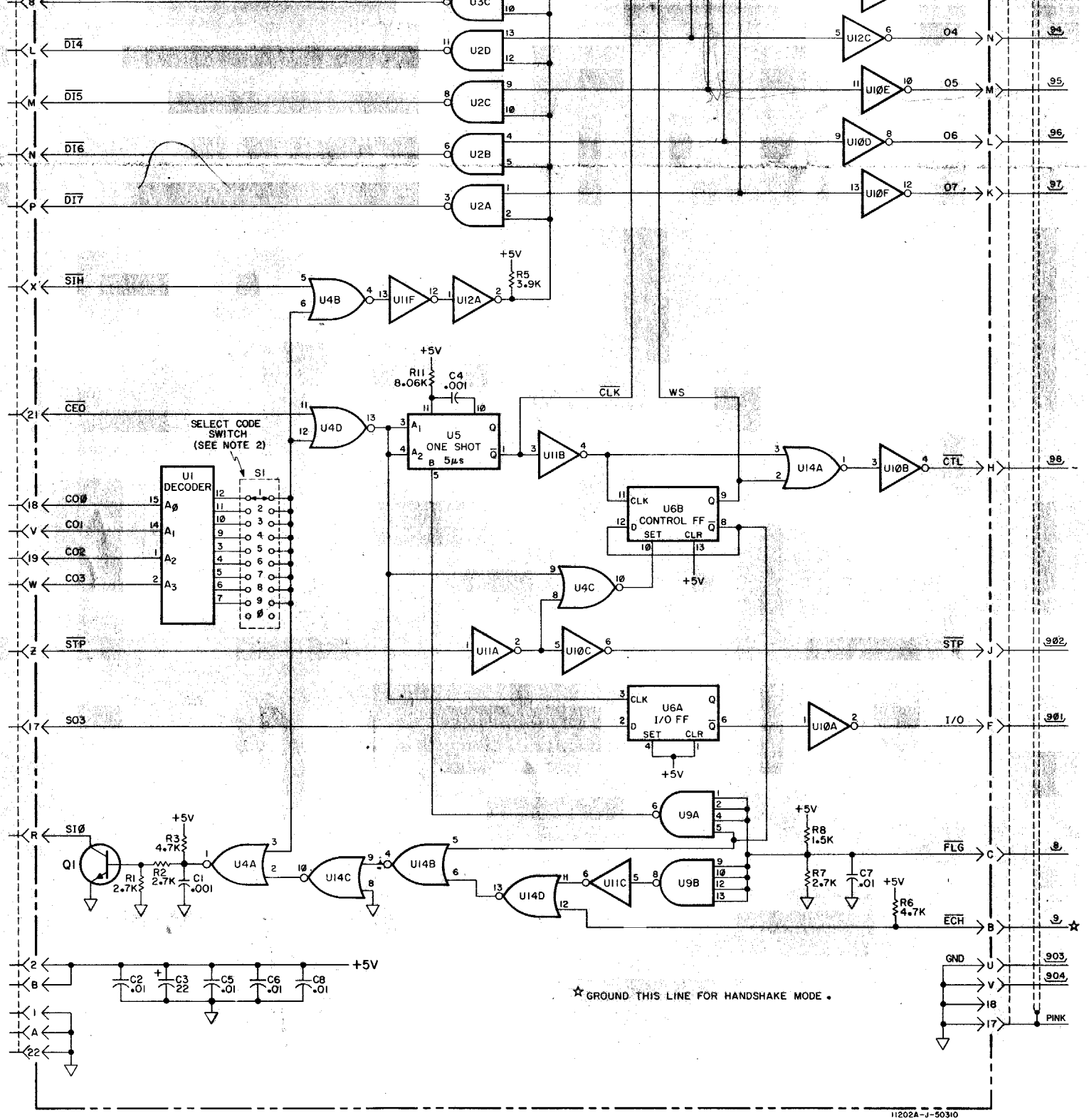
NOTE 1: Unless indicated otherwise, resistor values are shown in ohms and capacitor values are shown in microfarads.

NOTE 2: See page 1-3 before changing the setting of S1.

NOTE 3: Wire color code is the same as resistor color code: The first number indicates the base color, second number indicates the wider strip, and third color indicates the narrower strip (e.g., 924 = white, red, yellow).

0 = Black	5 = Green
1 = Brown	6 = Blue
2 = Red	7 = Violet
3 = Orange	8 = Grey
4 = Yellow	9 = White


A1
11202A INTERFACE ASSEMBLY 11202-66591
CALCULATOR I/O CONNECTOR
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
U8
STORAGE REGISTER
U7
STORAGE REGISTER
U13F
U13E
U13D
U13C
U13B
U13A
U11D
U11E
U12F
U12E
U12D
U12B
U12C
U10E
U10D
U10F
R9-8 1.8K
R10-8 2.7K
R9-7 1.8K
R10-7 2.7K
R9-6 1.8K
R10-6 2.7K
R9-5 1.8K
R10-5 2.7K
R9-4 1.8K
R10-4 2.7K
R9-3 1.8K
R10-3 2.7K
R9-2 1.8K
R10-2 2.7K
R9-1 1.8K
R10-1 2.7K
+5V
I0
I1
I2
I3
I4
I5
I6
I7
XA1
WI
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
U3D
U3A
U3B
U3C
U2D
U2C
U2B
U2A
O0
O1
O2
O3
O4
O5
O6
O7
R5



11202A INTERFACE CIRCUIT DIAGRAM

APPENDIX

I/O CHARACTERS AND EQUIVALENT ASCII (US ASCII) FORMS

ASCII Char.	EQUIVALENT FORMS			CALCULATOR KEY [1]		
	Binary	Octal	Dec [2]	9810A	9820A/9821A	9830A
@	01000000	100	64	↑ ROLL	GO TO	SHIFT RESULT
A	01000001	101	65	A	A	A
B	01000010	102	66	B	B	B
C	01000011	103	67	C	C	C
D	01000100	104	68	D	D	D
E	01000101	105	69	E	E	E
F	01000110	106	70	F	F	F
G	01000111	107	71	G	G	G
H	01001000	110	72	H	H	H
I	01001001	111	73	I	I	I
J	01001010	112	74	J	J	J
K	01001011	113	75	K	K	K
L	01001100	114	76	L	L	L
M	01001101	115	77	M	M	M
N	01001110	116	78	N	N	N
O	01001111	117	79	O	O	O
P	01010000	120	80	π	P	P
Q	01010001	121	81	b	Q	Q
R	01010010	122	82	a	R	R
S	01010011	123	83	y→( )	S	S
T	01010100	124	84	x→( )	T	T
U	01010101	125	85	1/x	U	U
V	01010110	126	86	int x	V	V
W	01010111	127	87	IN- DIRECT	W	W
X	01011000	130	88	y←( )	X	X
Y	01011001	131	89	x←( )	Y	Y
Z	01011010	132	90	x^2	Z	Z
[	01011011	133	91	$\sqrt{x}$	PG3 [4]	—
\	01011100	134	92	LABEL	√	—
]	01011101	135	93	CHG SIGN	PG2 [4]	—
^	01011110	136	94	ENTER EXP	ENTER EXP	↑
_	01011111	137	95	SUB RETURN	→	—

ASCII Char.	EQUIVALENT FORMS			CALCULATOR KEY [1]		
	Binary	Octal	Dec [2]	9810A	9820A/9821A	9830A
`	01100000	140	96	↑ ROLL	GO TO	—
a	01100001	141	97	A	A	SHIFT A
b	01100010	142	98	B	B	SHIFT B
c	01100011	143	99	C	C	SHIFT C
d	01100100	144	100	D	D	SHIFT D
e	01100101	145	101	E	E	SHIFT E
f	01100110	146	102	F	F	SHIFT F
g	01100111	147	103	G	G	SHIFT G
h	01101000	150	104	H	H	SHIFT H
i	01101001	151	105	I	I	SHIFT I
j	01101010	152	106	J	J	SHIFT J
k	01101011	153	107	K	K	SHIFT K
l	01101100	154	108	L	L	SHIFT L
m	01101101	155	109	M	M	SHIFT M
n	01101110	156	110	N	N	SHIFT N
o	01101111	157	111	O	O	SHIFT O
p	01110000	160	112	π	P	SHIFT P
q	01110001	161	113	b	Q	SHIFT Q
r	01110010	162	114	a	R	SHIFT R
s	01110011	163	115	y→( )	S	SHIFT S
t	01110100	164	116	x→( )	T	SHIFT T
u	01110101	165	117	1/x	U	SHIFT U
v	01110110	166	118	int x	V	SHIFT V
w	01110111	167	119	IN- DIRECT	W	SHIFT W
x	01111000	170	120	y←( )	X	SHIFT X
y	01111001	171	121	x←( )	Y	SHIFT Y
z	01111010	172	122	x^2	Z	SHIFT Z
{	01111011	173	123	$\sqrt{x}$	PG3 [4]	—
|	01111100	174	124	LABEL	√	—
}	01111101	175	125	CHG SIGN	PG2 [4]	—
~	01111110	176	126	ENTER EXP	ENTER EXP	—
DEL	01111111	177	127	SUB RETURN	→	—

11202A-C-50673 T-0001

ASCII Char.	EQUIVALENT FORMS			CALCULATOR KEY [1]		
	Binary	Octal	Dec [2]	9810A	9820A/9821A	9830A
NULL	00000000	000	0	CONTINUE	SPACE	—
SOH	00000001	001	1	IF FLAG	STOP	—
STX	00000010	002	2	IF x<y	1 PC2 [4]	—
ETX	00000011	003	3	IF x=y	≠	—
EOT	00000100	004	4	IF x>y	$	—
ENQ	00000101	005	5	GO TO	LOAD	—
ACK	00000110	006	6	PAUSE	&	—
BELL	00000111	007	7	↓	'	—
BS	00001000	010	8	x⇄y	8 PC1 [4]	—
HTAB	00001001	011	9	x⇄y	+	—
LF	00001010	012	10	CLEAR	*	—
VTAB	00001011	013	11	CLEAR	2 PC1 [4]	—
FF	00001100	014	12	SET FLAG	,	—
CR	00001101	015	13	SET FLAG	−	—
DLE	00010000	020	16	0	NORMAL	—
DC1	00010001	021	17	IF FLAG	TRACE	—
DC2	00010010	022	18	IF x<y	FIXED N	—
DC3	00010011	023	19	IF x=y	FLOAT N	—
DC4	00010100	024	20	IF x>y	4	—
NAK	00010101	025	21	GO TO	5	—
SYNC	00010110	026	22	PAUSE	6	—
ETB	00010111	027	23	↓	7	—
CAN	00011000	030	24	—	8 PC1 [4]	—
EM	00011001	031	25	—	9 PC1 [4]	—
ESC	00011011	033	27	—	2 PC2 [4]	—

ASCII Char.	EQUIVALENT FORMS			CALCULATOR KEY [1]		
	Binary	Octal	Dec [2]	9810A	9820A/9821A	9830A
space	00100000	040	32	CONTINUE	SPACE	Space Bar
!	00100001	041	33	1	STOP	SHIFT ! 1
"	00100010	042	34	2	1 PC2 [4]	—
#	00100011	043	35	3	≠	SHIFT # 3
$	00100100	044	36	4	$	SHIFT $ 4
%	00100101	045	37	5	%	SHIFT % 5
&	00100110	046	38	6	&	SHIFT & 6
'	00100111	047	39	7	'	SHIFT ' 7
(	00101000	050	40	8	(	(
)	00101001	051	41	9	)	)
*	00101010	052	42	×	*	*
+	00101011	053	43	+	+	+
,	00101100	054	44	CLEAR x	,	,
−	00101101	055	45	−	−	−
.	00101110	056	46	.	.	.
/	00101111	057	47	÷	/	/
0	00110000	060	48	0	0	0
1	00110001	061	49	1	1	1
2	00110010	062	50	2	2	2
3	00110011	063	51	3	3	3
4	00110100	064	52	4	4	4
5	00110101	065	53	5	5	5
6	00110110	066	54	6	6	6
7	00110111	067	55	7	7	7
8	00111000	070	56	8	8	8
9	00111001	071	57	9	9	9
:	00111010	072	58	×	R( )	* :
;	00111011	073	59	+	2 PC2 [4]	+ ;
<	00111100	074	60	CLEAR x	≤	SHIFT < ,
=	00111101	075	61	−	=	=
>	00111110	076	62	.	>	SHIFT > .
?	00111111	077	63	÷	?	SHIFT ? /

[1] When SHIFT is shown, the SHIFT key is held down while the following key is pressed. Where a key is not shown in the 9830A column, use a WRITE (FORMAT B) statement to output the decimal-equivalent number.

[2] Decimal numbers are used with PC2 READ BYTE, WRITE BYTE, and 9830A WRITE (FORMAT B) statements.

[3] The keys colored light-brown correspond to the shifted output mode; refer to the appropriate PC Block Operating Manual for instructions.

[4] These are the blank keys and are numbered from top to bottom as on the 9820A or 9821A keyboard. The characters can be output with the indicated PC Block.

Scan Copyright ©
The Museum of HP Calculators
www.hpmuseum.org

Original content used with permission.

Thank you for supporting the Museum of HP Calculators by purchasing this Scan!

Please to not make copies of this scan or make it available on file sharing services.