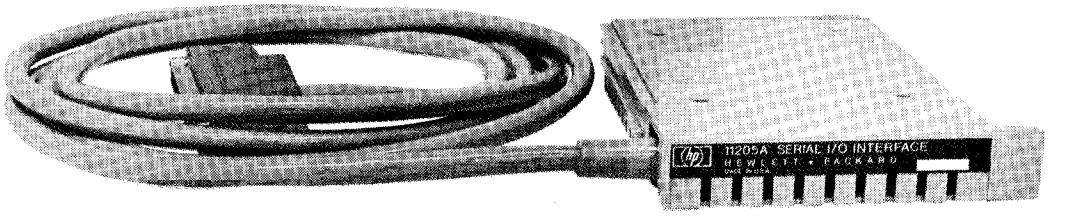
INSTALLATION and SERVICE MANUAL

11205A SERIAL INTERFACE



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Chapter 1
GENERAL INFORMATION

INTRODUCTION

The -hp- 11205A Serial I/O Interface enables a variety of data communications terminals to be used in a 9800 Series calculator system. When using this interface and an appropriate peripheral control block, data and other ASCII-coded* information can be transferred between the calculator and a device that conforms to EIA** specification RS-232-C (e.g., a teletypewriter or a CRT communications terminal.)

This manual describes how to install and service the 11205A Interface and contains instructions for operating equipment such as a Teletype Model ASR33 or ASR38 with 9800 Series calculators.

THE PERIPHERAL CONTROL BLOCK

In general, each calculator must have an appropriate peripheral control block when using this interface. The manual supplied with the block describes how to control and exchange data with peripheral equipment. Contact your nearest -hp- Sales and Service Office for information on the correct peripheral control block for your calcualtor system; office locations are listed at the back of this manual.

The 9830A Calculator does not need a peripheral control block if the terminal is used as a printer only. See Appendix F in the 9830A Operating and Programming Manual for instructions on connecting a 'primary printer' to the calculator.

HARDWARE DESCRIPTION

The interface consists of a circuit card inside a case (which plugs into any one of the calculator I/O connectors) and an eight-foot shielded cable. One end of the cable is connected to the circuit card and the other end is wired to a standard, 25-pin EIA connector.

TECHNICAL SPECIFICATIONS

I/O Format

The interface sends and receives information in standard, 8-bit serial ASCII code. Since the 8-bit character is combined with one 'start' bit and one or two 'stop' bits, the I/O character format can be set to either 10- or 11-bit format (see DATA FORMAT, page 1-4).

*American Standard Code for Information Interchange.
**Electronic Industries Association.

Character Transfer (BAUD) Rates

Any one of these five BAUD rates can be selected (the interface is supplied to you set at 110 BAUD):

110 BAUD (10 char/sec when using 11-bit format)
150 BAUD (15 char/sec when using 10-bit format)
300 BAUD (30 char/sec when using 10-bit format)
600 BAUD (60 char/sec when using 10-bit format)
1200 BAUD (120 char/sec when using 10-bit format)

Signal Levels

Interface I/O and control signal levels conform to EIA RS-232-C specifications.

Signal Lines

(pin numbers refer to a 25-pin EIA connector)

Pin 1 **Protective Ground**
Pin 2 **Data Input** (from terminal to calculator)
Pin 3 **Data Output** (from calculator to terminal)
Pin 5 **Clear To Send signal** – greater than 3v indicates that the calculator is ready to receive data.
Pin 6 **Data Set Ready signal** – line is always at +9v to hold terminal in 'ready-to-receive' state.
Pin 7 **Signal Ground**
Pin 11 **Peripheral Busy signal** – line is not normally used but can be wired to signal the calculator when the terminal is ready to accept data:

not ready signal >+3v.
ready signal <–3v.

Power

The interface is powered from the calculator.

INSTALLATION CONSIDERATIONS

SETTING THE BAUD RATE

The interface BAUD rate must be set by means of a BAUD RATE switch to match the character transfer rate of the terminal device (see the list of available BAUD rates on page 1-2). If your terminal accepts or transmits data at a different rate than is available on the interface, the interface BAUD rate can be adjusted by changing the value of two components (see NOTE 5 on the circuit diagram).

The BAUD Rate switch is accessible through a small hole in the interface card. Switch settings are marked on the card. When setting the switch, carefully rotate the switch using a small, flat-blade screwdriver.

SELECT CODE

Since all peripheral devices are connected to the calculator in a party-line fashion, each device must have a unique address so that the calculator can specify which device must respond to each operation. This address, or 'select code', consists of a one or two-digit number and is preset on the interface card.

Although the 11205A Interface is set to respond to select code 15 when supplied, you can set any one of nine other select codes by following this procedure:

1. Switch the calculator and the terminal OFF.
2. Disconnect the interface from the calculator. Remove the four screws located on the top of the card assembly; turn the card over and lift off the bottom cover.
3. Locate the Select Code Switch (see Figure 1-1). Raise the hinged cover on the switch. Using a small, flat-blade screwdriver, *carefully rotate* the selector tab until it is positioned at the desired select code number. Numbers are printed on the side and on the top cover of the switch ('0' corresponds to select code 15). Before closing the cover, be sure the slot in the selector tab is at a right angle to the length of the switch.

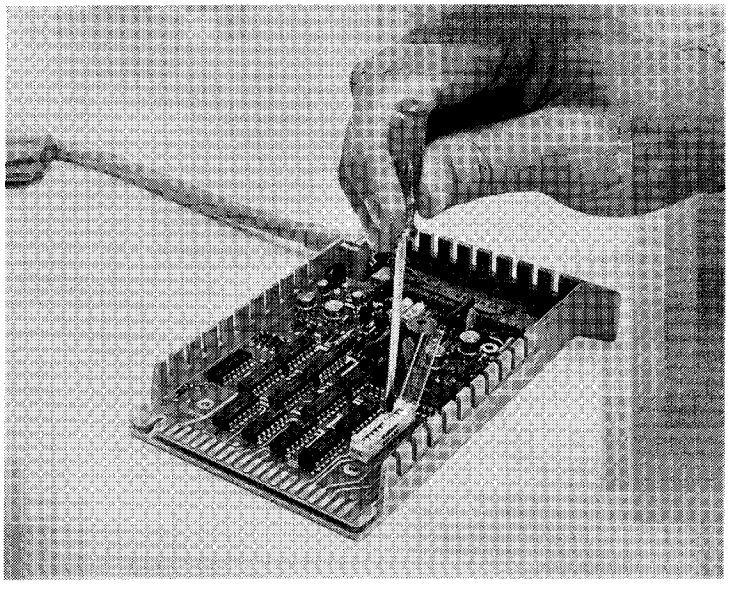


Figure 1-1. Setting The Select Code

4. Close the switch cover and replace the interface card bottom cover. Secure the cover with the four screws which were removed in step 2.
5. Place a select code label on the peripheral device to indicate the new select code. A package of labels is supplied with the interface.
6. Reconnect the interface to the calculator, and turn the calculator and the terminal ON. Verify that the desired select code is set by executing an I/O operation (or running a program) which specifies the new select code.

DATA FORMAT

The interface can accept serial data which is transmitted in either 10- or 11-bit format (i.e., one or two 'stop' bits accompany each character). The interface is set to 11-bit format when supplied; however, 10-bit format can be set by changing the position of R2 on the interface circuit board.

CAUTION

USE A LOW-WATTAGE SOLDERING IRON WHEN RELOCATING PARTS, TO HELP AVOID DAMAGE TO THE MULTILAYER BOARD.

OUTPUT DELAY

The interface provides an internal delay of about 200 msec. after transmitting any of these ASCII control characters:

FE_0	(Format Effector)
H_{tab}	(Horiz. Tab)
LF	(Line Feed)
V_{tab}	(Vert. Tab)
FF	(Form Feed)
CR	(Carriage Return)

That delay is adequate to allow most terminals to respond to control characters. If you wish to disable the internal delay and permit the terminal to control the output rate, change the position of R11 on the interface board and connect the 'peripheral ready line' from your terminal to pin 11 of the interface cable connector (see 'Pin 11' on page 1-2).

Chapter 2

OPERATING INSTRUCTIONS

Many data communications terminals are available which can be used with the 11205A Interface. However, you should verify the terminal's operating characteristics (conformance to EIA specification RS-232-C, compatible BAUD rate, etc.) when considering using that device in your calculator system.

At present, the 11205A Interface has been used with each of the following devices.

HP Model 2600A CRT Terminal
HP Model 2762A Teleprinter
Teletype Model ASR33*
Teletype Model ASR38**

The Teletype Model ASR38 is used in the following examples as representative of the type of terminal that is compatible with this interface.

GETTING STARTED

To set the teletype for calculator-controlled operation, press the LINE button.

The teletype tapepunch can be controlled manually by using the TAPE PUNCH lever. Transferring data to the calculator via the teletype tapereader is not possible, however, unless the terminal has been modified to enable tapereader control via the Clear-To-Send interface line (-hp- cannot make that modification).

Most of the examples in this chapter assume that the interface is set to select code 15.

*Must be equipped with a Teletype No. 186136 (automatic answer) or 198420 (manual answer) Voltage Interface Kit.
**Must be equipped with Teletype No. 188724 Interface Cable.

MODEL 10 SYSTEM

The 11205A Interface can be used with a Model 9810A Calculator and a peripheral control block to control any of the devices previously listed. For more information on the peripheral control block operations to be described, see Chapter 2 of your Peripheral Control Block Operating Manual.

MESSAGE OUTPUT

FMT 4 (select code) FMT (character keys) FMT

This sequence outputs ASCII Characters from the Model 10 to the teletype. See the table in Appendix A for the available output characters. Also, to output lower case alpha characters to the ASR38, precede the output character keys with the ↑(SHIFT) key.

For example, to output the characters 'ABCabc' and then output a CR/LF instruction,

PRESS: FMT 4 1 5 FMT

PRESS: A B C ↑ A B C ↑

PRESS: SET FLAG CLEAR FMT

PRINTOUT: ABCabc

DATA OUTPUT

FMT 4 (select code) PRINT SPACE

Data in the X-register is output as a string of ASCII-coded numeric characters.

For example, to output π in the FLOAT format,

PRESS: CLEAR FLOAT π

PRESS: FMT 4 1 5 PRINT SPACE

PRINTOUT: 3.141592654E 00

DATA INPUT

FMT 3 (select code) .

This sequence causes the calculator to accept a series of ASCII-coded characters. The calculator ignores all characters other than +, −, decimal point, or digits prior to accepting data. Each character except 'E' is entered into the X-register as it is received. The 'E' character causes the next two digits, and + or −, to be entered as an exponent. Any other character input after data terminates the input operation.

As an example, here is how to input π from the teletype:

On the calculator,

PRESS: (CLEAR) (FLOAT)

PRESS: (FMT) (3) (1) (5) (.)

On the teletype,

PRESS: (3) (.) (1) (4) (space bar)

DISPLAY: x 3.140000000 00

MODEL 20 SYSTEM

Except where noted, the following operations can be performed using either the 11220A PC I Block or the 11224A PC II Block. Refer to your Peripheral Control Block Operating Manual for information on formatting.

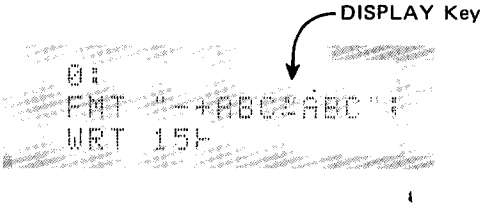
MESSAGE OUTPUT

Execute a line of the form:

FMT " <message> " ; WRT <select code>

The table in Appendix A lists the available output characters. To output lower-case alpha to the ASR38, precede the <message> with the DISPLAY key.

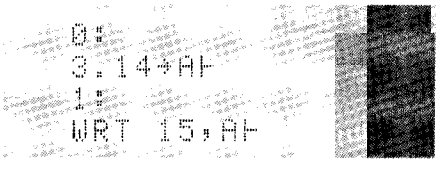
The following program line outputs a CR/LF instruction and the characters 'ABCabc'.



DATA OUTPUT

Data is output by first storing the data in a register, and then executing a WRITE statement to output that register's contents.

The following program lines output π within the free-field (default) format.



DATA INPUT

Data is input by executing a READ statement. NOTE: When a PC I block is used, READ statements can be executed from a program only.

See your Peripheral Control Block Operating Manual for a description of delimiter characters and the data-input format.

For example, to input data, first load and run this program:*

```
0:
FMT *;RED 15,A%
1:
PRT A;SPC 2%
2:
END %
```

Then key in a number on the teletype and terminate the entry with any non-numeric key.

THE WRITE BYTE STATEMENT (PC II only)

WTB <select code> , <decimal number>

The <decimal number> is the decimal equivalent of the ASCII character to be output and can be expressed as a positive integer, a variable (by using a register name), or an expression. The number must be a positive integer in the range of from 0 to 255. The decimal equivalents of ASCII output characters are listed in the table in Appendix A.

The following program line outputs the ASCII character FF to advance the paper when printing forms.

```
0:
WTB 15,12%
```

THE READ BYTE STATEMENT (PC II only)

RDB <select code>

or

RDB <select code> ⇒ <register name>

This statement accepts the first character input and converts it to a decimal equivalent number. The number is entered into Z unless another register name is specified.

> **NOTE**
>
> Any device which outputs a parity bit (such as the ASR38) causes some characters to be read as values that are 128 greater than their decimal equivalent forms – this problem cannot be avoided.

*The FORMAT statement (line 0) is not needed to specify free-field format if the PC I Block is used.

For example, to input and print single characters, first load and run this program:

```
0:
FXD 0⊢
1:
RDB 15→A⊢
2:
PRT A;SPC 1⊢
3:
GTO 1⊢
4:
END ⊢
```

Now, on the teletype,

PRESS: (1) (2) (3) ___ (ø)

```
177    1
178    2
 51    3
180    4
 53    5
 54    6
183    7
184    8
 57    9
 48    0
```

Notice in the printout that some numeric characters (3, 5, 6, 9, 0) are represented as their decimal equivalents (see Appendix A), but other characters are represented by decimal values 128 greater than expected.

MODEL 30 SYSTEM

With the 11205A Interface, the teletype can be used as the 'primary printer'* for the Model 9830A Calculator. Simply use the instructions in Appendix F of the 9830A Operating and Programming Manual.

*The teletype must be set to select code 15 in order to operate as the primary calculator printer.

The teletype can also be used as a 'secondary printer' when a WRITE statement of this form is used:

WRITE (select code, format) "(characters or data)"

The following additional operations are available when the 11272 Extended I/O ROM is used.

THE ENTER STATEMENT

ENTER (select code, format) variable list

For example, the following statement inputs and stores three data values (each point is seperated by a non-numeric key). The '*' character specifies free-field input format.

```
80 ENTER(15,*)A,B,C
```

See Chapter 3 of the Extended I/O ROM Operating Manual for other uses of the ENTER statement.

THE WRITE BYTE FUNCTION

WBYTE decimal number

The ASCII equivalent of the decimal number specifed is output. For example, executing the following line rings the teletype's bell.

```
10 WRITE(15,*)WBYTE7
```

NOTE

When transmitting a single Carriage Return instruction, be sure to output *two* CR characters to ensure that the teletype has sufficient time to respond to the instruction.

THE READ BYTE FUNCTION

RBYTE select code

For example, executing the following line accepts the first character input and stores its decimal equivalent number into the X-register.

```
10 X=RBYTE 15
```

Chapter 3
SERVICE

This chapter contains a description of interface operation and instructions to help you troubleshoot and repair the interface circuits. A complete circuit diagram and a list of replaceable parts are at the back of this chapter.

This chapter describes Revision B interface boards. See Appendix B at the back of the manual for information on Revision A boards.

If you have difficulty repairing the interface or if you would rather have -hp- repair it, contact the nearest -hp- Sales and Service Office for assistance; office locations are listed in the back of this manual.

When ordering a replacement interface circuit board, specify -hp- Part No. 11205-66591.

CALCULATOR I/O LINES

Here is a definition of each calculator interface line used with the 11205A Interface.

> **NOTE**
>
> A bar above each line name indicates that the line goes low (ØV) when pulsed '1'; all other lines go high (+5V) when pulsed '1'.

CØØ
CO1
CO2
CO3

Peripheral Address lines — used to address the correct device.

$\overline{\text{CEO}}$

Control Enable line — provides the correct timing for interface operations.

DIØ
DI1
DI2
DI3
DI4
DI5
DI6
DI7

Calculator Data Input lines — data is transferred in bit-parallel, character-serial, ASCII code.

DOØ
DO1
DO2
DO3
DO4
DO5
DO6
DO7

Calculator Data Output lines — same I/O format as Data Input lines.

SIØ

Service Interrupt line — a logic '1' (high) indicates that the terminal is busy.

$\overline{\text{SIH}}$

Calculator Service Inhibit line — indicates that the calculator is busy and cannot input data.

$\overline{SO2}$ **Calculator Status line** — indicates that select code 15 is being output.

$\overline{STP}$ **Calculator Stop line** — indicates that the STOP key is pressed. An STP signal terminates the I/O operation.

GENERAL THEORY OF OPERATION

In general, the 11205A Interface is a serial -to- parallel data converter. When receiving data, it converts bit-serial, ASCII-coded data to bit-parallel, ASCII-coded data usable by the calculator. When sending data, it converts bit-parallel, ASCII-coded data to bit-serial ASCII code usable by terminal devices.

A simplified block diagram of the interface circuits is shown below.

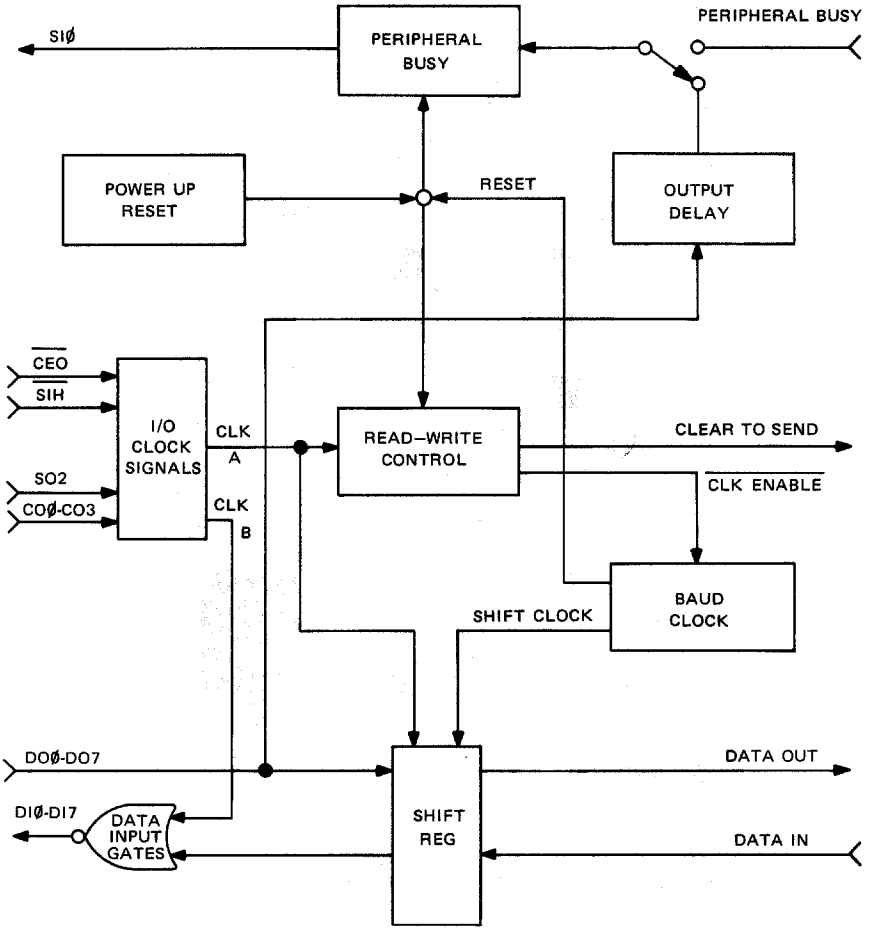


Figure 3-1. Simplified Block Diagram

DATA OUTPUT SEQUENCE (See Figure 3-2)

This sequence occurs for each output character:

1. The $\overline{CEO}$ and Select Code signals are combined to provide I/O clock signals 'A' and 'B'. The Read-Write Control circuit responds to the Clock A and holds the Clear To Send line low during the output operation. The Peripheral Busy Circuit responds to Clock B by sending a 'Terminal Busy' signal to the calculator.
2. After the data character is loaded into the Shift Register, the BAUD Clock is enabled for 10 or 11 counts (depending upon the setting of R2). Each time the Shift Register is clocked, one character bit is transferred to the terminal.
3. After the terminal receives the last bit(s) (one or two stop bits), it can signal the interface via the Peripheral Busy line. That line need not be used, however, since an internal delay is provided to delay output operation after certain control characters are sent.

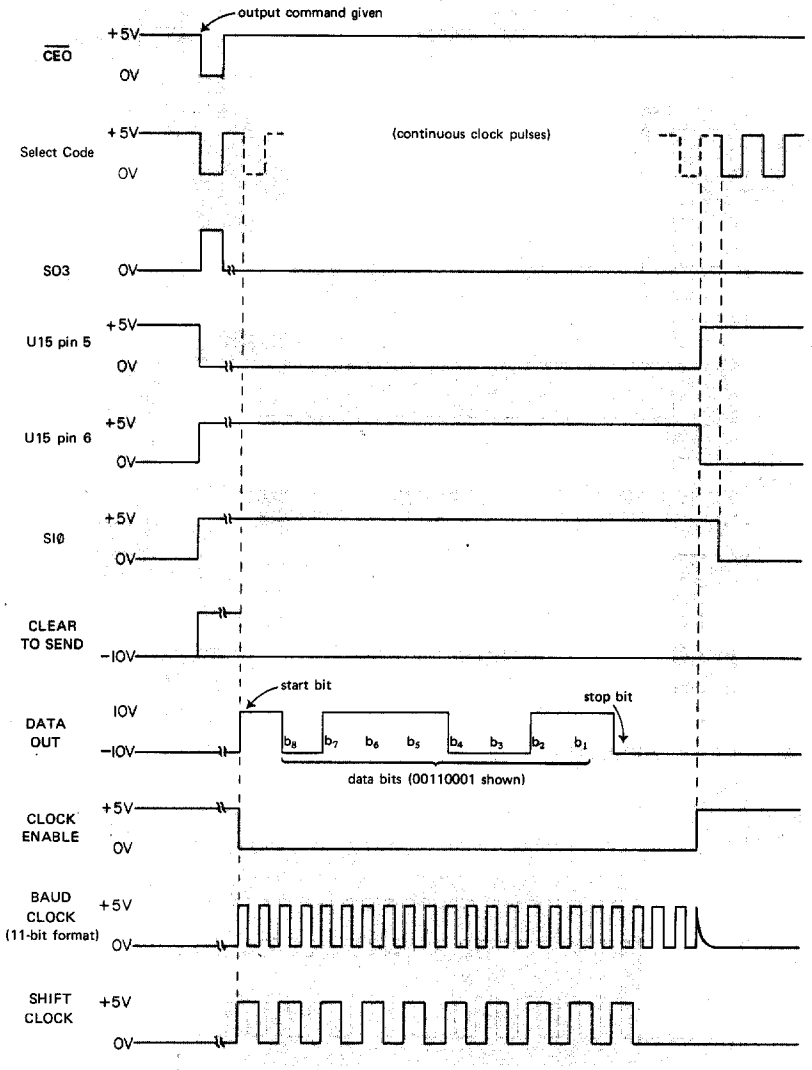


Figure 3-2. Data Output Timing Diagram

DATA INPUT SEQUENCE (See Figure 3-3)

This sequence occurs for each input character:

1. The $\overline{CEO}$ and Select Code signals provide a Clock A signal which is used to load the data from DOØ through DO7 into the Shift Register. The Read-Write Control circuit also responds to Clock A by forcing the Clear To Send line high, which signals the terminal to output a character. Also, SIØ goes high to indicate that the terminal is busy.
2. When the start bit is received, the BAUD Clock is enabled for 10 or 11 counts. Then the Shift Register loads one data bit with each clock pulse. If two stop bits are received, the second one is ignored.
3. The BAUD Clock is disabled after outputting 10 or 11 pulses, depending upon the setting of R2. Then SIØ is forced low from either an Output Delay signal or a Peripheral Busy signal.
4. Finally, the Data Input gates are enabled and the character is transferred to the calculator.

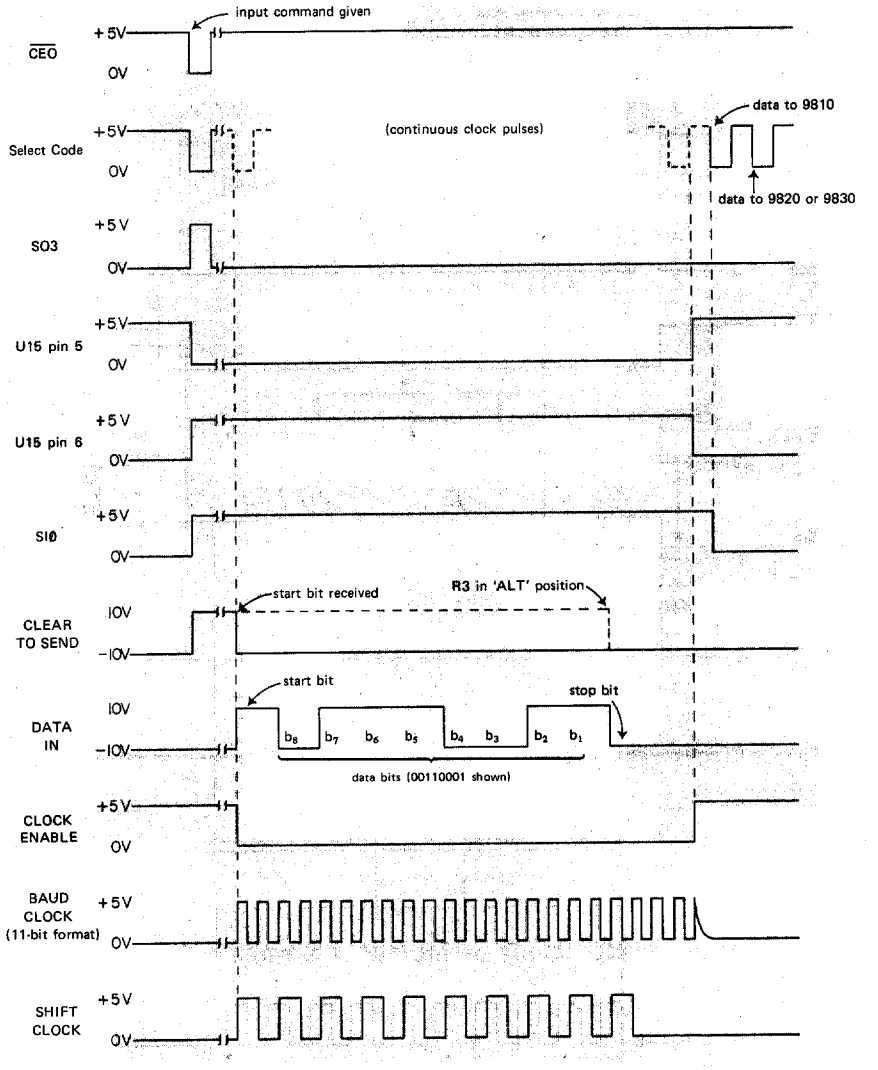


Figure 3-3. Data Input Timing Diagram

DETAILED THEORY OF OPERATION

I/O CLOCK (Refer to page 3-19)

Clock A is generated from the decoded select code signal and Clock B consists of the select code and the $\overline{CEO}$ signal.

U11 is a 4-to-10-line decoder which converts the 4-line BCD select code signal to a Øvolt signal on one of 10 output lines. Clock A and Clock B signals are present only if S1 is set to the position corresponding to the select code signal being received.

The decoder is enabled only when $\overline{SO2}$ is high and $\overline{SIH}$ is low.

BAUD CLOCK

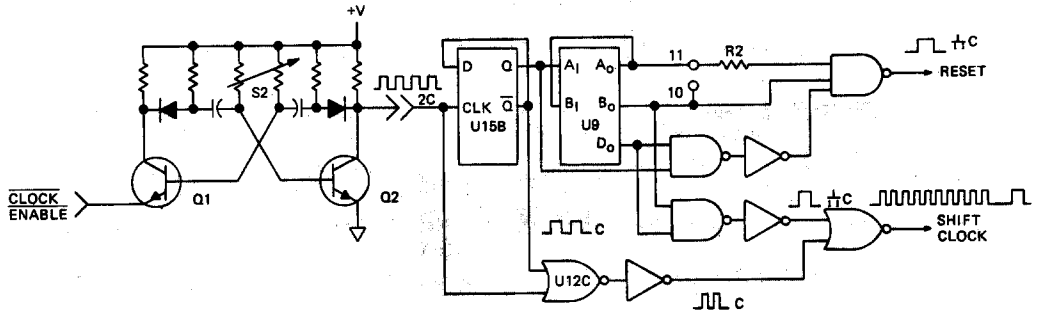


Figure 3-4. BAUD Clock Circuit

The BAUD Clock circuit generates the Reset and Shift Clock control signals. The setting of S2 determines the BAUD Clock rate and must match the I/O rate of the terminal device.

Grounding the emitter of Q1 enables multivibrator Q1–Q2, which runs at twice the BAUD rate indicated on the interface cover. The output of Q2 is halved by flip-flop U15B and shaped by NOR gate U12C. The Shift Clock signal contains either nine or ten pulses, depending upon when the clock is disabled. The Reset signal is output after every 10 or 11 Shift Clock pulses. The position of R2 determines when the Reset signal is output.

READ – WRITE CONTROL

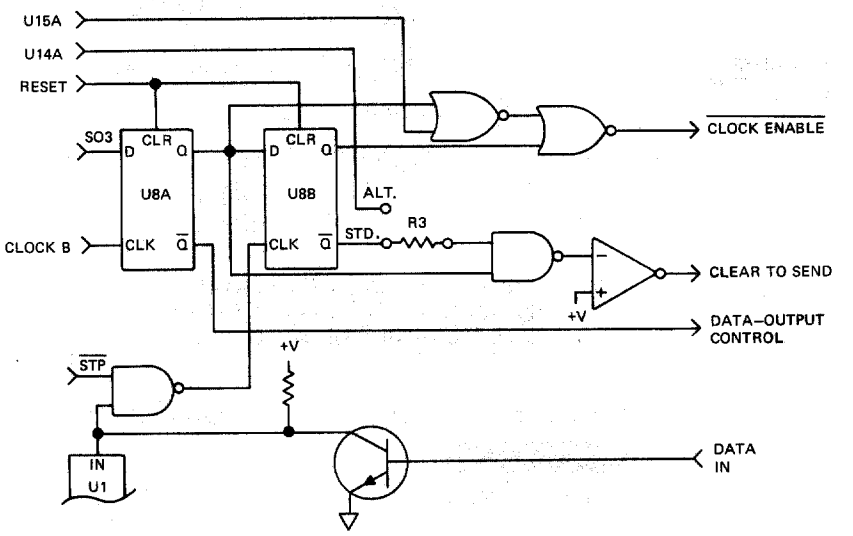


Figure 3-5. Read-Write Control Circuit

The Read-Write Control circuit determines whether the interface is in the input or output mode and signals the terminal as to which mode is set via the Clear To Send line.

The output mode is set either when calculator power is switched ON or after the BAUD Clock outputs a Reset signal (see the BAUD CLOCK section). The Power-Up Reset circuit generates a Reset pulse whenever calculator power is switched ON.

At the start of each output operation, U8A is clocked low (Q is low) to initiate a $\overline{\text{Clock Enable}}$ signal. The $\overline{\text{Clock Enable}}$ line remains low until U15A is cleared by a Reset pulse. Then the Clear To Send line is forced low for the entire output operation.

At the start of each input operation, U8A is clocked high (Q is high) and forces the Clear To Send line high. As the first data bit appears on the Data In line, U8B is clocked low to force the Clear To Send line low. The $\overline{\text{Clock Enable}}$ signal is also generated from the U8B low output. The $\overline{\text{Clock Enable}}$ line remains low until the Reset pulse is generated. If R3 is in the alternate position, the Clear To Send line is held high until the last Shift Clock pulse is generated (see the timing diagram on page 3-4).

SHIFT REGISTER (Refer to page 3-19)

The Shift Register consists of the 4-bit registers U1 and U4 and the flip-flops U6A and U6B. Together, they handle 10-bit I/O characters, which contain the 8-bit ASCII character, one 'start' bit and one 'stop' bit.

During input operations, each bit of serial data from the terminal is clocked into the Shift Register on the leading edge of the Shift Clock signal. The data is then held on the Shift Register output lines until the Input NAND Gates (U2 and U3) are enabled and the data is gated to the calculator.

During output operations, the parallel ASCII-coded data on lines DOØ through DO7 is loaded into U1 and U4. Then, as each bit is shifted through the Shift Register, it is transferred to the terminal via the Data Out line.

OUTPUT DELAY (Refer to page 3-19)

Whenever one of the six ASCII-coded control characters listed on page 1-4 is output, a 200 msec one-shot pulse is generated by U10. U10 is enabled when pins 3 and 4 are high and a Clock B pulse is at pins 1 and 2. When R11 is connected for 'internal delay', this pulse delays the SIØ signal to the calculator for 200 msec, to allow the terminal to respond to the output control character.

TROUBLESHOOTING AND REPAIR

EQUIPMENT REQUIRED

-hp- 180A Oscilloscope or equivalent
-hp- 10525A Logic Probe or equivalent
-hp- 10526A Logic Pulser or equivalent

The Calculator:
-hp- 9810A with a Peripheral Control Block, or
-hp- 9820A with 11224A or 11220A PC Block, or
-hp- 9830A with or without 11272 I/O ROM.

EQUIPMENT SETUP

Switch the calculator OFF, remove the covers from the circuit board and cable, and remove the calculator top cover. Then set up the equipment as shown in Figure 3-6. *Be sure that the board is installed with the circuit side up and that the interface is not connected to a terminal.*

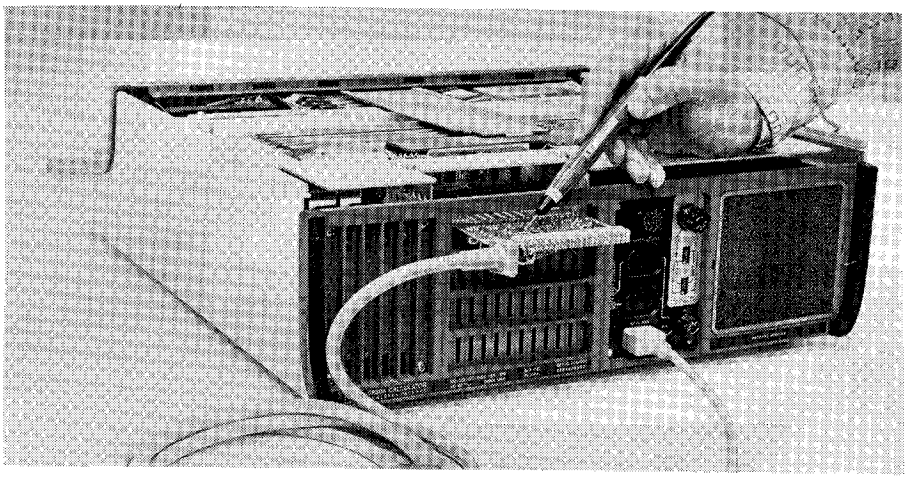


Figure 3-6. Troubleshooting The Interface

BROKEN TRACE REPAIR

If one or more internal traces are open or have high resistance, the trace should be bridged, using insulated wire, on the back of the board whenever possible.

CAUTION

USE A LOW-WATTAGE SOLDERING IRON WHEN REPLACING PARTS, TO HELP AVOID DAMAGE TO THE MULTILAYER BOARD.

POWER SUPPLY CHECKOUT (Refer to page 3-19)

Switch the calculator ON, then check the interface +9v and −9v power supplies (test points are shown on the component locator). If either voltage supply is not within ±10%, check the calculator 5v supply at the point shown on the component locator. If 5v ±2% is not measured, the calculator power supplies should be checked; refer to the Calculator Service Manual or ocntact the nearest -hp- Calculator Service Representative for assistance. assistance.

BAUD CLOCK CHECKOUT

Load the appropriate one of the following programs into your calculator before starting this procedure (each program assumes that the interface is set to select code 15).

Model 10 Calculator (a peripheral control block is required):

```
0000--FMT---42
0001--  4   --04
0002--  1   --01
0003--  5   --05
0004--FMT---42
0005--RUP---22
0006--FMT---42
0007--GTO---44
0008--  0   --00
0009--END---46
```

Model 20 Calculator (with an 11224A PC II Block):

```
0:
WTB 15,64H
1:
GTO 0H
2:
END H
```

Model 20 Calculator (with an 11220A PC I Block):

```
0:
FMT "@";WRT 15⊢
1:
GTO 0⊢
2:
END ⊢
```

Model 30 Calculator (using an 11272 I/O ROM):

```
20 WRITE (15,*)"WBYTE64"
30 GOTO 20
40 END
```

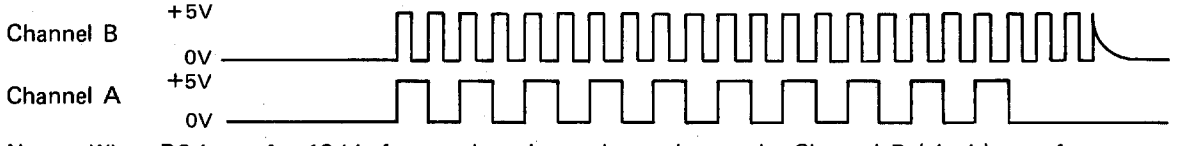
Model 30 Calculator (without an I/O ROM):

```
10 FORMAT B
20 WRITE (15,10)"@"
30 GOTO 10
40 END
```

1. Connect the 'scope to these points on the circuit board:

   Channel A → U7 pin 4
   Channel B and External Sync → pin N (interface cable connector)

2. Position the BAUD rate switch (S2) to its counter-clockwise position (1200 Hz).
3. Start the program. The following waveforms should be seen when the clock and counter are operating correctly.



Note: When R2 is set for 10-bit format there is one less pulse on the Channel B (clock) waveform.

- If the waveforms are correct (i.e., correct frequency and number of pulses) go to the 'Data Transfer Checkout' on Page 3-11.
- If the clock frequency is correct but the wrong number of pulses are seen, go to step 5.
- If the waveforms cannot be verified (i.e., the clock is dead) go to the next step.

4. a. Stop the program and verify that U15 pin 5 is low — if not, drive it low by pulsing pin 3 (replace U15 if necessary).
IMPORTANT: U15 pin 5 must be at 0v before continuing with this step.

   b. Verify that U5 pin 9 is high. If it is not high and:

   - If R11 is positioned for 'Ext. Delay', check the components related to Q6.
   - If R11 is positioned for 'Int. Delay', check the components in the Output Delay circuit.

   c. Monitor U12 pin 6 with the logic probe and start the program — U12 pin 6 should flash low as the program is started. If this pulse is not seen, the calculator is probably defective; call an -hp- Calculator Service Representative for assistance.

   d. Stop the program, monitor U12 pin 4, reset U15 pin 5 to low (see step 4a), and start the program again — U12 pin 4 should flash high as the program is started. If necessary, replace U12 and repeat this step.

   e. While running the program, check the following points and replace the associated component if the state is not seen (high = 5v; low = Øv).

COMPONENT:	STATE:
U15 pin 5	low
U15 pin 6	high
U9 pin 5	low
U8 pin 6	high
U8 pin 8	high
U8 pin 9	low
U6 pin 1	high
U12 pin 1	high
U7 pin 1	low

   If the preceding components check out but the clock is still dead, check each component associated with the clock. *IMPORTANT: If any components are replaced, be sure the clock frequency is still 1200 Hz ±1% by adjusting the values of C5 and C11.*

5. Assuming that the clock is running but that an incorrect number of pulses are seen, perform these steps to check the counter circuits:

   a. Stop the program, disconnect the circuit board from the calculator, and remove the interface cable from the circuit board.

   b. Ground the collector of Q1. Then reconnect the circuit board to the calculator.

   c. Verify that U15 pin 5 is high.

   d. Start the program and verify that the counter (U9) is reset (check that U9 pins 9, 10, 12, 13 are low); if it's not, reset it (at pin 14) with the logic pulser.

   e. Once the counter is reset (state 'ØØØØ'), check the following gates and replace any which do not check out:

COMPONENT:	STATE:
U14 pin 8	high
U14 pin 3	high
U13 pin 4	low
U13 pin 6	low
U7 pin 4	high
U5 pin 6	high

f. Using the logic pulser at U9 pin 14, increment the counter to state '10' (pin 13 = 0 , pin 9 = 1 , pin 10 = 0 , pin 12 = 1)

g. With the counter at state '10', check the following components and replace any which do not check out:

COMPONENT:	STATE:
U14 pin 8	low
U14 pin 3	low
U13 pin 4	high
U13 pin 6	high
U7 pin 4	low
U5 pin 6	high

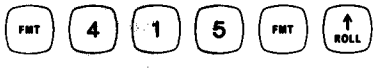
h. Monitor U5 pin 6 while incrementing the counter one more state — pin 6 should flash low (replace U5 if necessary). Now check these components and replace any which do not check out:

COMPONENT:	STATE:
U8 pin 5	low
U9 pin 9	low
U15 pin 5	high
U15 pin 6	low

i. Now replace the interface cable connector and remove the ground from Q1.

DATA TRANSFER CHECKOUT

1. Start the program used in the preceding checkout and monitor pin R on the connector with the 'scope. The waveform should match the Clear-To-Send signal shown in Figure 3-3 on page 3-4 . If the waveform cannot be verified, check and replace U16 and/or U14.
2. Stop the program, disconnect the interface card from the calculator, unplug the interface cable connector, and ground the collector of Q1.
3. Reconnect the interface card and verify that U15 pin 5 is low. If not, drive it low by pulsing pin 3.
4. Execute the appropriate instruction FROM THE CALCULATOR KEYBOARD:

Model 10: 

Model 20: `FMT "@";WRT 15⊢`

Model 30:
Store this line: `10 FORMAT B`

SHIFT,RESULT Keys

Execute this line: `WRITE (15,10)"@"`

Now check the following components and replace any which do not check out:

(low = 'ϕ', high = '1')

COMPONENT:	STATE:
U1 pin 13	ϕ
U1 pin 12	1
U1 pin 10	ϕ
U1 pin 9	ϕ
U4 pin 13	ϕ
U4 pin 12	ϕ
U4 pin 10	ϕ
U4 pin 9	ϕ
U6 pin 5	ϕ
U6 pin 8	ϕ

5. Use the logic pulser to pulse U1 pin 7 — the '1' bit which is at U1 pin 12 should shift through the register in the same order as the pins are listed above (from U1 pin 13 to U6 pin 8).
6. When the '1' bit is at U6 pin 8, check these points:

COMPONENT:	STATE:
U6 pin 8	low
U7 pin 10	low
U7 pin 13	high
DATA IN line (pins 15,S)	−10v

7. Press STOP. Then reconnect the interface cable connector, remove the ground from Q1, and connect the 'scope to pin N of the interface cable connector.
8. Verify that U15 pin 5 is high. Then execute the following appropriate instruction FROM THE CALCULATOR KEYBOARD:

Model 10: [FMT] [4] [1] [5] [PRINT SPACE]

Model 20: `RED 15,A⊢`

Model 30*: `ENTER (15,*)A`

*If an 11272 ROM is not available, check U14, Q5 and go to step 9.

Now monitor U7 pin 1 with the logic probe while applying +5v to pins 16 and T of the interface cable connector; U7 pin 1 should pulse low as pins 16 and T are forced high (this means that the clock is enabled and will run for 10 or 11 counts). If the foregoing sequence doesn't occur, check U14, Q5, and the components associated with Q5.

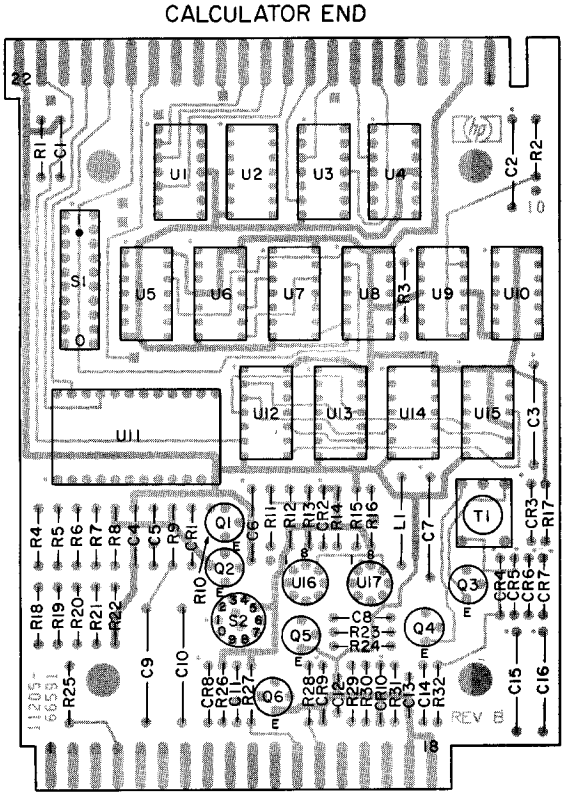
9. Finally, check gates U2 and U3 with the logic probe.

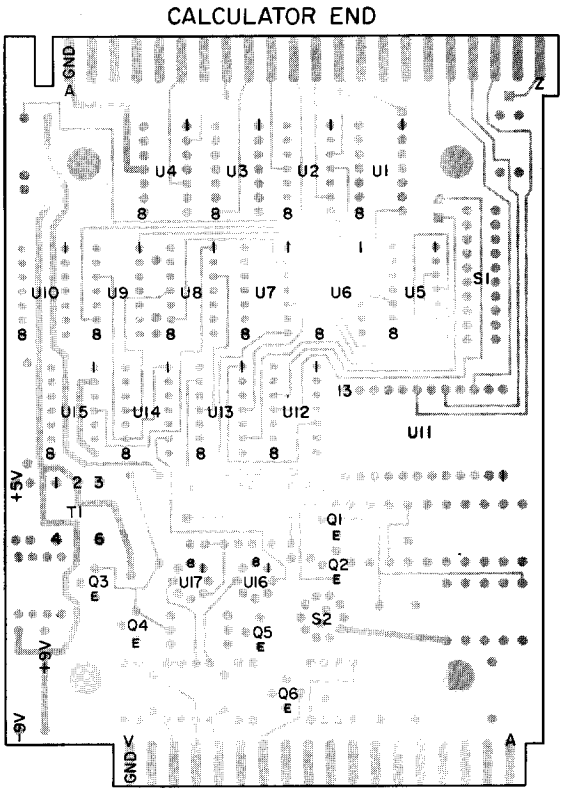
If you have successfully performed all of the preceding checkouts and the interface still has a problem, you can either go back to the beginning and try again or call an -hp- Service Representative for assistance.

REPLACEABLE PARTS LIST

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A1	11205-66591	1	PC Board Assembly, REV.B
C1	0160-3847	2	Cap.,Fixed: .01μF,25V
C2	0180-0106	2	Cap.,Fixed: 60μF,6V
C3	0180-1861	1	Cap.,Fixed: 27μF,15V
C4	0160-3847		Cap.,Fixed: .01μF,25V
C5	*	1	(installed during calibration)
C6	0180-1701	1	Cap.,Fixed: 6.8μF,6V
C7	0180-0106		Cap.,Fixed: 60μF,6V
C8	0150-0023	2	Cap.,Fixed: 2000PF,1000V
C9,C10	0160-2612	2	Cap.,Fixed: .027μF,50V
C11	*	1	(installed during calibration)
C12,C13	0160-0938	2	Cap.,Fixed: 1000PF,100V
C14	0150-0023		Cap.,Fixed: 2000PF,1000V
C15,C16	0180-1746	2	Cap.,Fixed: 15μF,20V
CR1	1901-0040	9	Diode: Si,.05A,30V
CR2	1901-0028	1	Diode: Si,.75A,400V
CR3-CR10	1901-0040		Diode: Si,.05A,30V
U1	1820-0599	2	IC:Digital
U2,U3	1820-0269	2	IC:SN7403N
U4	1820-0599		IC:Digital
U5	1820-0907	1	IC:SN74I2N
U6	1820-0596	3	IC:DM74L74N
U7	1820-0584	2	IC:SN74L02
U8	1820-0596		IC:DM74L74N
U9	1820-0443	1	IC:SN74L93N
U10	1820-0913	1	IC:Digital
U11	1820-0702	1	IC:SL17303
U12	1820-0584		IC:SN74L02
U13	1820-0174	1	IC:SN7404N
U14	1820-0583	1	IC:DM74L00
U15	1820-0596		IC:DM74L74N
U16,U17	1820-0203	2	IC:Op. Ampl,741C
L1	9140-0114	1	Inductor: 10μH
Q1,Q2	1854-0071	2	Transistor: Si,NPN
Q3,Q4	1854-0556	2	Transistor: Si,NPN
Q5,Q6	1854-0354	2	Transistor: Si,NPN

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
R1	0684-5621	6	Res.,Fixed: 5600Ω,5%,1/4W.
R2,R3	0684-0271	3	Res.,Fixed: 2.7Ω,5%,1/4W.
R4,R5	0698-4121	4	Res.,Fixed: 11.3KΩ,1%,1/8W.
R6	0757-0349	2	Res.,Fixed: 22.6KΩ,1%,1/8W.
R7	0698-4496	2	Res.,Fixed: 45.3KΩ,1%,1/8W.
R8	0698-4493	2	Res.,Fixed: 34KΩ,1%,1/8W.
R9	0683-1825	2	Res.,Fixed: 1800Ω,5%,1/4W.
R10	0683-1335	2	Res.,Fixed: 13KΩ,5%,1/4W.
R11	0684-0271		Res.,Fixed: 2.7Ω,5%,1/4W.
R12	0683-2735	2	Res.,Fixed: 27KΩ,5%,1/4W.
R13	0684-5621		Res.,Fixed: 5600Ω,5%,1/4W.
R14	0757-0278	1	Res.,Fixed: 1780Ω,1%,1/8W.
R15	0757-0420	1	Res.,Fixed: 750Ω,1%,1/8W.
R16	0684-5621		Res.,Fixed: 5600Ω,5%,1/4W.
R17	0683-2735		Res.,Fixed: 27KΩ,5%,1/4W.
R18,R19	0698-4121		Res.,Fixed: 11.3KΩ,1%,1/8W.
R20	0757-0349		Res.,Fixed: 22.6KΩ,1%,1/8W.
R21	0698-4496		Res.,Fixed: 45.3KΩ,1%,1/8W.
R22	0698-4493		Res.,Fixed: 34KΩ,1%,1/8W.
R23	0684-5621		Res.,Fixed: 5600Ω,5%,1/4W.
R24,R25	0684-1021	3	Res.,Fixed: 1000Ω,5%,1/4W.
R26	0683-1825		Res.,Fixed: 1800Ω,5%,1/4W.
R27	0683-1335		Res.,Fixed: 13KΩ,5%,1/4W.
R28	0684-5621		Res.,Fixed: 5600Ω,5%,1/4W.
R29,R30	0684-3311	2	Res.,Fixed: 330Ω,5%,1/4W.
R31	0684-5621		Res.,Fixed: 5600Ω,5%,1/4W.
R32	0684-1021		Res.,Fixed: 1000Ω,5%,1/4W.
S1	3101-1677	1	Program Switch, 10 position
S2	3100-3228	1	Rotary Switch, 5P2T
T1	9100-3403	1	Inverter Transformer
W1	11205-61601	1	Cable Assembly w/connectors
	11205-04103	1	Interface cover, metal
	5040-5911	1	Interface case, plastic
	7120-2940	2	Select Code Labels
	11205-90000	2	Manual





SCHEMATIC NOTES:

NOTE 1: Unless indicated otherwise, resistor values are shown in ohms and capacitor values are shown in microfarads.

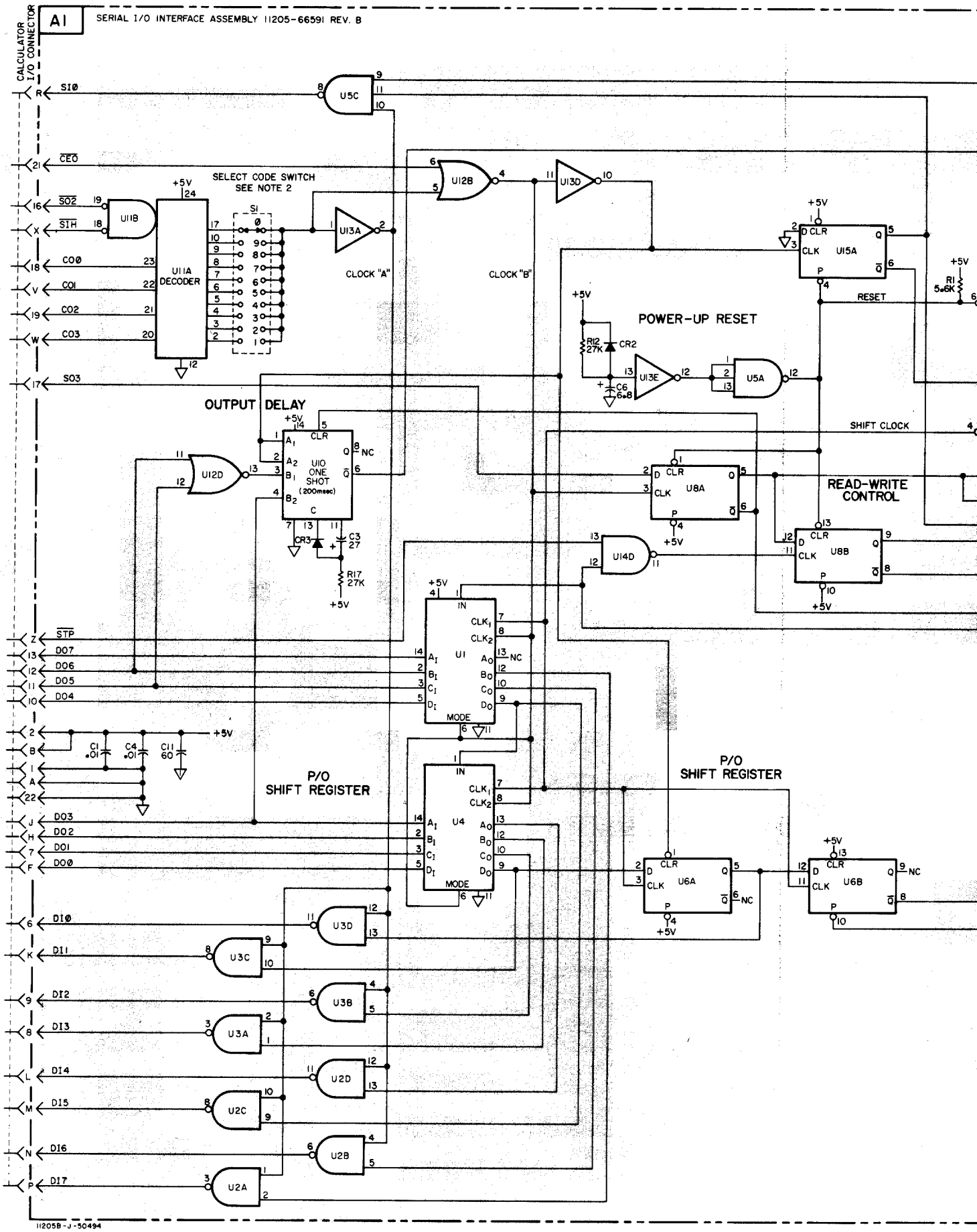
NOTE 2: Position '0' on the select code switch corresponds to select code 15. See page 1-3 before changing the setting of this switch.

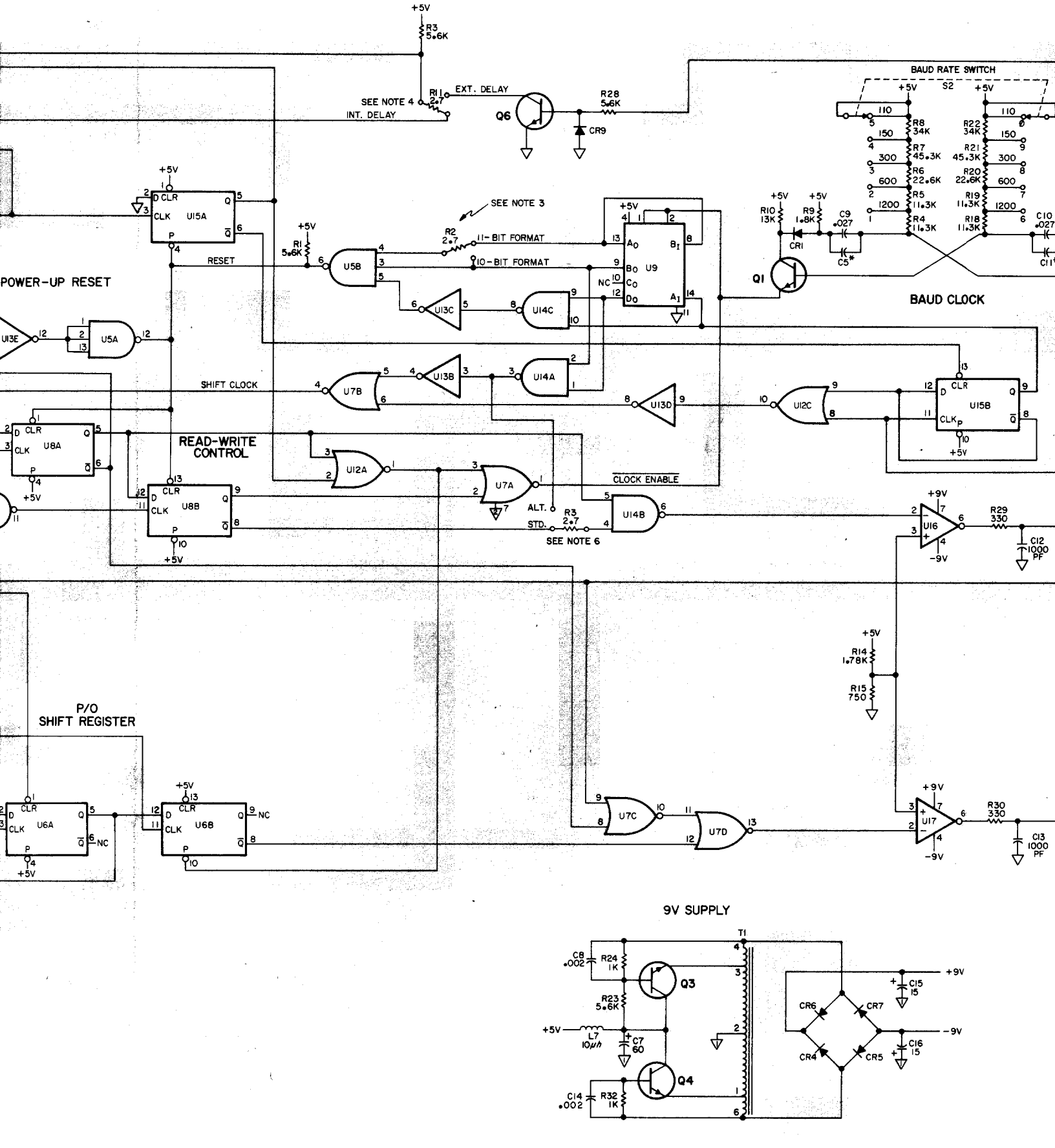
NOTE 3: The position of R2 determines whether 10-bit or 11-bit format is used and should match the terminal's I/O format.

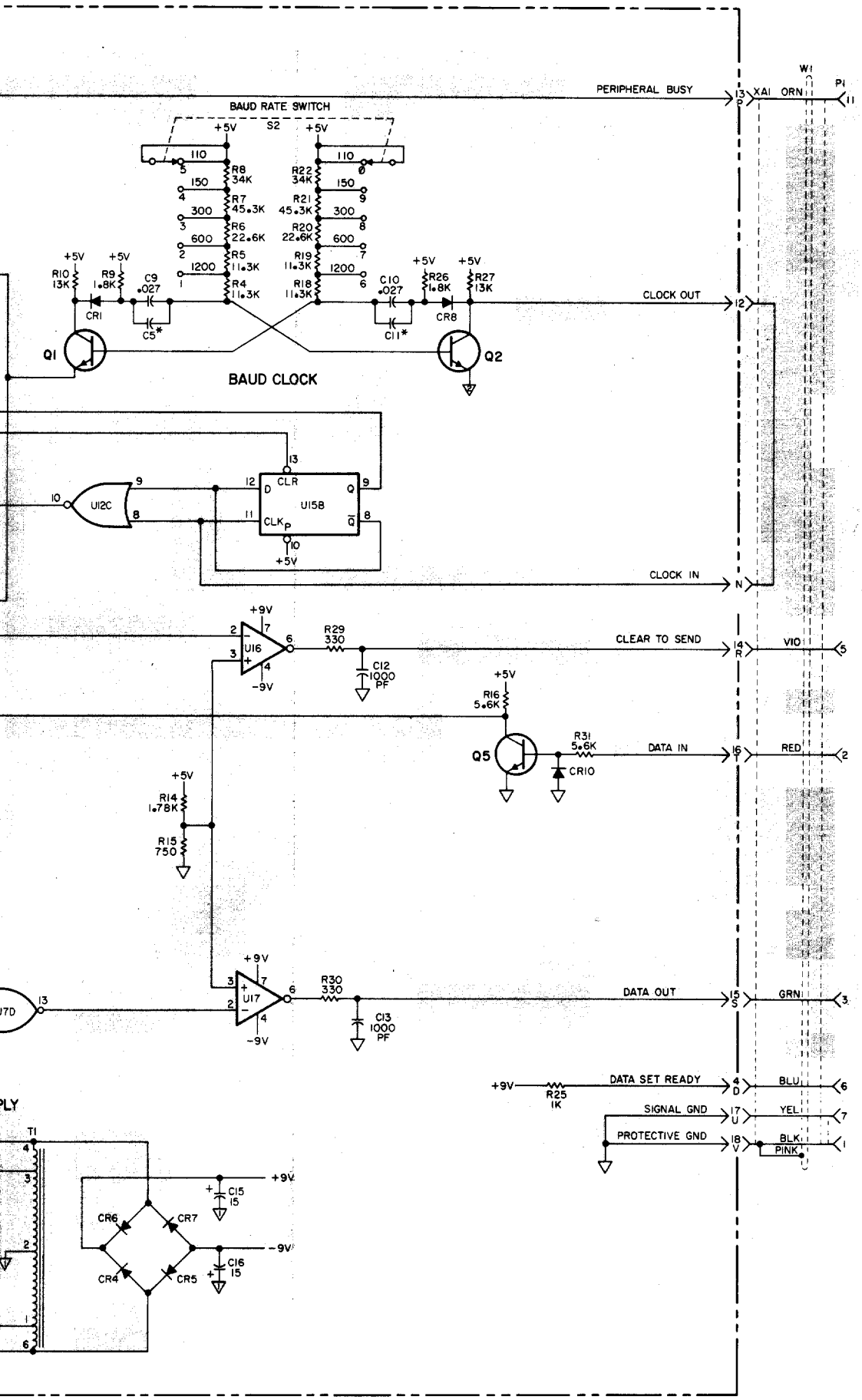
NOTE 4: The position of R11 determines whether internal delay or external delay is used when transmitting data (see page 1-4).

NOTE 5: The BAUD Clock rates can be changed by adjusting the values of C9 and C10. Increasing their values (together) lowers the clock frequency. The BAUD rate must be equal to the terminal's I/O rate.

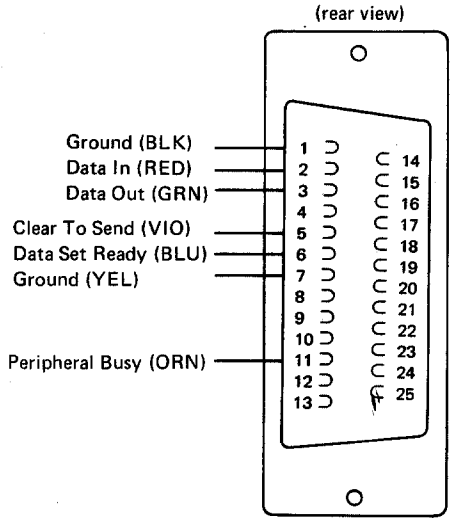
NOTE 6: The position of R3 determines operation of the Clear To Send signal during input operations. If R3 is set to the 'STD' position, the Clear To Send line remains high until the start bit is received. If R3 is set to the 'ALT' position, the Clear To Send line remains high until the first stop bit is received.


A1
SERIAL I/O INTERFACE ASSEMBLY 11205-66591 REV. B
CALCULATOR I/O CONNECTOR
SELECT CODE SWITCH SEE NOTE 2
CLOCK "A"
CLOCK "B"
POWER-UP RESET
RESET
SHIFT CLOCK
OUTPUT DELAY
READ-WRITE CONTROL
P/O SHIFT REGISTER
P/O SHIFT REGISTER
U11A DECODER
U10 ONE SHOT (200msec)
U1
U4
11205B-J-50494
REVISED
ORG


+5V
R3 5.6K
SEE NOTE 4
INT. DELAY
R11 2.7
EXT. DELAY
Q6
R28 5.6K
CR9
BAUD RATE SWITCH
S2
R8 34K
R7 45.3K
R6 22.6K
R5 11.3K
R4 11.3K
R22 34K
R21 45.3K
R20 22.6K
R19 11.3K
R18 11.3K
110
150
300
600
1200
R10 13K
R9 1.8K
C9 .027
C5*
CR1
Q1
C10 .027
C11*
BAUD CLOCK
U15A
POWER-UP RESET
RESET
R1 5.6K
U5B
SEE NOTE 3
R2 2.7
11-BIT FORMAT
10-BIT FORMAT
U9
U13C
U14C
U13E
U5A
SHIFT CLOCK
U7B
U13B
U14A
U13D
U12C
U15B
U8A
U8B
READ-WRITE CONTROL
U12A
U7A
CLOCK ENABLE
ALT.
STD.
R3 2.7
SEE NOTE 6
U14B
+9V
-9V
U16
R29 330
C12 1000 PF
R14 1.78K
R15 750
P/O SHIFT REGISTER
U6A
U6B
U7C
U7D
U17
R30 330
C13 1000 PF
9V SUPPLY
T1
C8 .002
R24 1K
Q3
R23 5.6K
L7 10μh
C7 60
Q4
C14 .002
R32 1K
CR6
CR7
CR4
CR5
C15 15
C16 15


BAUD RATE SWITCH
S2
+5V
110
150
300
600
1200
R8 34K
R7 45.3K
R6 22.6K
R5 11.3K
R4 11.3K
R22 34K
R21 45.3K
R20 22.6K
R19 11.3K
R18 11.3K
R10 13K
R9 1.8K
C9 .027
CR1
C5*
Q1
BAUD CLOCK
C10 .027
C11*
R26 1.8K
R27 13K
CR8
Q2
PERIPHERAL BUSY
CLOCK OUT
CLOCK IN
U12C
U15B
CLR
D
CLK
Q
+9V
-9V
U16
U17
R29 330
C12 1000 PF
R30 330
C13 1000 PF
CLEAR TO SEND
DATA OUT
R16 5.6K
R31 5.6K
Q5
CR10
DATA IN
R14 1.78K
R15 750
R25 1K
DATA SET READY
SIGNAL GND
PROTECTIVE GND
W1
XA1
ORN
P1
VIO
RED
GRN
BLU
YEL
BLK
PINK
T1
CR6
CR7
CR4
CR5
C15 15
C16 15

P1
(rear view)


Ground (BLK)
Data In (RED)
Data Out (GRN)
Clear To Send (VIO)
Data Set Ready (BLU)
Ground (YEL)
Peripheral Busy (ORN)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

APPENDIX A

EQUIVALENT ASCII FORMS

ASCII Char *	EQUIVALENT FORMS Binary	Octal	Dec ☆	Model 10 Key	Model 20 Key
@	01000000	100	64	↑ ROLL	GO TO
A	01000001	101	65	A	A
B	01000010	102	66	B	B
C	01000011	103	67	C	C
D	01000100	104	68	D	D
E	01000101	105	69	E	E
F	01000110	106	70	F	F
G	01000111	107	71	G	G
H	01001000	110	72	H	H
I	01001001	111	73	I	I
J	01001010	112	74	J	J
K	01001011	113	75	K	K
L	01001100	114	76	L	L
M	01001101	115	77	M	M
N	01001110	116	78	N	N
O	01001111	117	79	O	O
P	01010000	120	80	π	P
Q	01010001	121	81	b	Q
R	01010010	122	82	a	R
S	01010011	123	83	$y\rightarrow(\ )$	S
T	01010100	124	84	$x\rightarrow(\ )$	T
U	01010101	125	85	$1/x$	U
V	01010110	126	86	int x	V
W	01011000	127	87	IN-DIRECT	W
X	01011001	130	88	$y\overrightarrow{\leftarrow}(\ )$	X
Y	01011010	131	89	$x\leftarrow(\ )$	Y
Z	01011010	132	90	x^2	Z

ASCII Char *	EQUIVALENT FORMS Binary	Octal	Dec ☆	Model 10 Key ‡	Model 20 Key ‡
[	01011011	133	91	$\sqrt{x}$	3 PC2 †
/	01011100	134	92	LABEL	↵
]	01011101	135	93	CHG SIGN	4 PC2 †
↑	01011110	136	94	ENTER EXP	ENTER EXP
←	01011111	137	95	SUB RETURN	→
ACK	01111100	174	124	LABEL	↵
CTL	01111101	175	125	CHG SIGN	—
ESC	01111110	176	126	ENTER EXP	ENTER EXP
DEL	01111111	177	127	SUB RETURN	→
0	00110000	060	48	0	0
1	00110001	061	49	1	1
2	00110010	062	50	2	2
3	00110011	063	51	3	3
4	00110100	064	52	4	4
5	00110101	065	53	5	5
6	00110110	066	54	6	6
7	00110111	067	55	7	7
8	00111000	070	56	8	8
9	00111001	071	57	9	9
:	00111010	072	58	×	R( )
;	00111011	073	59	+	2 PC2 †
<	00111100	074	60	CLEAR x	≤
=	00111101	075	61	−	=
>	00111110	076	62	•	>
?	00111111	077	63	÷	

ASCII Char *	EQUIVALENT FORMS Binary	Octal	Dec ☆	Model 10 Key ‡	Model 20 Key ‡
NULL	00000000	000	0	CONTINUE	SPACE
SOM	00000001	001	1	IF FLAG	STOP
EOA	00000010	002	2	IF x<y	—
EOM	00000011	003	3	IF x=y	≠
EOT	00000100	004	4	2	$
WRU	00000101	005	5	GO TO	LOAD
RU	00000110	006	6	PAUSE	&
BELL	00000111	007	7	↓	'
FE_0	00001000	010	8	x⇄y	1 PC1 †
H_{TAB}	00001001	011	9	x⇄y	+
LF	00001010	012	10	CLEAR	*
V_{TAB}	00001011	013	11	CLEAR	2 PC1 †
FF	00001100	014	12	SET FLAG	,
CR	00001101	015	13	SET FLAG	—
DC_0	00010000	020	16	0	NORMAL
DC_1	00010001	021	17	IF FLAG	TRACE
DC_2	00010010	022	18	IF x<y	FIXED N
DC_3	00010011	023	19	IF x=y	FLOAT N
DC_4	00010100	024	20	IF x>y	4
ERR	00010101	025	21	GO TO	5
SYNC	00010110	026	22	PAUSE	6
LEM	00010111	027	23	↓	7
S_O	00011000	030	24	—	3 PC1 †
S_i	00011001	031	25	—	4 PC1 †

ASCII Char *	EQUIVALENT FORMS Binary	Octal	Dec ☆	Model 10 Key ‡	Model 20 Key
space	00100000	040	32	CONTINUE	SPACE
!	00100001	041	33	1	STOP
"	00100010	042	34	2	1 PC2 †
#	00100011	043	35	3	≠
$	00100100	044	36	4	$
%	00100101	045	37	5	%
&	00100110	046	38	6	&
(apost) '	00100111	047	39	7	'
(	00101000	050	40	8	(
)	00101001	051	41	9	)
*	00101010	052	42	×	*
+	00101011	053	43	+	+
(comma) ,	00101100	054	44	CLEAR x	,
-	00101101	055	45	—	—
.	00101110	056	46	.	.
/	00101111	057	47	÷	/

*The characters acceptable for data input are within a gray field.

☆Decimal numbers are used with PC II READ BYTE, WRITE BYTE, and Model 30 WRITE statements.

‡The keys colored light-brown correspond to the shifted output mode.

†These are the blank keys and are numbered from top to bottom as on the keyboard. The characters can be output with the indicated PC Block only.

APPENDIX B

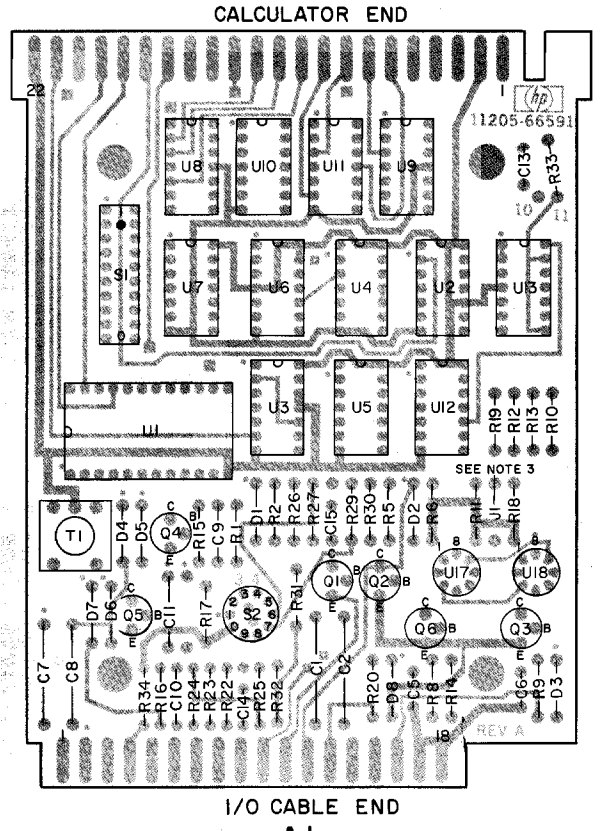
Manual Changes
for Revision A Circuit Boards

The following parts list, component locators, and circuit diagram apply to 11205A Interface circuit boards with 'REV A' designation. Those boards were delivered before August, 1973.

A Revision B circuit board can be used to replace a defective Revision A board. The reverse situation is not possible in all cases, however, since the Revision A board is not compatible with the 9830A Calculator. Otherwise, interfacing specifications and requirements are identical for Revision A and B boards.

REPLACEABLE PARTS LIST

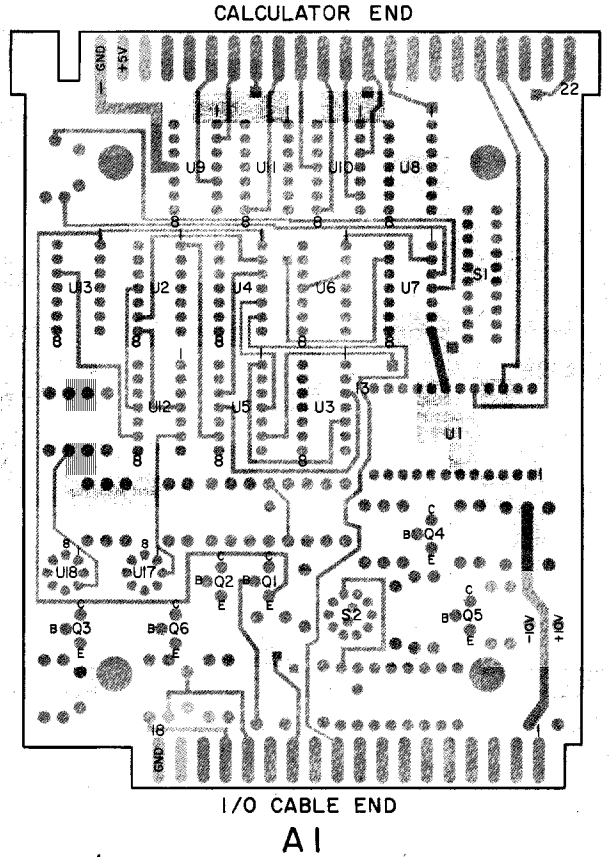
	REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION		
A1		11205-66591	1	PC Board Assembly, REV.A		
	C1, C2	0160-3165	2	C-F: .047µfd		
	C5, C6	0160-0938	2	C-F: 1000PF, 100V		
	C7, C8	0180-0116	2	C-F: 6.8µfd, 35V		
	C9, C10	0150-0023	2	C-F: .002µfd		
	C11	0180-0106	2	C-F: 60 µfd, 6V		
	C13,14,15	*	3	(Installed during calibration)		
	CR1-CR8	1901-0040	8	Diode: Si, .05A, 30V		
	IC1	1820-0702	1	IC: SL17303		
	IC2	1820-0596	2	IC: Dgtl, DM74L74N		
	IC3, IC4	1820-0584	2	IC: SN74L02		
	IC5	1820-0174	1	IC: SN7404N		
	IC6	1820-0596		IC: Dgtl, DM74L74N		
	IC7	1820-0907	1	IC: Dgtl, SN7412N		
	IC8, IC9	1820-0599	2	IC: Dgtl, SN74L95		
	IC10, IC11	1820-0269	2	IC: SN7403N		
	IC12	1820-0583	1	IC: SN74L00		
	IC13	1820-0601	1	IC: Dgtl, DN74L93N		
	IC17, IC18	1820-0203	2	IC: Op. Amp, 741C		
	Q1, Q2	1854-0071	2	XSTR: Si, NPN		
	Q3	1854-0354	2	XSTR: Si, NPN		
	Q4, Q5	1854-0556	2	XSTR: Si, NPN		
	Q6	1854-0354		XSTR: Si, NPN		
	R1, R6	0757-0290	2	R-F: 6190 OHM, 1%		
	R2, R5	0698-4427	2	R-F: 1650 OHM, 1%		
	R8	0684-3311	2	R-F: 330 OHM, 10%		
	R9 - R11	0684-5621	4	R-F: 5600 OHM, 10%		
	R12	0757-0278	1	R-F: 1780 OHM, 1%		
	R13	0757-0420	1	R-F: 750 OHM, 1%		
	R14	0684-3311		R-F: 330 OHM, 10%		
	R15, R16	0684-1021	3	R-F: 1000 OHM, 10%		
	R17	0684-5621		R-F: 5600 OHM, 10%		
	R18, R19	0684-2221	2	R-F: 2200 OHM, 10%		
	R21, R23	0757-0445	4	R-F: 13K, 1%		
	R24	0698-3159	2	R-F: 26.1K, 1%		
	R25	0698-4498	2	R-F: 53.6K, 1%		
	R26	0757-0124	2	R-F: 39.2K, 1%		
	R27, R29	0757-0445		R-F: 13K, 1%		
	R30	0698-3159		R-F: 26.1K, 1%		
	R31	0698-4498		R-F: 53.6K, 1%		
	R32	0757-0124		R-F: 39.2K, 1%		
	R33	0684-0271	1	R-F: 2.7 OHM, 10%		
	R34	0684-1021		R-F: 1000 OHM, 10%		
	S1	3101-1677	1	Switch: Program		
	S2	3100-3228	1	Switch: 2P5T		
	T1	9100-3403	1	Transformer, Inverter		
	W1	11205-61601	1	Cable Assembly with connectors		
		5040-5911	1	Interface Case,plastic		
		11205-04103	1	Interface Cover,metal		
		11205-90000	2	Manual,Installation and Service		



A1

hp Part No. 11205-66591 Rev. A

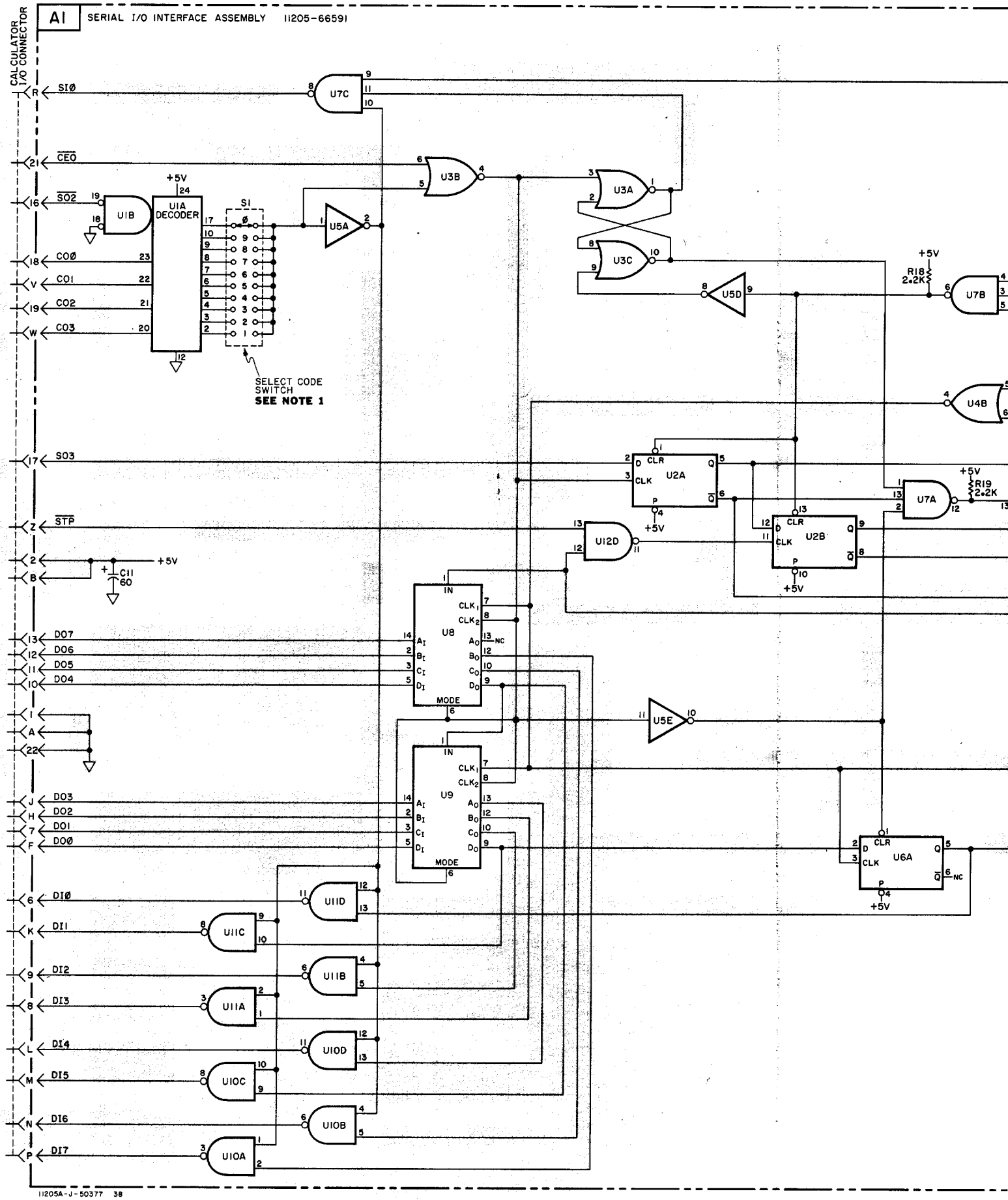
(Componet Side)



A1

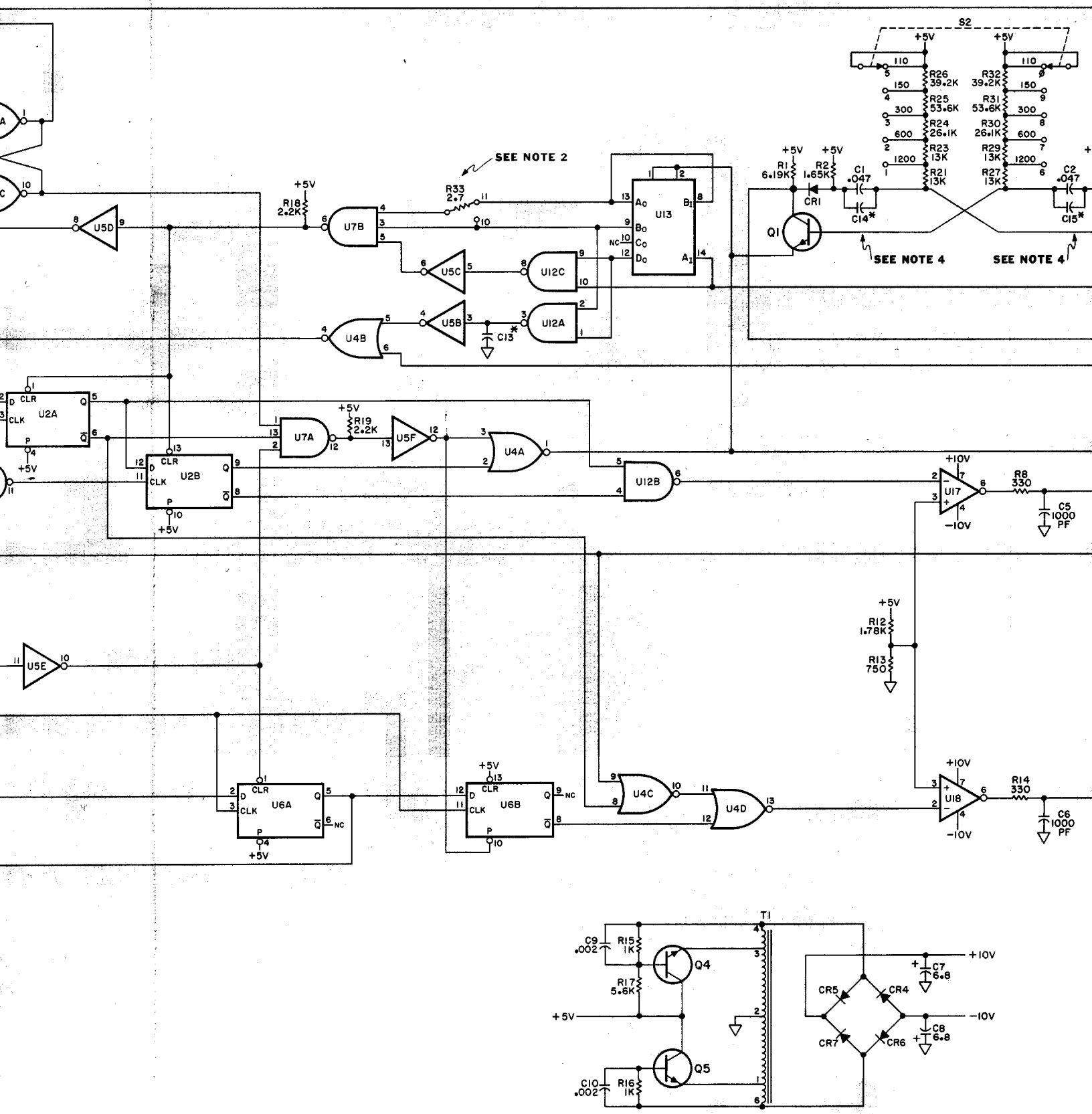
hp Part No. 11205-66591 Rev. A

(Circuit Side)



NOTE 1: The select code switch is set to select code 15 (position '0') . See Page 4 before resetting this switch.

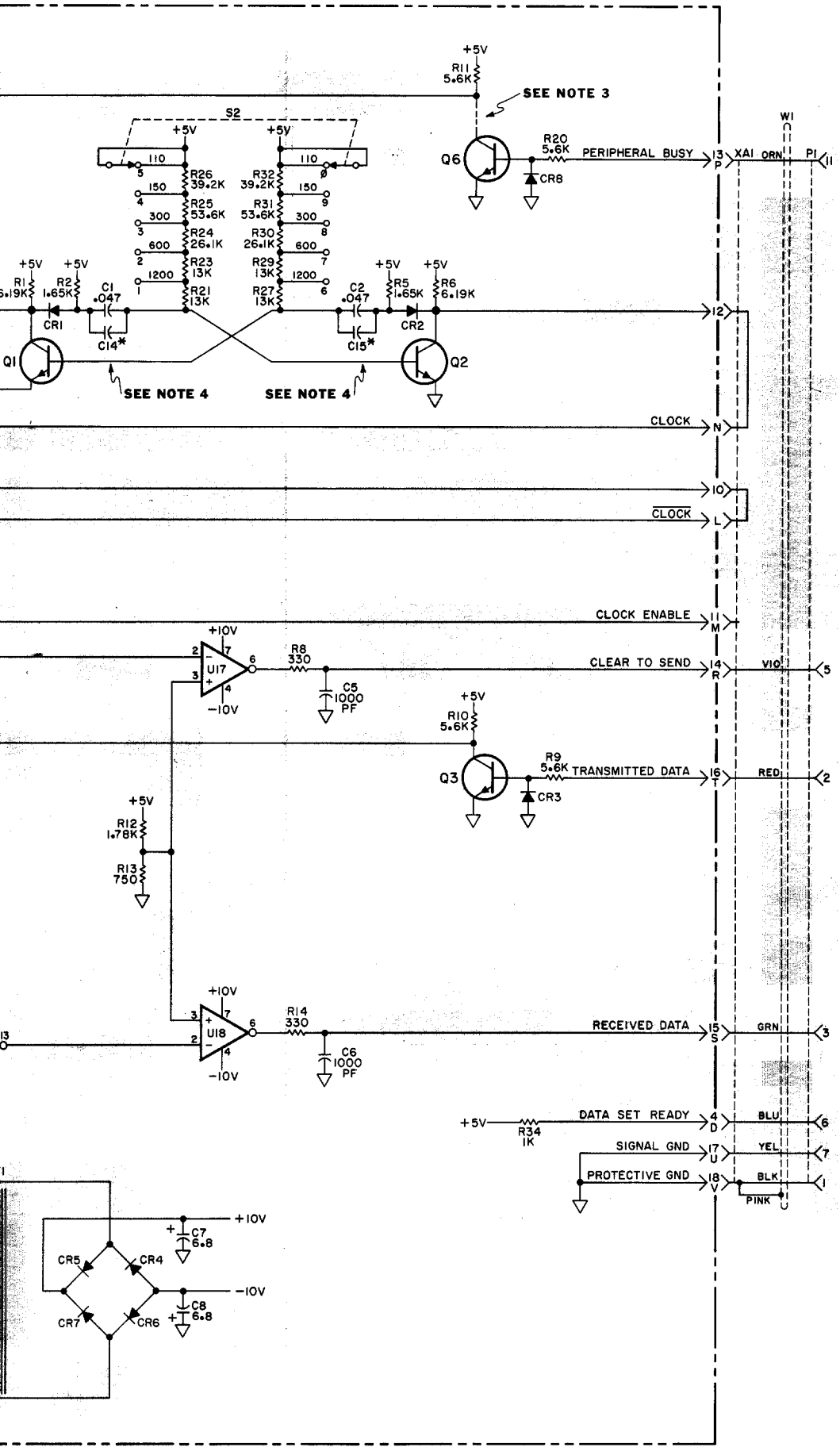
NOTE 2: the position of R33 determines whe format is set. See Page 4 before changing the NOTE 3: The Peripheral Busy line is enabled jumper wire here - see 'pin 11-Peripheral Busy

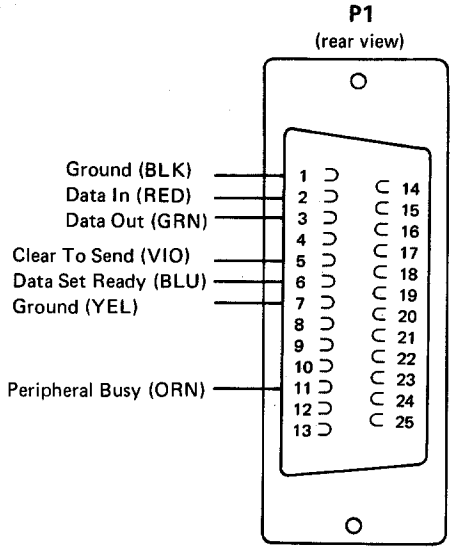


NOTE 2: the position of R33 determines whether 10 or 11- bit format is set. See Page 4 before changing the position of R33.

NOTE 3: The Peripheral Busy line is enabled by connecting a jumper wire here - see 'pin 11-Peripheral Busy line' on Page 3 .

NOTE 4: The BAUD clock frequencies can be changed b the values of C14 and C15 - increasing their values lower frequency, while decreasing their values raises the clock f The BAUD rate must match the I/O transfer rate of the





NOTE 4: The BAUD clock frequencies can be changed by altering the values of C14 and C15 - increasing their values lowers the clock frequency, while decreasing their values raises the clock frequency. The BAUD rate must match the I/O transfer rate of the terminal.

11205A CIRCUIT DIAGRAM (Revision A Boards)