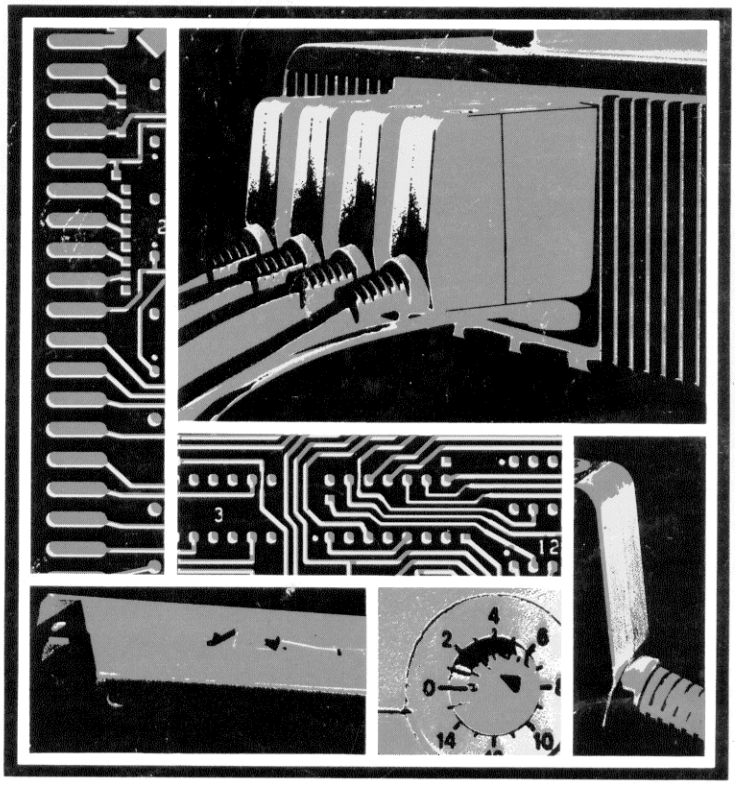
HP 98036A
Installation and Service



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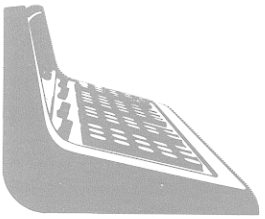
HP 98036A
Serial I/O Interface
Installation and Service Manual



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Printing History

New editions of this manual will incorporate all material updated since the previous edition. Update packages may be issued between editions and contain replacement and additional pages to be merged into the manual by the user. Each updated page will be indicated by a revision date at the bottom of the page. A vertical bar in the margin indicates the changes on each page. Note that pages which are rearranged due to changes on a previous page are not considered revised.

The manual printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates which are incorporated at reprint do not cause the date to change.) The manual part number changes when extensive technical changes are incorporated.

December 1979...First Edition
January 1981...Second Edition (adds Option 002).

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Table of Contents

Chapter 1

General Information

Manual Introduction

This manual describes the installation and operation of the HP 98036A Serial I/O Interface when used with an HP Desktop Computer and a data communications device. Theory of operation and troubleshooting chapters are also included to provide servicing information.

Complete background information about serial interfacing is provided by the Interfacing Concepts Manual for your Desktop Computer.

For those who are familiar with Hewlett-Packard interfaces and serial I/O, Chapters 2 and 4 provide sufficient hardware and programming information to enable you to "get on board" quickly.

Chapter Summaries

- Chapter 1 describes the 98036A interface, the interface specifications, and the cable options available.
- Chapter 2 explains how to set the hardware configuration switches and how to install the interface.
- Chapter 3 describes the various I/O registers that are contained on the interface card.
- Chapter 4 explains how to program the interface. Examples show how to read the status, set mode and control words, and transmit and receive data.
- Chapter 5 contains the theory of operation.
- Chapter 6 provides troubleshooting and repair information.
- Appendix A contains example programming applications.

98036A Description

The HP 98036A Serial I/O Interface allows the computer to communicate with serial **asynchronous** data communication devices. The 98036A is equipped with both RS-232C and 20ma current loop drivers and receivers for the data transmitter and receiver. Data can be transferred at bits rates of 75 to 9600 bits per second. The interface is capable of **asynchronous** communication. A universal receiver/transmitter integrated circuit (USART) is used to manipulate data and provide the basic hardware protocol for **asynchronous** operation. The I/O ROM must be installed in the computer in order to use the interface. The interface is available with two cable configurations to allow the computer to act as a data terminal or the digital portion of a modem.

Specifications

Power Requirements: (from the computer)	+5 Volts at 300ma typ. 400 max. ±12 Volts at 20ma typ. 40 max
Operating Temperature Range:	0°C to 45°C
Bit Rates:	9600, 4800, 2400, 1800, 1200, 600, 300, 150, 110, and 75 bits/second.
Mode of Operation:	**Asynchronous**
Data Buffer:	Transmitter-one character Receiver-one character
Dimensions:	Approximately 16.3x8.9x3.8cm (6.4x3.5x1.5 inches)
Net Weight:	4.16kg (1 lb. 14 oz)
Cable Length:	2 metres (6.5 ft.)

Cable Options

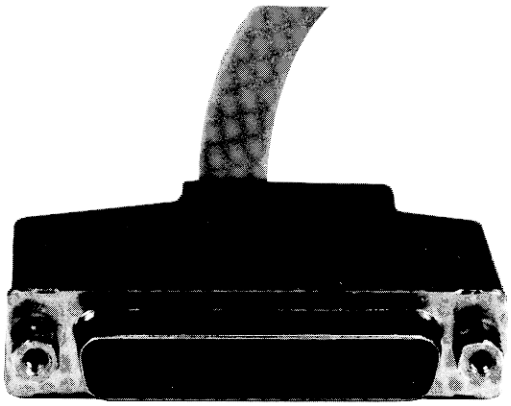
The 98036A interface is available in three cable configurations: standard, Option 001 and Option 002.

The interface can be ordered for specific Desktop Computers by specifying the appropriate ordering option. See the following table.

Cable Configuration	Ordering Option		
	System 25	System 35	System 45
Standard	Standard	335	445
Option 001	001	301	401
Option 002	Not Available	302	402

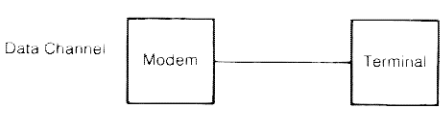
For example, to order a standard interface for a System 45, specify ordering Option 445.

The standard 98036A Interface cable is shipped with a 2 metre (6.5 ft.) cable terminated with a standard female EIA 25 pin connector. The standard interface is connected between the computer and a data terminal.

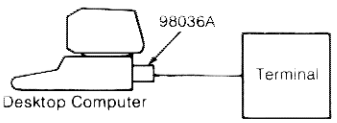


Standard Cable Connector

Using the standard interface cable, the computer takes the place of a modem or computer communicating with a terminal.

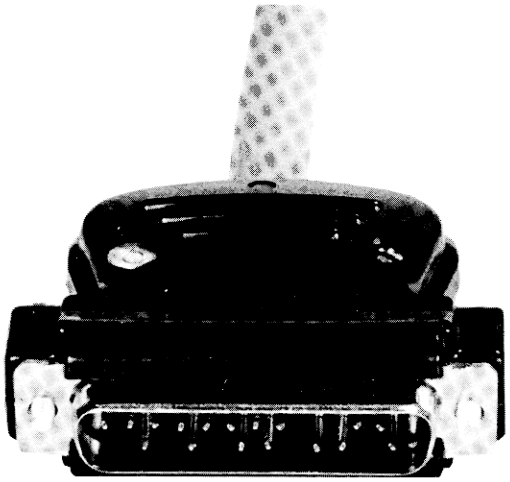


Using Normal Data Communications

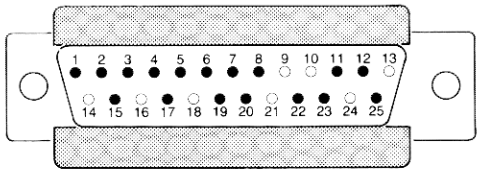


Using Desktop Computer/98036A(Standard)

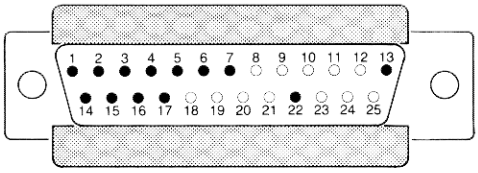
The 98036A Options 001 and 002 Interface cables are shipped with a 2 metre (6.5 ft.) cable terminated with a standard male EIA 25 pin connector. The following drawings show the differences between the Option 001 and 002 cables.



Cable Connector

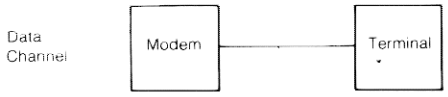


Option 001

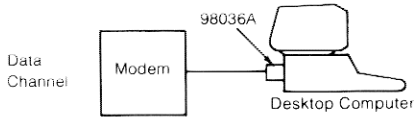


Option 002

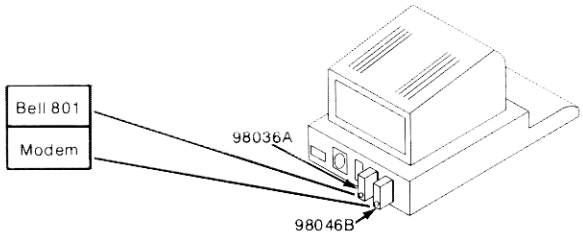
Using the Option 001 interface cable, the computer acts as a data terminal connected to a modem.



Using Normal Data Communications



Using Desktop Computer/98036A (Option 001)



Using Desktop Computer/98036 (Option 002)

NOTE

The Option 002 interface cable is used ONLY with the optional Distributed System Software for System 35/45 desktop computers. No register control/access should be attempted for Option 002 interfaces. See your software manual for Option 002 interface programming details.

Here is a list of the signal lines and the corresponding connector pin numbers used in the standard and option 001 cables.

Table 1. Cable Signals

DCE (Standard)		RS232-C			DTE (Option 001)	
Register Access	Standard Pin	Direction ↔	Pin #	Signal Name	Option 001 Pin #	Register Access
n.a.	1	↔	1	Protective Ground	1	n.a.
read	3	←	2	Transmitted Data	2	write
write	2	→	3	Received Data	3	read
R4E, bit 7	6	←	4	Request to Send	4	R4D, bit 5
R4D, bit 5	4	→	5	Clear to Send	5	(Note 1)
R4D, bit 1	17	→	6	Data Set Ready	6	R4E, bit 7
n.a.	7	→	7	Logic Ground	7	n.a.
R6 OUT, bit 0	16	→	8	Carrier Detect	8	R6 IN, bit 0
n.a.	—		9	(Reserved for test)	—	n.a.
n.a.	—		10	(Reserved for test)	—	n.a.
n.a.	—	↔	11	Data Rate Select (U.K.) (Note 2)	11	R6 OUT, bit 2
R6 OUT, bit 1	13	→	12	Second Carrier Detect	12	R6 IN, bit 2
n.a.	—	→	13	Second CTS	—	n.a.
n.a.	—	←	14	Second TXD	—	n.a.
n.a.	—	→	15	Transmitter Clock	15	(Note 3)
n.a.	—	→	16	Second RXD	—	n.a.
n.a.	—	→	17	Receiver Clock	14	(Note 3)
n.a.	—		18	—	—	n.a.
R6 IN, bit 0	8	←	19	Second RTS	16	R6 OUT, bit 0
(Notes 1,4)	5	←	20	Data Terminal Ready	17	R4D, bit 1
R6 OUT, bit 2	11	→	21	Signal Quality Detect	—	n.a.
R6 OUT, bit 3	10	→	22	Ring Indicator	9	R6 IN, bit 1
R6 IN, bit 1	9	←	23	Data Rate Select	13	R6 OUT, bit 1
n.a.	—	←	24	Transmit clock (term)	—	n.a.
n.a.	—		25	—	10	n.a.

Note 1: this line cannot be read
Note 2: this line unassigned by RS-232-C
Note 3: switch selectable on 98036A
Note 4: can be set high by switch on 98036A

Chapter 2

Installation

Introduction

Before installing the interface in your Desktop Computer it will be necessary to configure the interface for your particular application. Two methods are provided for interface configuration: hardware (switches) and software (program control). The hardware configuration switches determine the preset state of the interface when power is first applied or the computer is reset. Software configuration enables you to change the state of the mode and control words from within a program. The mode and control words remain in this configuration until either a new program statement changes them, the computer is reset, or power is switched off.

Hardware Configuration (Exterior Access)

The following hardware configuration switches cannot be changed from within a program but interface disassembly is not required for access to these switches.

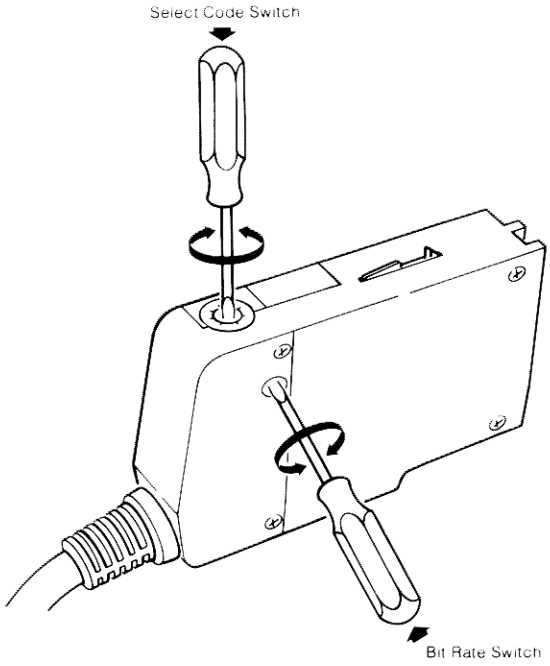
Bit Rate (or Baud) Switch

The bit rate can be changed through the access hole in the side of the interface (see the next drawing). Set the bit rate switch to correspond to the bit rate of the data communications device connected to the interface. The following table shows the bit rates provided and the corresponding switch positions. Rotate the switch to the desired position with a small screwdriver.

Switch Position	Bit Rate	
1	9600	Use 1/16 Bit Resolution
2	4800	
3	2400	Use 1/64 Bit Resolution
4	1800	
5	1200	
6	600	
7	300	
8	150	
9	110	
0	75	

Select Code Switch

The interface select code switch is changed through the access hole provided in the top of the interface. The standard and Option 002 interfaces are preset at the factory to a select code of 10. The Option 001 interface is preset at the factory to a select code of 11. The select code should be checked for the proper setting as required by your system. Each interface must be set to a different select code. The Desktop Computer reserves certain select codes for its own internal peripherals. The Owners Manual supplied with your Desktop Computer lists the select code settings that may be used. To change the select code, use a small screwdriver and turn the switch to the desired setting (see the following drawing).



Hardware Configuration (Interior Access)

The following hardware configuration switches set the default status of the USART mode word. Control of the following is provided by the USART mode word:

- Number of stop bits.
- Parity type.
- Enable-Disable parity.
- Character length.
- Bit Resolution.

NOTE

Although you can configure the USART mode word with register I/O program statements, the USART mode word is set to the default condition whenever power is applied, the computer is reset, or an interface reset is executed.

The interface MUST be disassembled in order to gain access to the USART mode word configuration switches. The following switches also require interface disassembly for access:

- I/O Mode Switch
- Driver Power Switch
- Receiver Clock Switch
- Transmitter Clock Switch
- Clear To Send Line Switch

The following table shows the factory settings for all interface configuration switches.

Interface Configuration Switches	Factory Setting	Can be changed from software	Disassembly required to change setting
Select Code			
Standard Cable	10	No	No
Option 001 Cable	11	No	No
Option 002	10	No	No
Bit Rate	300	No	No
I/O mode Switch	RS-232	No	Yes
Driver Power Switch	RS-232	No	Yes
Receiver Clock Switch	Internal	No	Yes
Transmitter Clock Switch	Internal	No	Yes
Clear to Send Line Switch			
Standard	Always High	No	Yes
Option 001	Always High	No	Yes
Option 002	Device Controlled	No	Yes
Stop Bits	2	Yes	Yes(default)
Parity	Disabled	Yes	Yes(default)
Character Length	8	Yes	Yes(default)
Bit Resolution	1/64	Yes	Yes(default)

Instructions for setting these switches and the USART mode switches are provided following the next section.

Interface Disassembly

This section describes how to disassemble the interface. To disassemble the interface, use the procedure outlined below and refer to Figure 1.

- Remove the four screws that hold the rear housing to the front housing.
- Pull the rear housing off the front housing slightly, disconnect the cable connector from the PC assembly and remove the rear housing.
- Remove the four remaining screws in the front housing and separate the front housing cases.
- Carefully separate the printed circuit assemblies.
- See Figure 2 for the various switch locations.
- After setting the switches, reverse this procedure to assemble the interface. Be sure that the pins on the A2 assembly are properly seated in the connectors on the A1 assembly.

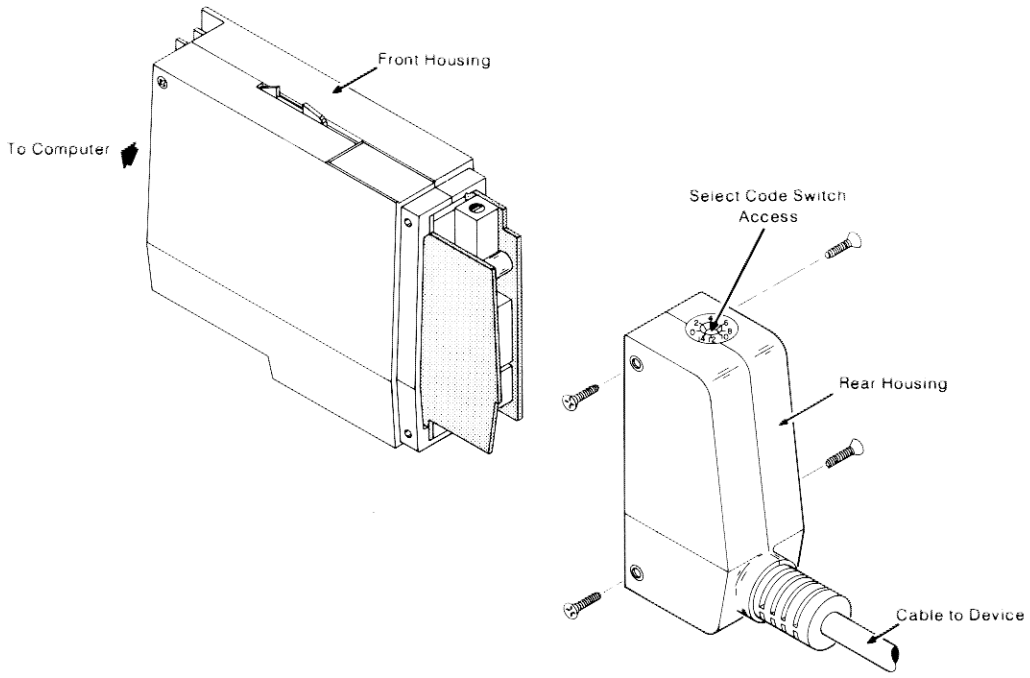


Figure 1. Interface Disassembly

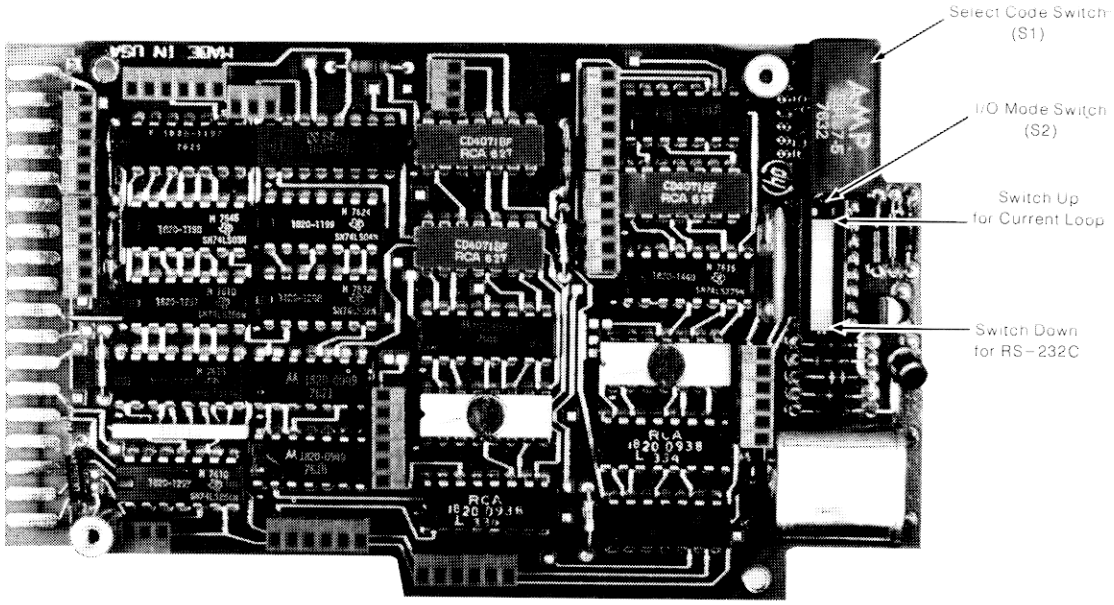


Figure 2. Interface Configuration Switches

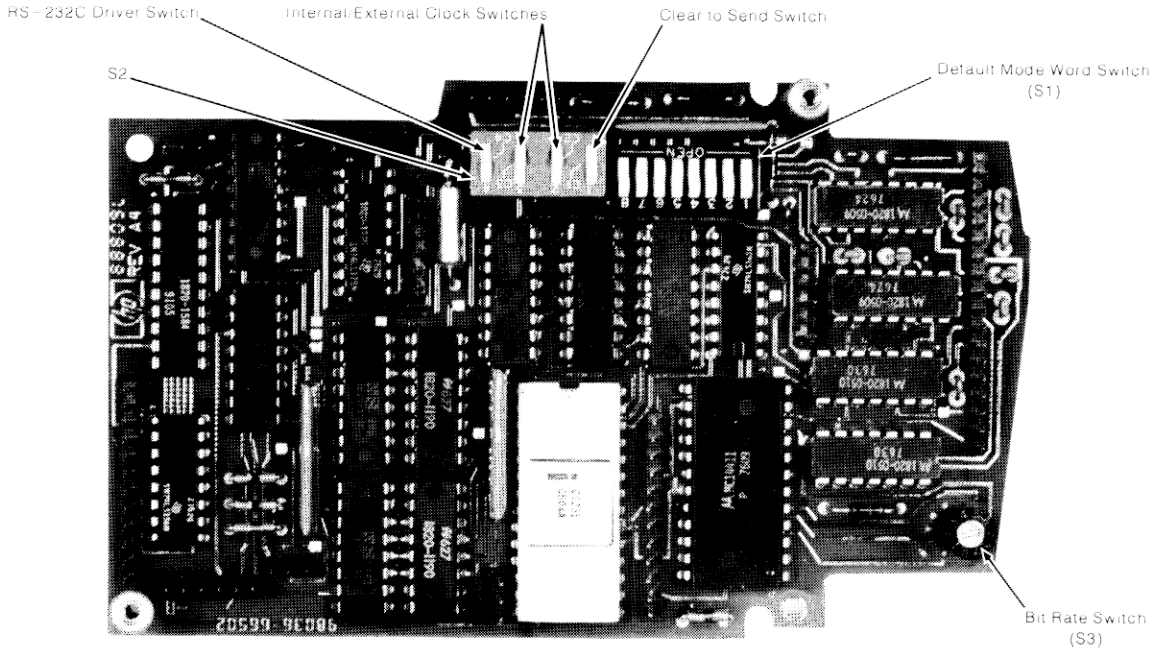


Figure 2.(cont.)

Setting The Switches

This section describes how to set the interface configuration switches for your particular requirements.

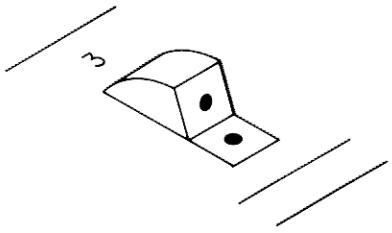
The following questions will help you determine how the interface switches should be set.

- What is the number of bits per character?
- Will parity be used?
- Even or odd parity?
- How many stop bits will be used?
- What bit resolution will be used?
- Will the operation be RS-232C or current loop?
- Will the internal clock be used for the transmitter and receiver clock?
- Does your data communications device provide the clear to send line (option 001 cable)?
- Does your data communications device provide the data terminal ready line (standard cable)?

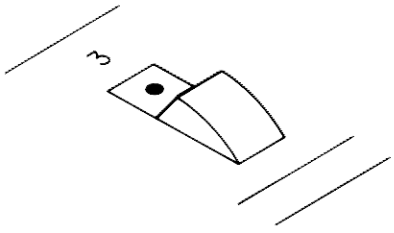
Mode Word Switches

The mode word switches (see figure 2) determine the default mode word used by the interface. The mode word determines the mode of interface operation. The default mode word is used when power is applied to the interface or when the interface or computer is reset. The default mode word can be overridden by subsequent mode words from the computer. Here is a description of each mode word bit position.

Any switch set to the open position sets the switch to a logical 1 (high). Any switch set to the opposite position sets the switch to a logical 0 (low).



1 = open



0 = closed

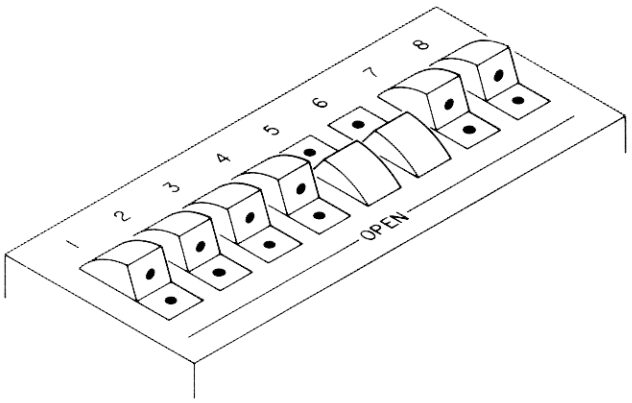
Bits 7 and 6 — Determine the number of stop bits used.

Bit 5 — Determines whether odd or even parity is to be used (when parity is enabled).

Bit 4 — Enables or disables parity.

Bits 3 and 2 — Indicate how many bits per character (character length).

Bits 1 and 0 — Determine the bit resolution. Characters can be transferred at either the rate of the bit rate clock, or 1/16 the rate of the bit rate clock, or 1/64 the rate of the bit rate clock. The 1/64 position is recommended for increased immunity to signal distortion.



NOTE

Do not use the 1/64 bit resolution setting when the bit rate is set to 4800 or 9600 bits per second. Use the 1/16 bit resolution.

NOTE

Setting bits 1 and 0 both to zeros will result in erroneous interface operation. Do not operate the interface with bits 1 and 0 of the mode word both set to zero.

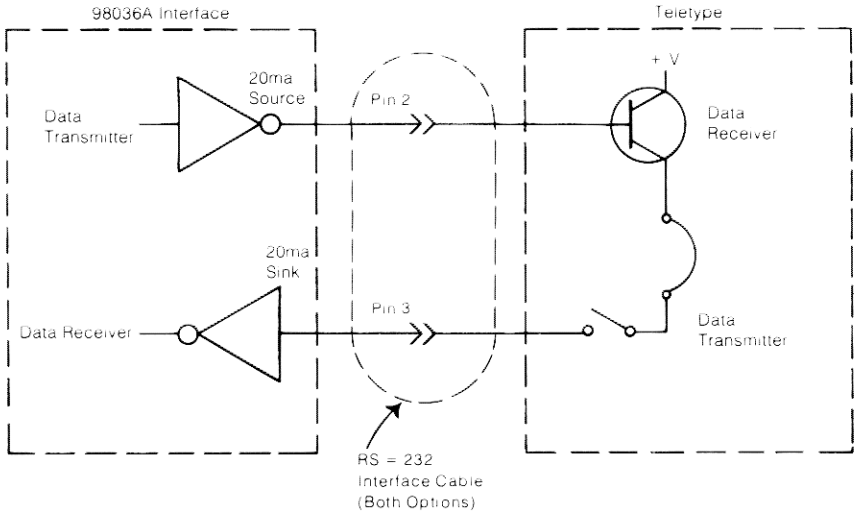
Input/Output Mode Switch

Set the I/O mode switch (See Figure 2) for either RS-232C or 20ma current loop operation depending on the device to be connected to the interface.

The RS-232C position is used when the interface is to be connected to a RS-232C compatible data terminal or modem.

The 20ma current loop position is used when the interface is to be connected to some teletype terminals. Only the transmit data and receive data lines are switched in current loop operation. The RS-232C control signals are not available in the current loop mode.

The following diagram shows a typical current loop connection.



RS-232C Driver Switch

The RS-232C driver switch MUST be set to the same position as the I/O mode switch. If the I/O mode switch is set for RS-232C operation, then the RS-232C driver switch MUST be set to the RS-232C position. If the I/O mode switch is set for current loop operation, then the RS-232C driver switch MUST be set to the current loop position.

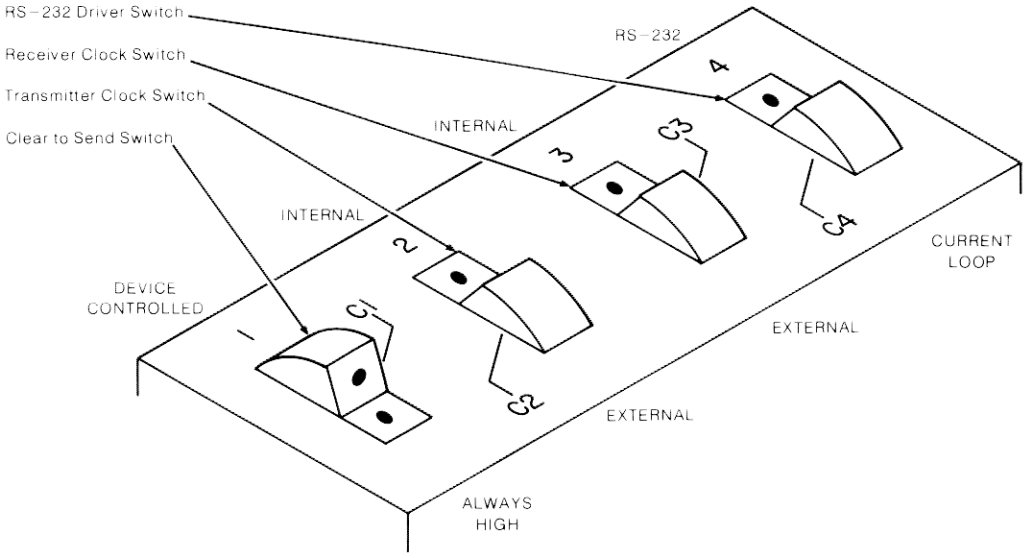
Internal/External Clock Switches

External transmit and receive clocks may be used instead of the internal bit rate clock. This feature is not usually used for asynchronous operation. The external clock should have a 50% duty cycle, and be sure that the interface bit resolution is the same as the external clock resolution.

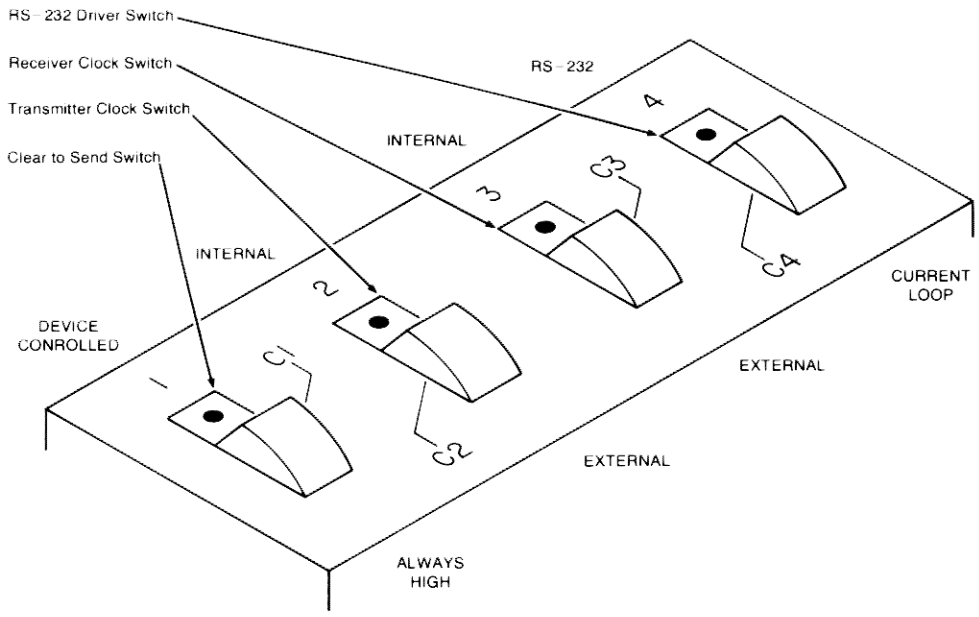
When either the transmit or receive clock switch is set to the internal position, the internal bit rate clock is used. When either the transmit or receive clock switch is in the external position, an appropriate external clock must be input to the interface. See Table 1 for the cable signal line numbers.

Clear to Send Switch

If the device connected to the interface does not provide the clear to send signal (data terminal ready line), set the clear to send switch to the 'always high' position. If the device does provide the clear to send signal, set the switch to the 'device controlled' position.



Factory Preset Switch Positions for Standard and Option 001



Factory Preset Switch Positions for Option 002

Interface Installation

After the interface configuration switches have been set, assemble the interface housing by reversing the disassembly procedure. Be sure that the pins on the A2 assembly are properly seated in the connectors on the A1 assembly. With the computer switched off, install the interface into any one of the I/O slots on the back of the computer. Connect the other end of the interface cable to an applicable data communications device (e.g., data terminal, modem).

Chapter 3

The Interface Registers

Introduction

This chapter describes the contents of the various 98036A interface registers. Access to these registers is described in Chapter 4. The 98036A interface is controlled by I/O ROM statements. When writing to and reading from the interface, internal interface registers (R4, R5, and R6) are written into, and read from, to control and monitor the interface operation. All registers are 8-bits long. Each register bit enables or disables an interface function or operation. In the following description of the registers, notice that some of the R4 and R6 bit definitions are different depending on whether the standard or the option 001 cable is used. Option 002 bit definitions are not shown.

Bit Position Values

Each 8-bit register (R4, R5, or R6) has a decimal value assigned to each bit. To set a bit in a register, you add the decimal value for that bit to your register I/O statement value. For example, to set bit 4 to a 1, the value specified is decimal 16 (see the following drawing).

Bit Position	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decimal Value	128	64	32	16	8	4	2	1

To set bits 5, 4, and 1, add the values of those bits and specify the result (i.e., 32 + 16 + 2 = 50).

In this manner, any bit or combination of bits can be set in the R4, R5, or R6 registers.

When writing into a register, all the register bits are accessed. Thus when changing a bit in a register, the entire register word must be sent. For example. setting only bit 3 of a register will clear all the other bits of that register. Always send the sum total value of a register when setting or changing a register.

R4 Registers

There are two R4 registers (R4OUT and R4IN). All communication between the computer and the USART passes through either R4OUT or R4IN. Transmit data, the USART mode word, and the USART control word are sent through the R4OUT register while received data and the USART status word are entered through the R4IN register. With this in mind, the R4 registers can be thought of as five distinct pseudo-registers (R4A through R4E). Here are the functions provided by the R4 registers:

Function	Register Used	Pseudo Register
Data Output	R4OUT	R4A
Data Input	R4IN	R4B
USART Mode Word	R4OUT	R4C
USART Control Word	R4OUT	R4D
USART Status Word	R4IN	R4E

Transmit Data Register (R4A)

Each character sent from the computer enters this register before it is sent serially to the data communications device. A register I/O operation is used to output characters from the computer to this register through R4OUT. All 8-bits of the transmit data register are used for the data character.

Received Data Register (R4B)

Serial data received from a data communications device is assembled into an 8-bit character before it is input by the computer. A register I/O operation from the computer is used to input a character from this register through R4IN. All 8-bits of the received data register are used for the data character.

NOTE

The USART mode and control words allow configuration of the 98036A via program control. These words are set to the default conditions when power is applied or the computer is reset. They can be changed under program control.

The USART Mode Word (R4C)

The mode word determines the mode of operation of the interface. A mode word is sent to the interface using register I/O statements from the computer. A mode word from the computer overrides the default mode word that was set (from the default mode word switches) during an interface reset. Here is a description of the USART mode word bit positions.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Number of Stop Bits 00=not valid 01=1 bit 10=1.5 bits 11=2 bits		Parity Type 0=Odd 1=Even	Parity Enable 0=Disable 1=Enable	Character Length 00=5 bits 01=6 bits 10=7 bits 11=8 bits		Bit Rate Factor 00=not used 01=1×bit rate clock 10=1/16×bit rate clock 11=1/64×bit rate clock	
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bits 7 and 6 — Determine the number of stop bits used.

Bit 5 — Determines whether odd or even parity is to be used (if parity is enabled).

Bit 4 — Enables or disables parity.

Bits 3 and 2 — Indicates the number of bits per character (character length).

Bits 1 and 0 — Determine the rate at which characters will be transferred. Characters can be transferred at either the rate of the bit rate clock, or 1/16 the rate of the bit rate clock, or 1/64 the rate of the bit rate clock. The 1/64 position is recommended for increased immunity to signal distortion.

NOTE

Do not use the 1/64 bit resolution setting when the bit rate is set to 4800 or 9600 bits per second. Use the 1/16 bit resolution.

NOTE

Setting bits 1 and 0 both to zeros will result in erroneous interface operation. Do not operate the interface with bits 1 and 0 of the mode word both set to 0.

The USART Control Word (R4D)

The USART is the integrated circuit in the interface that transmits and receives data in the proper format. The USART control word is accessed when bit 0 of the R5OUT register is a one. The USART control word is output from the computer with register I/O statements. Here is a description of the USART control word bit positions.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 0	USART Reset	Clear To Send Pin 5(Standard) / Request To Send Pin 4 (Option 001)	Reset Status Bits of USART Status Word	Send Break Character	Enable Data Receiver	Data Set Ready Pin 6(Standard) Data Terminal Ready Pin 20 (Option 001)	Enable Data Transmitter
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bit 7 — Bit 7 is not used and must always be a 0.

Bit 6 — Is used to reset the USART. When bit 6 is a 1, the USART is forced into an idle mode. The next byte sent to the interface will be accepted as a USART mode word.

Bit 5 — This is a programmable RS-232C signal. In the case of the standard cable, the signal is sent to the device on the Clear To Send line (pin 5). In the case of the option 001 cable, the signal is sent to the device on the Request To Send line (pin 4).

Bit 4 — Resets status bits 3, 4, and 5 of the USART status word to 0.

Bit 3 — Enables the USART to output a "break" to the data communications device. This causes a continuous space to be output. The "break" signal is not automatically terminated. Your software must reset the "break" signal.

Bit 2 — When this bit is a 1, it allows the interface to receive characters for transfer to the computer.

Bit 1 — For the standard cable, when bit 1 is a 1, a Data Set Ready signal is sent to the data terminal of pin 6 of the terminal connector. For the option 001 cable, when bit 1 is a 1, a Data Terminal Ready signal is sent to the modem on pin 20 of the modem connector.

Bit 0 — The USART transmitter is enabled when this bit is a 1.

NOTE

The power-up default control word is 5. Bits 0 and 2 are set.

The USART Status Word (R4E)

The status word can be accessed when bit 0 of R5OUT is a 1. A read binary statement from the computer is used to input the status word to the computer. Here is a description of the USART status word bit positions.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Request To Send Pin 4(Standard) Data Set Ready Pin 6 (Option 001)	Always 0	Framing Error	Overrun Error	Parity Error	Transmitter Empty	Receiver Ready	Transmitter Ready
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bit 7 — Using the standard cable, bit 7 indicates the status of the Request To Send line, pin 4 of the terminal connector. Using the option 001 cable, bit 7 indicates the status of the Data Set Ready line, pin 6 of the modem connector.

Bit 6 — Not used, always 0.

Bit 5 — This bit is a 1 when the received data did not contain the proper number of stop bits or when a break has been received.

Bit 4 — This bit is a 1 when data is received before the data receiver buffer is empty (overrun error).

Bit 3 — This bit is a 1 when a parity error occurs.

Bit 2 — This bit is a 1 when the USART's data transmitter buffer is empty.

Bit 1 — This bit is a 1 when the USART's data receiver is ready with a received character.

Bit 0 — This bit is a 1 when the USART's data transmitter buffer is ready to transmit data.

R5 Registers

There are two R5 registers. R5OUT holds the interface control word. The interface control word is sent to the R5OUT register using register I/O statements from the computer.

R5IN holds the interface status word. The interface status word is input by the computer from the R5IN register.

Here is a description of the R5OUT and R5IN bit positions.

R5OUT Register

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interface Interrupt Enable	———	Programmed Interface Reset	———	———	Interrupt Control 2 Receiver Control	Interrupt Control 1 Transmitter Control	R4 Control 0 = Data IN OUT 1 = Control Status
BIT VALUE = 128	BIT VALUE = 64	BIT VALUE = 32	BIT VALUE = 16	BIT VALUE = 8	BIT VALUE = 4	BIT VALUE = 2	BIT VALUE = 1

Bit 7 — When bit 7 is a 1, the interface is enabled to interrupt the computer's operation. Either bit 1 or bit 2 should be a 1 when bit 7 is a 1.

Bit 6 — Not used.

Bit 5 — When bit 5 is set to a 1, the interface is reset to the power up default condition. The power up default conditions are:

1. The default mode word will be used.
2. The USART control word is set to 5.
3. All other registers are set to 0.

Bit 5 is reset during the interface reset.

Bits 4 and 3 — Not used.

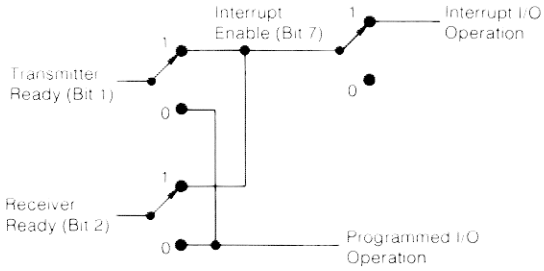
Bit 2 — Enables the interface's receiver for interrupt operation. When bit 2 is a 1 and the receiver is ready, an interrupt I/O operation will be performed (if bit 7 is also set). Bit 2 must be a 0 for normal programmed input operation.

Bit 1 — Enables the transmitter for interrupt operation. When bit 1 is a 1 and the transmitter is ready, an interrupt I/O operation will be performed (if bit 7 is also set). Bit 1 must be a 0 for normal programmed output operation.

Bit 0 — Determines whether the next transfer to or from the computer will be a data character or a control or status word. When bit 0 is a 1, access to the USART mode, status, and control words is enabled. With this access established, control words can be sent or changed and the USART status can be read. When bit 0 is a 0, data can be received or transmitted depending on how the USART control word was set.

NOTE

Bit 1 and bit 2 of R5OUT must be cleared for non-interrupt I/O operation.



R5IN Register

Most Significant Bit — Least Significant Bit

BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Peripheral Status 1	Interface Interrupt Enable Status	0	Interface I.D. 0 Always 0	Interface I.D. 1 Always 1	0	0	Control Status 2 Receiver Mode	Control Status 1 Transmitter Mode
BIT VALUE=256	BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bit 8 — Is the interface status bit. This bit is always 1 when the interface is installed and operational in the computer.

Bit 7 — Is a 1 when the interface interrupt is enabled (bit 7 of R5OUT).

Bit 6 — Not used, always 0.

Bit 5 and 4 — Identify the interface as a serial interface. Bit 5 is always 0 and bit 4 is always 1.

Bits 3 and 2 — Not used, always 0.

Bit 1 — Is a 1 when the receiver interrupt control is enabled (bit 2 of R5OUT).

Bit 0 — Is a 1 when the transmitter interrupt control is enabled (bit 1 of R5OUT).

R6 Registers

There are two R6 registers. The R6 registers are accessed by interface read and write operations.

R6OUT is controlled by the computer and is used to send control information to the data communications device. the contents of R6OUT are changed by a register I/O operation to the interface. The control information is then sent to the data communications device.

R6IN monitors the RS-232 status lines from the data communications device. The contents of the register are input to the computer by a register I/O operation.

Here is a description of the R6OUT and R6IN bit positions for both the standard and option 001 cables. Remember, when using the standard cable, the Desktop Computer/98036A Interface acts like a modem in communicating with a terminal and when using the option 001 cable, the Desktop Computer/98036A Interface acts like a terminal connected to a modem.

R6OUT Register (standard cable)

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
———	———	———	Half/Full Speed Control (Interface)	Ring Indicator Pin 22	Signal Quality Detect Pin 21	Secondary Carrier Detect Pin 12	Data Carrier Detect Pin 8
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bits 7 thru 5 — Not used.

Bit 4 — This bit is used to signal the interface that either half of full speed data transfer is being done (see R6IN, bit 1). When bit 4 is a 0, normal bit rate clock speed is being used. When bit 4 is a 1, data transfer is half the switch selected bit rate clock speed. Bit 4 information is used internally by the interface.

Bit 3 — Normally indicates a ringing signal to the data terminal on pin 22 of the terminal connector when bit 3 is a 1. Since no ringing signal is involved in a standard cable application, this bit is not normally used, however it is available.

Bit 2 — Normally is used to indicate to the data terminal whether or not there is a high probability of an error in the data received by the modem. If bit 2 is a 1, the received data is probably in error. This signal is sent to the terminal on pin 21 of the terminal connector. Since no data channel is involved in a standard cable application, this bit is not normally used however it is available.

Bit 1 — Normally indicates to the data terminal that the secondary channel carrier is being sent, when bit 1 is a 1. This signal is sent to the data terminal on pin 12 of the terminal connector. The secondary channel in a standard cable application is a pseudo-channel since no carrier is involved.

Bit 0 — Normally indicates to the data terminal that the primary channel carrier is being received, when bit 0 is a 1. This signal is sent to the data terminal on pin 8 of the terminal connector. The primary channel in a standard cable application is a pseudo-channel since no carrier is involved.

R6IN Register (standard cable)

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 1	Always 1	Always 1	Always 1	Always 1	Always 0	Data Signal Rate Select Pin 23	Secondary Request To Send Pin 19
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bits 7 thru 2 — Not used.

Bit 1 — This signal is sent to the interface from the data terminal on pin 23 of the terminal connector. This signal is used when the terminal has two data signalling rates or two ranges of data signalling rates. When bit 1 is a 1, the higher data signalling rate or range of rates is selected.

Bit 0 — This signal is sent to the interface from the data terminal on pin 19 of the terminal connector. When bit 0 is a 1, the secondary request to send line is raised high indicating to the interface that the terminal has information to send.

R6OUT Register (option 001 cable)

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
———	———	———	Half/Full Speed Control	Testing Purposes Pin 25	Data Signal Rate Select (U.K.)Pin 11	Data Signal Rate Select Pin 23	Secondary Request To Send Pin 19
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bits 7 thru 5 — Not used.

Bit 4 — This bit is used to signal the interface that either half or full speed data transfer is in effect (see R6OUT, bit 1). When this bit is a 0, normal bit rate clock speed is being used. When bit 4 is a 1, data transfer is half the switch selected bit rate. Bit 4 information is used internally by the interface.

Bit 3 — Is used for testing purposes only. This bit is output to pin 25 of the modem connector.

Bit 2 — This signal is sent from the interface to the modem on pin 11 of the modem connector. Pin 11 is used in the United Kingdom for the Data Signal Rate Select signal. The signal is used to select between two data signalling rates or two ranges of data signalling rates. When bit 2 is a 1, the higher data signalling rate or range of data signalling rates of the modem is being requested.

Bit 1 — This signal is sent from the interface to the modem on pin 23 of the modem connector. Pin 23 is used for the Data Signal Rate Select signal. The signal is used to select between two data signalling rates or two ranges of data signalling rates. When bit 1 is a 1, the higher data signalling rate of the modem is requested.

Bit 0 — Is sent from the interface to the modem on pin 19 of the modem connector. When this signal is a 1, the Secondary Request to Send signal is sent to the modem indicating to the modem that the computer has information to send.

R6IN Register (option 001 cable)

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 1	Always 1	Always 1	Always 1	Always 1	Secondary Carrier Detect Pin 12	Ring Indicator Pin 22	Data Carrier Detect Pin 8
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bits 7 thru 3 — Not used.

Bit 2 — The signal is sent to the interface from the modem on pin 12 of the modem connector. When bit 2 is a 1, it indicates that the secondary channel carrier is being received.

Bit 1 — This signal indicates to the interface that a ringing signal is being received by the modem when bit 1 is a 1. The signal is sent to the interface on pin 22 of the modem connector.

Bit 0 — This signal, Carrier Detect, indicates to the interface that the modem is receiving an acceptable signal, when bit 0 is a 1. This signal is sent to the interface on pin 8 of the modem connector.

Chapter 4

Talking to the Interface

Introduction

This chapter describes how to program the 98036A interface for your particular data communications application. It is assumed that you have set the hardware configuration switches (Chapter 3) as required. A select code value of 10 is assumed for all program statements shown. BASIC and HPL program statements are provided.[1] The appropriate I/O ROM(s) must be installed in your Desktop Computer.

Setting Control or Data Mode

Since the same interface register (R4) is used for transfer of USART control and status information as well as data, some method of determining "which is which" must be provided. Bit 0 of the R5OUT register is used for this purpose.

When bit 0 of R5OUT is 0, all data transferred to the R4OUT register from the computer is sent over the data communications link by the USART as serial data and all data entered into the computer from the R4IN register is the serial data received by the USART from the data communications link.

When bit 0 of R5OUT is 1, the data transferred to the R4OUT register by the computer is interpreted as either the USART's mode or control word, and the data entered from the R4IN register into the computer is the USART status word.

NOTE

When you set bit 0 of R5OUT, you are then in the USART control or status mode. You must clear bit 0 of R5OUT before you can resume data transfers.

---

1 The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

Here's the R5OUT register.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interface Interrupt Enable	———	Programmed Interface Reset	———	———	Interrupt Control 2 Receiver Control	Interrupt Control 1 Transmitter Control	R4 Control 0 = Data IN OUT 1 = Control Status
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Here's how to change bit 0 of R5OUT.

```
The following lines show how to set R5OUT to either control or data mode[1]

        BASIC                       HPL

10  WAIT WRITE 10,5;1       0: wtc 10,1          ! Set R5OUT to CONTROL mode
20  WAIT WRITE 10,5;0       1: wtc 10,0          ! Set R5OUT to DATA mode
```

Status

One important requirement of an interface is to provide you with status information. The 98036A interface returns two types of status information:

- Interface status.
- USART status.

Interface Status

The status of the interface is contained in the R5IN register. Here's how to read the interface status from the R5IN register.

```
The following program lines read the interface status register (R5IN)[1]

        BASIC                       HPL

10  STATUS (10);A           0: rds(10)→A         ! Get interface status
20  DISP "STATUS=";A        1: dsp"STATUS=",A    ! Display the Status value

STATUS= 272
```

[1] The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

Here is the R5IN register.

Most Significant Bit — Least Significant Bit

BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Peripheral Status 1	Interface Interrupt Enable Status	0	Interface I.D. 0 Always 0	Interface I.D. 1 Always 1	0	0	Control Status 2 Receiver Mode	Control Status 1 Transmitter Mode
BIT VALUE=256	BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

The value returned into variable A is the summed total of the bit value(s) of all bits that are set (1). In the above example the status value is 272. This value means that bits 4 and 8 are set (16+256=272), and all other bits (0 through 3 and 5 through 7) are 0.

USART Status

In order to obtain the status of the USART, you must first set bit 0 of R5OUT to the control mode (1), then perform an R4IN operation to return the USART status word.

```
The following program sets R5OUT to the control mode, reads the USART
status register into variable "A", displays the USART status value, and
and sets R5OUT back to the data mode.[1]

        BASIC                          HPL

10  WAIT WRITE 10,5;1          0: wtc 10,1          ! Set R5OUT to control mode
20  A=READBIN(10)              1: rdb(10)→A         ! Read USART Status register
30  DISP "STATUS=";A           2: dsp"STATUS=",A    ! Display the status
40  WAIT WRITE 10,5;0          3: wtc 10,0          ! Set R5OUT to data mode


STATUS= 5
```

Here is the USART status word.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Request To Send Pin 4(Standard) Data Set Ready Pin 6 (Option 001)	Always 0	Framing Error	Overrun Error	Parity Error	Transmitter Empty	Receiver Ready	Transmitter Ready
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

1 The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

The value returned into variable A is the summed total of the bit value(s) of all bits that are set (1). In this example the value of A is 5. This value means that bits 0 and 2 are set (1+4=5), and all other bits (1, and 3 through 7) are 0.

Resets

Three programmed resets are provided by the 98036A interface. The resets provided are:

- Programmed interface reset.
- Error bit reset.
- USART reset.

Programmed Interface Reset

When the programmed interface reset is executed, the 98036A interface is reset to the power up default condition. The power up default conditions are:

- The USART mode word is reset to the default condition specified by the mode word switches.
- The USART control word is set to a decimal value of 5 (Bits 0 and 2 are 1).
- All other interface registers are cleared (set to 0).

In order to reset the interface, simply send a control word to set bit 5 of the R5OUT register. Here's the R5OUT register.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interface Interrupt Enable	———	Programmed Interface Reset	———	———	Interrupt Control 2 Receiver Control	Interrupt Control 1 Transmitter Control	R4 Control 0 = Data IN/ OUT 1 = Control/ Status
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Here's a program line to set bit 5 of R5OUT.

```
The following program line executes a PROGRAMMED INTERFACE RESET.
R5OUT is automatically set to the data mode when this is executed.[1]

        BASIC                       HPL

10  WAIT WRITE 10,5;32        0: wtc 10,32          ! Execute the RESET
```

[1] The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

Error Bit Reset

When an error is detected in the received data, the USART sets an error bit in the USART status word. If you suspect that errors may exist in your input data you can periodically check the USART status word (see USART Status) for the presence of error bits. If errors have been detected you should reset the error bits in order to detect any subsequent errors.

To reset the USART error bits you must first set bit 0 of R5OUT to the control mode (1), then perform an R4OUT operation with bit 4 set.

Here's the USART control word.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 0	USART Reset	Clear To Send Pin 5(Standard) Request To Send Pin 4 (Option 001)	Reset Status Bits of USART Status Word	Send Break Character	Enable Data Receiver	Data Set Ready Pin 6(Standard) Data Terminal Ready Pin 20 (Option 001)	Enable Data Transmitter
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Here's how to reset the USART error bits.

The following program lines set R5OUT to the control mode, resets the USART error bits, and sets R5OUT back to the data mode.[1]

BASIC

```
10  WAIT WRITE 10,5;1
20  WRITE BIN 10;16
30  WAIT WRITE 10,5;0
```

HPL

```
0: wtc 10,1      ! Set R5OUT to control mode
1: wtb 10,16     ! Reset the USART error bits
2: wtc 10,0      ! Set R5OUT to data mode
```

USART Reset

When a USART reset is executed, the USART is forced into an idle mode.[2] The next data byte sent to the interface must be a new mode word for the USART. The USART then begins operating in the mode specified by the new mode word (see "USART Mode Word," page 34). The USART reset does NOT reset the interface but does reset the error bits. In order to reset the USART you must first set bit 0 of R5OUT to the control mode (1), then perform an R4OUT operation with bit 6 set.

1 The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

2 Because the USART is forced into the idle mode, data may be lost if it has not been completely transmitted. To avoid this potential loss, 2 null (0) or del (255) characters should be sent before resetting the USART.

Here's the USART control word.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 0	USART Reset	Clear To Send Pin 5(Standard) / Request To Send Pin 4 (Option 001)	Reset Status Bits of USART Status Word	Send Break Character	Enable Data Receiver	Data Set Ready Pin 6(Standard) Data Terminal Ready Pin 20 (Option 001)	Enable Data Transmitter
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Here's how to reset the USART.

```
The following program lines set R5OUT to control mode and reset the USART.
The USART then interprets the next data byte from the Desktop Computer as
as a new USART mode word.[1]

        BASIC                    HPL

10  WAIT WRITE 10,5;1       0: wtc 10,1      ! Set R5OUT to control mode
20  WRITE BIN 10;64         1: wtb 10,64     ! Reset the USART

The next write operation to the interface MUST be a new USART mode word.
The USART mode word is explained next.
```

USART Mode Word

When the USART reset has been executed (see USART reset, page 33) the USART clears the previous mode word, goes into an idle state, and waits for the computer to send a new mode word. A new mode word can NOT be sent to the USART unless a USART reset (setting bit 6 of USART Control word) has been executed.

Here's the USART mode word.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Number of Stop Bits 00=not valid 01=1 bit 10=1.5 bits 11=2 bits		Parity Type 0=Odd 1=Even	Parity Enable 0=Disable 1=Enable	Character Length 00=5 bits 01=6 bits 10=7 bits 11=8 bits		Bit Rate Factor 00=not used 01=1×bit rate clock 10=1/16×bit rate clock 11=1/64×bit rate clock	
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

1 The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

Assume that you want to set a new mode word to specify the following mode of operation.

1. Bit resolution of 1/64 is selected.
2. 7 bit character length specified. Note that character length only specifies the number of data bits that make up a complete character – start, stop, and parity bits are NOT considered part of the character and are NOT to be included when determining character length.
3. Parity is used and is specified as odd.
4. One stop bit is specified.

Here's how to determine the value of your new mode word.

Parameter	Permissible Value	Example Value
Bit Resolution	1=Bit/1 2=Bit/16 3=Bit/64	3
Character Length	0=5 bit characters 4=6 bit characters 8=7 bit characters 12=8 bit characters	8
Is parity used	0=no 16=yes	16
If parity what type	0=odd 32=even	0
How many stop bits	64=1 stop bit 128=1½ stop bits 192=2 stop bits	64
Summed total of the example values=		91

To send the example USART mode word, simply send the summed total of the example values (91) to the interface after a USART reset (see USART reset, page 33) has been executed.

Here's how to send a new mode word.

```
The following program line is executed after the USART reset routine.
The example value of 91 is sent as a new USART mode word.[1]

        BASIC                    HPL

30  WRITE BIN 10;91         2: wtb 10,91     ! Set new USART mode word
```

The next write operation MUST be a new USART control word. The USART control word is described next.

Transmitter/Receiver Control

This section describes the programming steps that provide control of various USART functions. The control functions described here are accessed via the USART control word. In order to change the USART control word you must first set bit 0 of R5OUT to the control mode (1), then write the USART Control word value to the R4OUT register.

Here's the USART control word.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 0	USART Reset	Clear To Send Pin 5(Standard) Request To Send Pin 4 (Option 001)	Reset Status Bits of USART Status Word	Send Break Character	Enable Data Receiver	Data Set Ready Pin 6(Standard) Data Terminal Ready Pin 20 (Option 001)	Enable Data Transmitter
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Bit 0 allows you to enable or disable the USART's transmitter. Bit 2 allows you to enable or disable the USART's receiver.

Here's how to control the transmitter and receiver.

```
The following program lines are executed after the USART mode word is
set.  The value (37) sets the "Request to Send" or "Clear to Send" line
and enables the transmitter and receiver.[1]

        BASIC                    HPL

40  WRITE BIN 10;37         3: wtb 10,37     ! Set new USART control word
50  WAIT WRITE 10,5;0       4: wtc 10,0      ! Set R5OUT to data mode
```

[1] The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

Break and R4 Modem Control Signals

This section describes the programming steps that enable you to send a "break," Data Set Ready/Data Terminal Ready, and Request to Send/Clear to Send. The controls described here are accessed via the USART control word. In order to change the USART control word you must first set bit 0 of R5OUT to the control mode (1).

Here's the USART control word.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 0	USART Reset	Clear To Send Pin 5(Standard) / Request To Send Pin 4 (Option 001)	Reset Status Bits of USART Status Word	Send Break Character	Enable Data Receiver	Data Set Ready Pin 6(Standard) Data Terminal Ready Pin 20 (Option 001)	Enable Data Transmitter
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

NOTE

The modem lines affected by bits 1 and 5 of the USART control word depend upon your particular cable options (see cable options, page 3).

Sending a "break"

A "break" is defined as a space condition held on the RS232 data line for ≥200msec.

Here's how to send a 200 msec "break" over the communications link.

The following program lines send a 200 millisecond "BREAK".[1]

```
BASIC                          HPL

10  WAIT WRITE 10,5;1          0: wtc 10,1      ! Set R5OUT to control mode
20  WRITE BIN 10;8             1: wtb 10,8      ! Send "Break" signal
30  WAIT 200                   2: wait 200      ! Wait 200 milliseconds
40  WRITE BIN 10;37            3: wtb 10,37     ! Send NEW USART control word
50  WAIT WRITE 10,5;0          4: wtc 10,0      ! Set R5OUT to data mode
```

1 The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

Clear to Send/Request to Send

Here's how to send Clear to Send (standard cable) to the terminal or Request to Send (option 001) to the modem.

```
The following program lines control the following modem signals:[1]
Clear to Send          (Standard Cable    - Pin 5)
Request to Send        (Option 001 Cable  - Pin 4)

       BASIC                    HPL


10  WAIT WRITE 10,5;1      0: wtc 10,1         ! Set RSOUT to control mode
20  WRITE BIN 10;32        1: wtb 10,32        ! Send CTS/RTS signal
30  WAIT WRITE 10,5;0      2: wtc 10,0         ! Set RSOUT to data mode
```

Data Set Ready/Data Terminal Ready

Here's how to send Data Set Ready (standard cable) to the terminal or Data Terminal Ready (option 001) to the modem.

```
The following program lines control the modem signals listed below.[1]
Data Set Ready              (Standard cable   - pin  6)
Data Terminal Ready         (Option 001 Cable - pin 20)

       BASIC                    HPL


10  WAIT WRITE 10,5;1      0: wtc 10,1         ! Set RSOUT to control mode
20  WRITE BIN 10;2         1: wtb 10,2         ! Send DSR/DTR modem line
30  WAIT WRITE 10,5;0      2: wtc 10,0         ! Set RSOUT to data mode
```

1 The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

Additional Modem Signals

This section describes the modem signals contained in the R6IN and R6OUT registers. Access to the R6 registers is obtained by performing an R6 read or an R6 write operation to the interface.

Here's the R6 registers.

R6 OUT (Standard Cable)

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
———	———	———	Half/Full Speed Control (Interface)	Ring Indicator Pin 22	Signal Quality Detect Pin 21	Secondary Carrier Detect Pin 12	Data Carrier Detect Pin 8
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

R6 IN (Standard Cable)

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 1	Always 1	Always 1	Always 1	Always 1	Always 0	Data Signal Rate Select Pin 23	Secondary Request To Send Pin 19
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

R6 OUT (Option 001 Cable)

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
———	———	———	Half/Full Speed Control	Testing Purposes Pin 25	Data Signal Rate Select (U.K.)Pin 11	Data Signal Rate Select Pin 23	Secondary Request To Send Pin 19
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

R6IN (Option 001 Cable)

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Always 1	Always 1	Always 1	Always 1	Always 1	Secondary Carrier Detect Pin 12	Ring Indicator Pin 22	Data Carrier Detect Pin 8
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

Carrier Detect

The two most commonly used R6 modem signals are the Carrier Detect signals.

The Carrier Detect signal from the modem is monitored by performing an interface read operation to the R6IN register (option 001 cable only). Here's how to check for the Carrier Detect signal.

The following program checks for Data Carrier Detect (Option 001 Cable)[1]

BASIC

```
10  READ IO 10,6;A
20  IF BIT(A,0) THEN 40
30  STOP
40  PRINT "BIT 0 Set"
50  STOP
```

HPL

```
0: wti 0,10           ! Selects select code 10
1: rdi (6)→A          ! Read R6IN
2: if bit(0,A);jmp 2  ! Check for Bit 0 set
3: stp
4: prt "BIT 0 Set"    ! Print Bit 0 message
5: stp
```

The Carrier Detect signal is sent to the terminal by performing an interface write operation to the R6OUT register (standard cable only).

Here's how to send the Carrier Detect signal.

The following program sends Data Carrier Detect (Standard Cable)[1]

BASIC

```
10  WRITE IO 10,6;1
```

HPL

```
0: wti 0,10           ! Selects select code 10
1: wti 6;1            ! Send Data Carrier Detect
```

[1] The program lines shown must be modified for System 45A or 9825A Systems Programming ROM applications. See Appendix A.

Other Modem Signals

Access to the following modem signals is also provided by the R6 registers:

- Data Signal Rate Select (for two speed modems).
- Data Signal Rate Select (United Kingdom applications).
- Ring Indicator.
- Secondary Carrier Detect.[1]
- Secondary Request to Send.[1]

Complete descriptions of these modem lines and their functions are found in Chapter 3, R6 Registers. These lines are monitored or sent as shown in the previous examples.

Half/Full Speed Interface Control

The RS-232C Data Signal Rate Select signal provides program selectable full or half speed transfer rates when two speed modems are used. Half speed transfer rates can be specified when error rates become unacceptable during full speed operation.

Interrupts

The 98036A provides interrupt-driven transfer capability. The interrupts are enabled under program control. The 9825A provides the enable interrupt (eir) statement, and the System 35/45 provides the CONTROL MASK and CARD ENABLE statements. These statements control bits 7, 2, and 1 of the R5OUT register. Bit 7 enables the interface to interrupt the computer when a pre-defined condition occurs and bits 2 and 1 define the condition(s). Bit 2, when set to a 1, causes an interrupt to be generated when received data is ready for transfer to the computer. Bit 1, when set to a 1, causes an interrupt to be generated when the transmitter is ready to accept more data from the computer.

Here's the R5OUT register.

Most Significant Bit — Least Significant Bit

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interface Interrupt Enable	———	Programmed Interface Reset	———	———	Interrupt Control 2 Receiver Control	Interrupt Control 1 Transmitter Control	R4 Control 0 = Data IN/ OUT 1 = Control/ Status
BIT VALUE=128	BIT VALUE=64	BIT VALUE=32	BIT VALUE=16	BIT VALUE=8	BIT VALUE=4	BIT VALUE=2	BIT VALUE=1

1 Secondary channel not implemented but these lines are provided.

Enabling Transmitter Interrupts

Here's how to enable transmitter interrupt operation.

```
The following program lines show how to enable the interface card
to generate an interrupt when the transmitter is ready to accept
more data from the computer.
```

```
        BASIC                          HPL

 10  ON INT# 10 GOSUB Xmit      0: oni 10,"xmit"   ! DEFINE THE BRANCH
 20  CONTROL MASK 10,130        1: eir 10,130      ! SET CONDITIONS
 30  CARD ENABLE 10
```

Enabling Receiver Interrupts

Here's how to enable receiver interrupt operation.

```
The following program lines show how to enable the interface card
to generate an interrupt when the receiver has data ready for input
to the computer.
```

```
        BASIC                          HPL

 10  ON INT#10 GOSUB Rxv        0: oni 10,"rxv"    ! DEFINE THE BRANCH
 20  CONTROL MASK 10,132        1: eir 10,132      ! SET CONDITIONS
 30  CARD ENABLE 10
```

Clearing Interrupts

Here's how to clear (disable) interrupt operation.

```
Here's how to disable the interrupts.
```

```
        BASIC                          HPL

 10  WRITE IO 10,0              0: wtc 10,0        ! CLEAR THE R5 REGISTER
```

The System 35/45 I/O ROM automatically provides for interrupt enable when BINT or WINT transfer types are specified. BINT and WINT transfer types can be used with serial peripherals such as printers, terminals, etc.

Chapter 5

Theory of Operation

Introduction

This chapter describes the 98036A theory of operation. Refer to the block diagrams and the 98036A schematic diagram while reading this chapter.

The 98036A Serial Interface converts 8-bit parallel data from the computer into a serial bit stream compatible with RS-232C hardware protocol. A Universal Receiver-Transmitter (USART) is the heart of the interface, performing the serial-to-parallel and parallel-to-serial conversions. Only the 8 least significant bits of the 16 bit computer I/O bus are used by the interface.

Interface Registers

The computer communicates with the interface through the R4, R5, and R6 registers. The registers have been assigned the following basic duties:

- R4 — Primary USART data register.
- R5 — Interface control and status register.
- R6 — Secondary data register.

The 98036A has an extended set of registers, expanding the R4 register into five unidirectional registers (from the computer's viewpoint), R4A through R4E. Bit configurations for the R4 registers are detailed in chapter 3. The actual location of R4A through R4E is in the USART integrated circuit.

The R4OUT register (U26 and U27) holds the data from the computer until the USART can accept the transfer.

The R4IN register (U29 and U30) holds received data until requested by the computer.

The least significant bit of the R5OUT register (U10) is the control/data bit (C/D), which defines R4 register access. Bits 1 and 2 are the interrupt control bits (INC1 and INC2) which allow the transmitter or receiver in the USART to be interrupt driven. Bit 7 is the interrupt enable, allowing the interface to interrupt the computer based on conditions defined by the INC1 and INC2 bits.

The R5IN register is not really a register but a group of tri-state buffers connected to indicate various states of the 98036A. These gates are in U24 and U32.

R6OUT is a partially implemented register used for controlling those RS-232C functions needed for more complex serial links. U28 comprises bits 0 through 3 of R6OUT. Bit 4 is used to control the half/full speed feature of the interface. This feature, implemented in U7, U20 and U21, will cut the bit rate of the interface in half when bit 4 of R6OUT is set. This is accomplished by either routing the bit rate clock directly to the USART or through a flip-flop divider (U21), and then to the USART.

R6IN is not a register but is similar to R5IN, being composed of tri-state gates. These gates are connected to RS-232C-to-TTL level translators and report the real-time condition of the associated RS-232C status lines. These tri-state gates are in U35.

Register Control

The computer control signals DOUT, IOSB, IC1, and IC2 indicate the current interface operation to be performed. No operations will be performed by the 98036A unless the peripheral address lines (PA0 trough PA3) match the select code on the select code switch S1. A match generates the My Peripheral Address (MYPA) signal which activates the register control decoder, U2.

The register control decoder takes the four computer control signals mentioned above and generates four output register strobe signals and four input register activation signals.

Flag Signals

Normally, if the interface is busy, the flag (FLG) line is low. In some cases, it may be desirable to operate the 98036A under programmed I/O in one direction and under interrupt driven I/O in the other direction. A section of the 98036A being operated under interrupt does not have control of the flag line and may therefore be operated independently of the other section. During this simultaneous operation, the tri-state USART data bus is controlled by the linked R4 state machines which control bus direction. At worst case, there may be a 2 microsecond delay in granting the bus to a requesting section, which is well within the minimum character

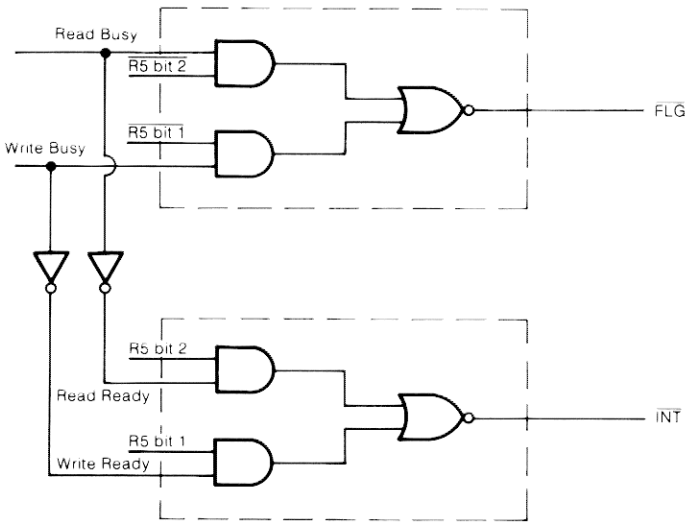
time in the interface, (approximately 1 millisecond). This character time varies with the bit rate and is important due to the nature of the RS-232 link. The computer usually has no control of the remote device, which may suddenly decide to transmit a block of text. If each character is not removed before the next received character is assembled, an overwrite will occur and the original character will be lost. This is why the operation of the receiver under interrupt is a good idea.

Interrupt Circuits

The interrupt poll responder (U22) has a two level interrupt scheme. Interfaces with select codes 2 through 7 (1 and 0 are illegal) are low priority while interfaces with select codes 8 through 15 are high priority. The 98036A select code is set as a high priority device from the factory to reduce the possibility of character overwrite. The select code however, is easily changed. To request an interrupt the interface sets an interrupt request line. If the interface has a low priority, it will set interrupt request low (IRL). If the interface has a high priority, it will set interrupt request high (IRH). The computer responds by setting interrupt poll (INT) and signifies whether a high or low level poll is occurring by placing the peripheral address line PA3 at the proper level. The interfaces that have interrupted at that level respond on the appropriate data line, for example if interface 3 requested service, it would respond on IOD3.

Interrupt control in the 98036A is implemented in U4, U10, U13, and a gate from U9. U22 is the interrupt poll responder.

The following simplified logic diagram shows how the flag and interrupt signals are generated by the interface card. The "read busy" and "write busy" signals are output by the input and output state machines.



For example, if R5 bit 1 and R5 bit 2 are both true then the flag line (FLG) is disabled, but an interrupt is generated (INT) when either Read Ready or Write Ready becomes true. Conversely, if R5 bit 1 and R5 bit 2 are both false then interrupts (INT) are disabled, but a flag (FLG) is generated when either Read Busy or Write Busy become true.

Clock Generator

The interface timing signals are all generated by the bit rate generator, U36. This includes the USART master clock, the state machine clocks and the bit rate clocks. U36 is a crystal controlled oscillator/divider.

I/O Drivers-Receivers

The signals inside the 98036A are all in the 0 to +5 volt range. Since the RS-232C specifications call for at least a ±3 volt swing, signal level translation is required. This is supplied by U37, U38, U39, and U40. The teletype-current-loop driver is composed of a discrete, switched 20ma. current source. The current receiver is a simple resistor divider with a zener diode clamp.

Setting Registers

Here is a description of the typical operations that occur in the interface when writing to and reading from the R4, R5, and R6 registers. The following sequence is described:

- WRITE IO statement to set bit 0 of R5OUT.
- WRITE BIN (or OUTPUT USING #,B) to set bit 6 of the USART control word, resetting the USART.
- WRITE BIN (or OUTPUT USING #,B) statement to set the USART mode word.
- WRITE BIN (or OUTPUT USING #,B) statement to set the USART control word.
- READBIN statement to read the USART status word.
- WRITE IO statement to clear bit 0 of R5OUT.
- STATUS statement to read interface status R5IN.
- WRITE IO statement to change R6OUT.
- READ IO statement to read R6IN.

Before any operation is started, the select code from the computer on the PA lines must match the interface select code. A match generates MYPA INT from U5 pin 3.

A WRITE IO statement from the computer results in an R5 strobe signal (R5SB) from pin 11 of U2.

The R5SB signal clocks the R5OUT register (U10) on pin 9. Since we want to set R5OUT bit 0 to a 1, IOD1 should be high. Bit 1 (U10 pin 15) is high when R5SB clocks U10. U14C is enabled and pin 12 of the USART (C/D) goes high. This sets the USART to accept the next byte as a control word.

A WRITE BIN (or OUTPUT USING #,B) statement to reset the USART (bit 6 of the USART control word) will result in IOD6 going high. The R4OUT strobe (R4SB) is generated to clock the IOD line information into R4OUT (U26 and U27).

R4SB also generates WR1 from U16 pin 13 and GEN from U17 pin 1. WR1 strobes pin 10 (WR) of the USART. GEN enables the R4OUT data to be sent to the USART on the D lines. Since the C/D line (pin 12) of the USART is set, this data byte is interpreted as a control word to the USART.

Since the previous byte reset the USART, the next WRITE BIN statement will be used as the USART mode word. This byte is input in the same sequence as described in the preceding paragraph.

The next byte after the mode word is handled in the same manner. This is the new control word for the USART.

While bit 0 of R5OUT is set the USART status word can be read. The READBIN statement generates R4IN from pin 4 of U2 which resets U19 pin 4 t a 0. Then D OUT from the computer goes to a 0. The R7SB signal (U2 pin 9) generates RD on pin 2 of U 16 and GEN on pin 1 of U17. The RD signal sets pin 13 of the USART and clocks the R4IN register (U29 and U30). When D OUT returns high, another R4IN strobe is generated which enables the R4IN tri-state gates (U29 and U30). The status word is then sent to the computer on the IOD lines.

Executing a WRITE IO statement with a decimal value of 0 will enable the interface to transmit and receive data. U10 pin 15 will be a 0 and the C/D line to pin 12 of the USART will be a 0.

Transmitting Data

Data transmitted to the data communications device is handled in the same manner as sending the USART mode and control words. The only difference is that pin 12 of the USART (C/D) is 0.

Receiving Data

Data received from the data communications device is handled in the same manner as reading the USART status word. The only difference is that pin 12 of the USART (C/D) is 0.

A WRITE IO 6 statement from the computer will generate R6SB on pin 12 of U2. This clocks the R6OUT register (U28) and sends information to the RS-232 signal lines.

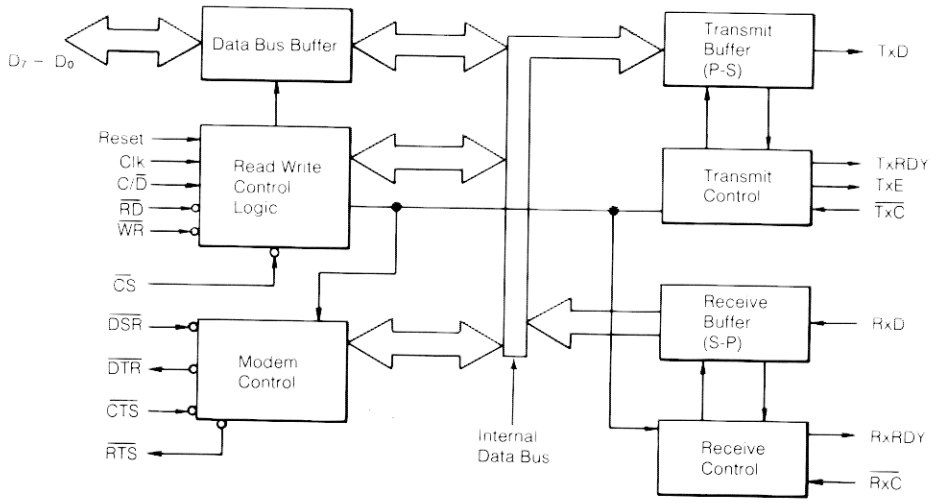
A READ IO statement from the computer will generate R6IN on pin 6 of U2. This enables the R6IN register (U35, U37, and U38). The R6IN information is sent to the computer on the IOD lines.

Reset

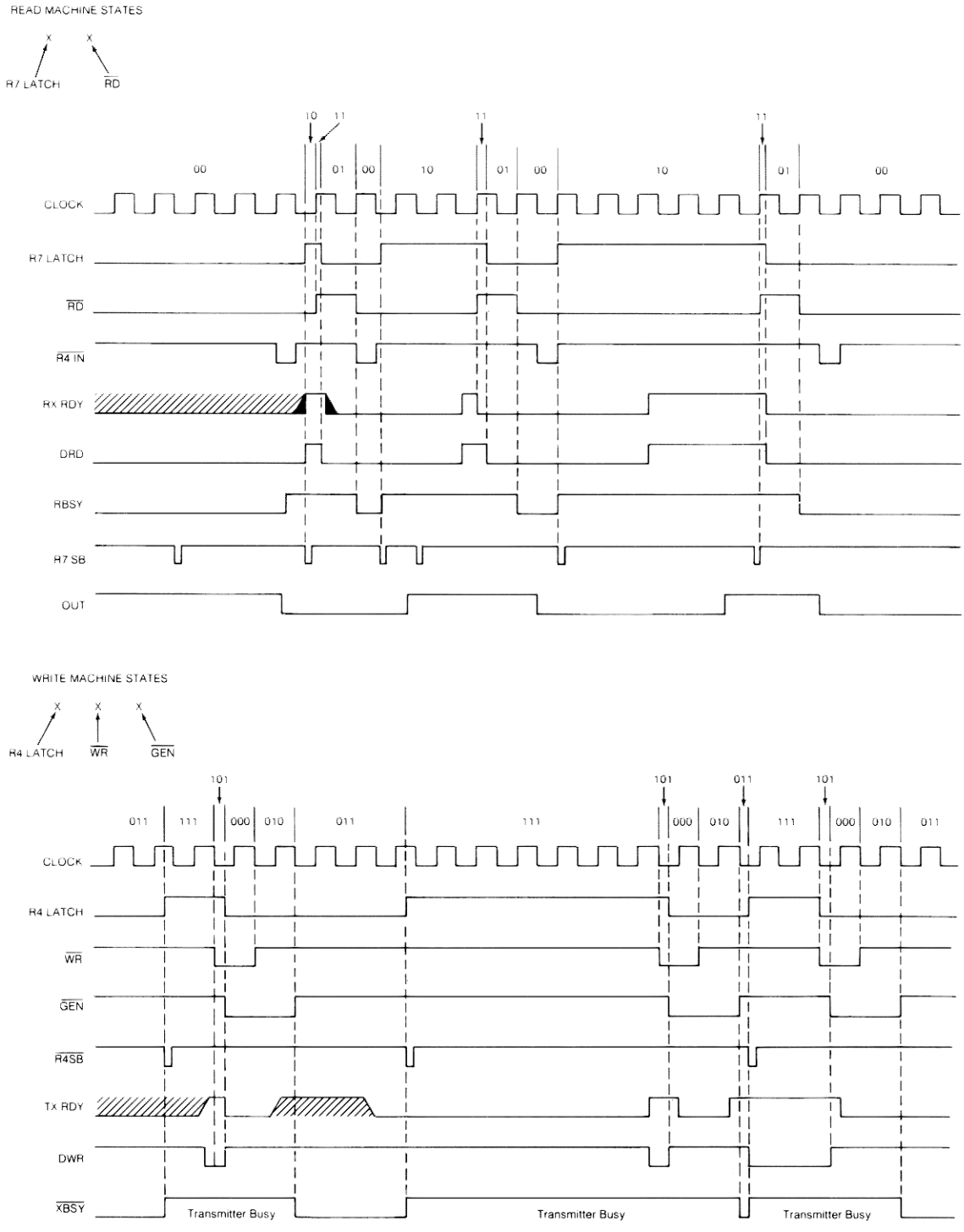
An interface reset (R5OUT bit 5) generates BUSY 2 from U5 pin 11 and RESET from U12 pin 6. RESET is applied to pin 21 of the USART (U31) to reset the USART latches. C/D from U14 pin 10 sets the USART to the control mode (pin 12=1) so the default control word and mode word can be written in the USART. WR2 from U6 pin 4 enables the default words to be written. MSEN from U6 pin 10 enables the default mode word from U34 and U33 to be written into the USART. CSEN from U6 pin 3 enables the control word (decimal 5) from U33 and U32 to be written into the USART. The last step of the reset operation is to set the C/D line to a 0 to enable data transfer.

The USART

The USART (U31) is the heart of the interface. Once the control and mode words are set, the USART provides the asynchronous mode format and the parallel-to-serial and serial-to-parallel data conversions. Here is a block diagram of the USART and a brief description of the mnemonics.



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
Clk	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for interface)
TxRDY	Transmitter Ready (ready for character from interface)
DSR	Data Set Ready
DTR	Data Terminal Ready
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground



98036A Timing Diagram

Chapter 6

Troubleshooting and Repair

Introduction

The following procedures assume that the computer, ROM, and peripheral device are operating correctly. If necessary, disconnect the interface from the computer and perform all other applicable test procedures before assuming that the interface is defective.

Recommended Equipment

The following is a list of equipment that will aid in troubleshooting the 98036A Serial Interface:

- Oscilloscope or Logic Probe
- Test Connector 98241-67936
- Extender Board 98241-67901
- Computer and appropriate ROM(s)

For checking most signals within the interface, any general purpose oscilloscope or logic probe can be used, if it is capable of indicating the presence of TTL level signals with pulse widths greater than 100ns.

Test Programs

Test programs to check the operation of the 98036A Interface are provided on the systems test tape supplied with your Desktop Computer. See the Systems Test Manual supplied with your computer for these test procedures.

Troubleshooting

To perform tests or checks on the interface, remove the front housing covers from the interface circuit assemblies. Use the Extender Board (98241-67901) to reconnect the interface to the computer (see the following photo).

Broken Trace Repair

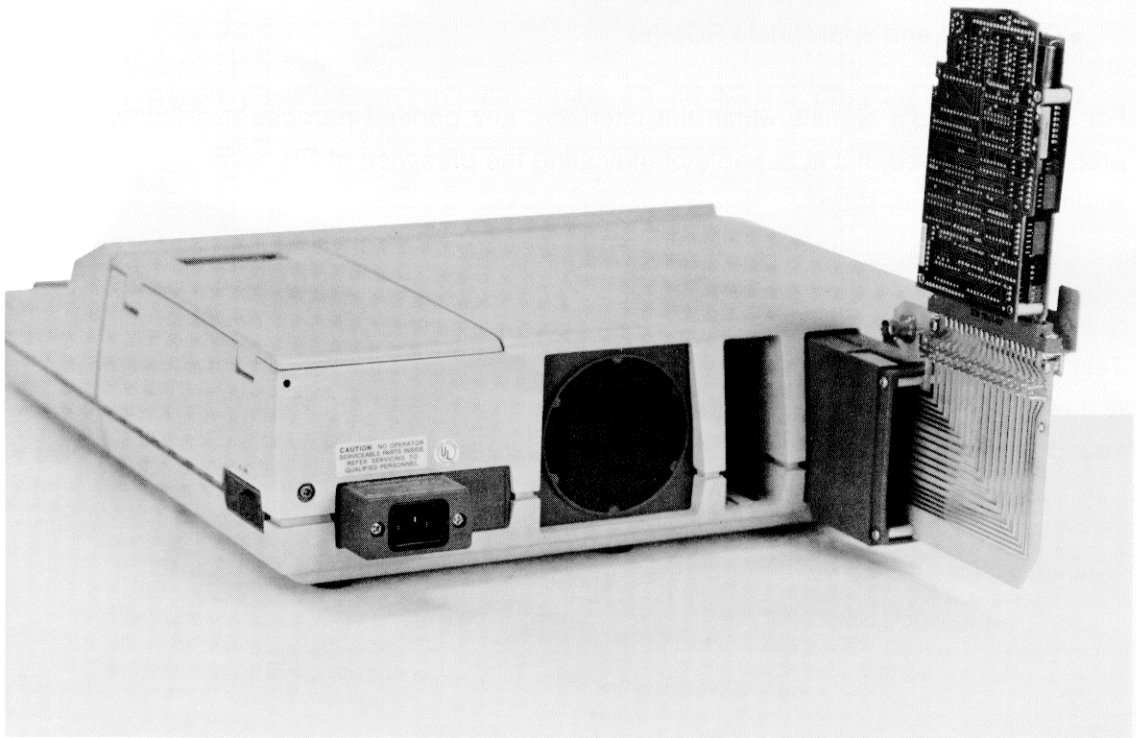
If one or more traces are open or have high resistance, the trace should be bridged using wire on the back of the boards where possible.

NOTE

The boards are of multi-layer construction and, therefore, require good soldering technique to prevent damage.

CAUTION

TO HELP PREVENT DAMAGE TO THE CIRCUIT BOARDS USE A LOW-TEMPERATURE SOLDERING IRON WHEN MAKING REPAIRS OR REPLACING PARTS.



Replaceable Parts

The next table lists the 98036A interface mechanical and electrical parts. The numbers in the quantity column indicate the total quantity of a part used on a particular interface assembly. The quantity is given only the first time the part number is listed.

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
A1	**98036-66501**		**Interface Assembly**
C1 thru C4	0160-3847	4	C-F: 01UF 25V
CR1	1902-3030	1	DIO: BKDN-3.01V
CR2	1902-3002	1	DIO: BKDN-2.37V
Q1	1853-0010	1	XSTR: PNP SM4713
Q2	1854-0215	1	XSTR: 2N3904
R1, R2	0757-0442	3	R-F: 10K 1%
R3	0683-1565	1	R-F: 15M 5%
R4	0757-0401	2	R-F: 100 1%
R5	0757-0465	1	R-F: 100K 1%
R6	0757-0288	1	R-F: 9.09K 1%
R7	0757-0279	1	R-F: 3.16K 1%
R8, R9	0757-0443	2	R-F: 11K 1%
R10	0757-0401		R-F: 100 1%
R11	0757-0442		R-F: 10K 1%
R12	1810-0203	1	R-Network
R13	1810-0139	1	R-Network
S1	3100-3364	1	Select Code Switch
S2	3101-2179	1	Switch, Current Loop
U1	1820-1297	2	IC: 74LS266
U2	1820-1427	1	IC: 74LS156
U3	1820-1297		IC: 74LS266
U4	1820-1198	1	IC: 74LS03
U5	1820-1197	1	IC: 74LS00
U6, U7	1820-0949	2	IC: CD4011
U8	1820-1208	1	IC: 74LS32
U9	1820-1199	1	IC: 74LS04
U10	1820-1562	1	IC: 74C175
U11	1820-0938	1	IC: CD4027
U12	1820-1145	1	IC: CD4049
U13	1820-1386	1	IC: MC14506
U14, U15	1820-1483	3	IC: CD4071
U16	1820-0939	2	IC: CD4013
U17	1820-0938		IC: CD4027
U18	1820-1486	1	IC: CD4081
U19	1820-1440	1	IC: SN74LS279
U20	1820-1483		IC: CD4071
U21	1820-0939		IC: CD4013
Y1	0410-1004	1	XTAL
	1251-4215	9	6 Pin Connector
	1251-4216	3	3 Pin Connector
A2	**98036-66502**		**Control Assembly**
C1 thru C4	0160-3847	5	C-F: .01UF 25V
C5	0180-0229	1	C-F: 33UF 10V
C6	0160-3847		C-F: .01UF 25V
C7 thru C14	0160-3694	8	C-F: 330PF 10%
CR1	1902-3030	1	DIO: BKDN 3.01V
R1 thru R4	0757-0442	4	R-F: 10K 1%
R5 thru R9	1810-0269	3	R-Network
S1	3101-1983	1	Switch, Default Mode Word
S2	3101-2172	1	Switch, Toggle
S3	3100-3378	1	Switch, Bit Rate

Replaceable Parts (cont.)

REFERENCE DESIGNATOR	-hp- PART NO.	TQ	DESCRIPTION
U22	1820-1427	1	IC: 74LS156
U23	1820-1584	1	IC: Binary Interface Buffer
U24	1820-1266	4	IC: 80C97
U25	1820-1562	1	IC: 74C175
U26, U27	1820-1190	4	IC: 74C173
U28	1820-1195	1	IC: 74LS175
U29, U30	1820-1190		IC: 74C173
U31	1820-1844	1	IC: USART
U32 thru U34	1820-1266		IC: 80C97
U35	1820-1492	1	IC:74LS368
U36	1820-1779	1	IC: Bit Rate Generator MC14411
U37, U38	1820-0510	2	IC: MC1489
U39, U40	1820-0509	2	IC: MC1488
P11	1251-3691	1	Connector Header
P1 thru P10	1251-4326	2	Connector Pins (36 pins per connector)
	98036-67901		**Front Housing Assembly** (Includes A1 and A2)
	2200-0536	8	Screw, 4-40
	7120-5911	1	Label
	7120-5171	1	Plate, USA
	5040-8163	1	Right Case
	5040-8158	1	Spring Latch
	5040-8161	1	Left Case
	7120-5717	1	Front Label
	98036-67902		**Rear Housing Assembly (standard)**
	2200-0510	2	Screw, 4-40
	5040-8174	1	Left Cover
	5040-8211	1	Right Cover (with hole)
	7120-5718	1	Rear Label
	98036-61601	1	Cable Assembly (standard)
	98036-61601		**Cable Assembly (standard)**
	1251-0392	1	Connector Hood
	1251-0688	17	Terminal Connector
	1251-2942	2	Connector Lock
	1251-3396	1	Connector Body
	1251-3399	17	Contact Connector
	1251-3808	1	Polarizing Plug
	1251-4701	1	Rod Housing
	1251-4702	1	Locking Rod
	5040-7859	1	Molded Cable
	98036-67903		**Rear Housing Assembly (Option 001)**
	7120-5719	1	Rear Lable, Option 001
	5040-8174	1	Left Cover
	5040-8211	1	Right Cover (with hole)
	98036-61602	1	Option Cable Assembly
	98036-61602		**Cable Assembly (Option 001)**
	1251-1438	1	Connector Hood
	1251-3397	17	Contact Connector
	1251-0063	1	Connector Body
	1251-3399	25	Connector Contact
	1251-3808	1	Polarizing Plug
	1251-4701	1	Rod Housing
	1251-4702	1	Locking Rod
	5040-7859	1	Molded Cable
	98036-67904		**Rear Housing Assembly (Option 002)**
	7121-0715	1	Rear Label, Option 002
	5040-8174	1	Left Cover
	5040-8211	1	Right Cover (with hole)
	98036-61603	1	Option Cable Assembly
	98036-61603		**Cable Assembly (Option 002)**
	1251-4998	1	Connector Hood
	1251-0688	17	Terminal Connector
	1251-6166	13	Contact Connector
	1251-3398	1	Connector Body
	1251-3808	1	Polarizing Plug
	1251-4701	1	Rod Housing
	1251-4702	1	Locking Rod
	5040-7859	1	Molded Cable

Appendix A

System 45A Programming Notes

THE FOLLOWING SHOWS THE MODIFICATIONS REQUIRED TO THE BASIC PROGRAM LINES SHOWN IN THE MANUAL FOR USE WITH THE SYSTEM 45A

```
   BASIC PROGRAM LINES                EQUIVALENT SYSTEM 45A

10  WAIT WRITE 10,5,0          10  IF NOT IOFLAG(10) THEN 10
                               11  WRITE IO 10,5,0
```

ALL WAITWRITE STATEMENTS MUST BE REPLACED WITH THE IOFLAG AND WRITE IO STATEMENT SEQUENCE AS SHOWN.

```
10  WRITE BIN 10,4;64          10 OUTPUT 10 USING "#,B";64
```

ALL WRITE BIN STATEMENTS MUST BE REPLACED WITH AN OUTPUT USING "#,B" STATEMENT AS SHOWN.

9825A Systems Programming ROM Notes

THE SYSTEMS PROGRAMMING ROM FOR THE 9825A PROVIDES SIMPLIFIED STATEMENTS FOR ACCESSING THE R4 MODE, CONTROL, AND STATUS WORDS. THE FOLLOWING SHOWS MODIFICATIONS FOR THE HPL PROGRAM LINES SHOWN IN THE MANUAL WHEN THE SYSTEMS PROGRAMMING ROM IS USED. PROGRAMS SHOWN ARE EQUIVALENT (SEE SYSTEMS PROGRAMMING MANUAL-09825-90027 FOR DETAILS).

R4 MODE WORD ACCESS

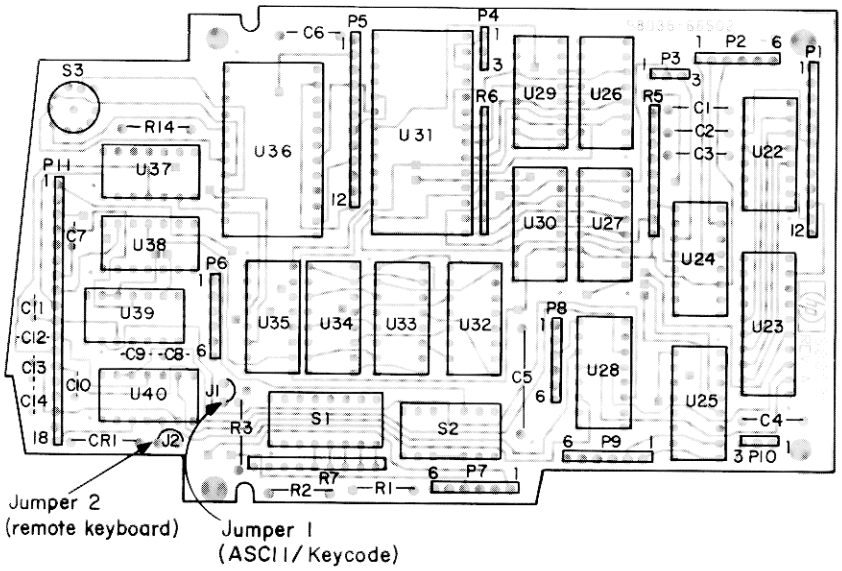
```
HPL PROGRAM LINES      SYSTEMS PROGRAMMING ROM EQUIVALENT

0: wtc 10,1
1: wtb 10,64
2: wtb 10,91           0: wsm 10,91      ! Sets MODE word only.
                             or
3: wtb 10,37           0: wsm 10,91,37   ! Sets MODE and CONTROL word.
4: wtc 10,0
```

```
            R4 CONTROL WORD ACCESS

HPL PROGRAM LINES       SYSTEMS PROGRAMMING ROM EQUIVALENT

0: wtc 10,1
1: wtb 10,2             0: wsc 10,2
2: wtc 10,0


            R4 STATUS WORD ACCESS

HPL PROGRAM LINES       SYSTEMS PROGRAMMING ROM EQUIVALENT

0: wtc 10,1
1: dsp rdb(10)          0: dsp rss(10)
2: wtc 10,0
```

Example Program

```
1     !  HERE IS A SIMPLE CHARACTER MODE EMULATOR THAT TRANSFERS DATA TO AN
2     !  H.P. 3000 COMPUTER AT 110 BAUD.  THIS PROGRAM REQUIRES NO MODEM.
3     !  WHEN "READY" AND THE COMPUTER PROMPT (:) APPEAR ON YOUR DISPLAY,
4     !  KEY IN YOUR DATA AND PRESS THE CONTINUE KEY OR THE STORE KEY TO
5     !  INDICATE THE END OF YOUR TRANSMISSION.
6     !
7     !
10    Card=10                                 ! DEFINE THE SELECT CODE
20    ON KBD GOSUB Key                        ! CHECK FOR KEYPRESS
30    RESET Card                              ! RESET THE INTERFACE
40    ON INT #Card,2 GOSUB Isr                ! DEFINE INTERRUPT
50    WAIT READ Card,4;Dummy                  ! DUMMY READ TO CLEAR INPUT BUFFERS
60    WRITE IO Card,7;0                       ! OUTPUT AN R7 STROBE
70    CONTROL MASK Card;132                   ! DEFINE THE INTERRUPT CONDITIONS
80    CARD ENABLE Card                        ! ENABLE THE INTERRUPTS
90    WRITE IO Card,4;13                      ! SEND END-LINE SEQUENCE TO THE REMOTE
100   DISP "READY"
110 Waiting:  GOTO Waiting                    ! WAIT FOR AN INTERRUPT
120 Isr: READ IO Card,4;Data                  ! READ IN THE DATA
130   WRITE IO Card,7;0                       ! OUTPUT AN R7 STROBE
140   IF Data>127 THEN Data=Data-128          ! CHECK FOR NON ASCII DATA
150   IF Data<>5 THEN Printout                ! DATA FROM REMOTE IS NOT AN "ENQ".
160   WAIT WRITE Card,4;6                     ! ANSWER THE "ENQ" WITH AN "ACK".
170   CARD ENABLE Card                        ! RE-ENABLE THE INTERRUPTS
180   RETURN
190 Printout: PRINT USING "#,B";Data          ! PRINT THE INPUT DATA
200   CARD ENABLE Card                        ! RE-ENABLE THE CARD
210   RETURN
220   !
230 Key:  K$=KBD$                             ! ON KEYBOARD ROUTINE
240   IF NUM(K$)=255 THEN K$=CHR$(13)         ! NON-ASCII KEY TO OUTPUT END-LINE
250   WAIT WRITE Card,4;NUM(K$)               ! TRANSMIT THE K$ DATA
260   RETURN
```

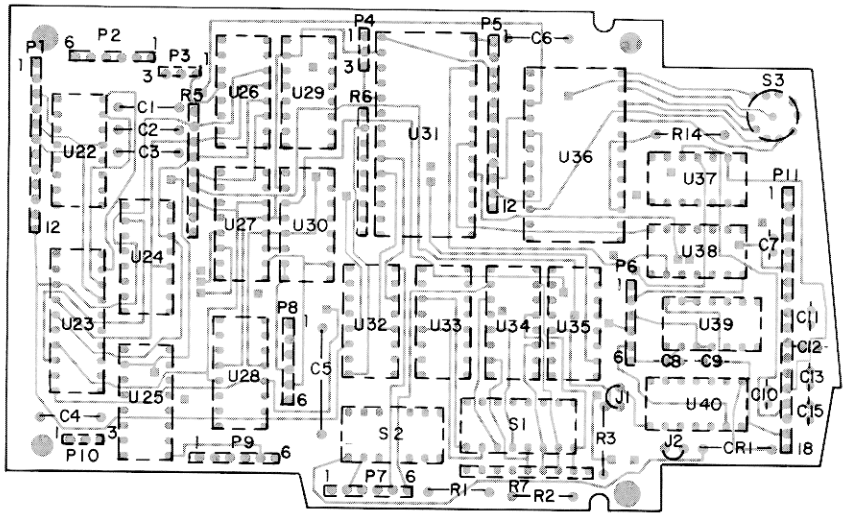
Appendix B



COMPONENT SIDE

A2

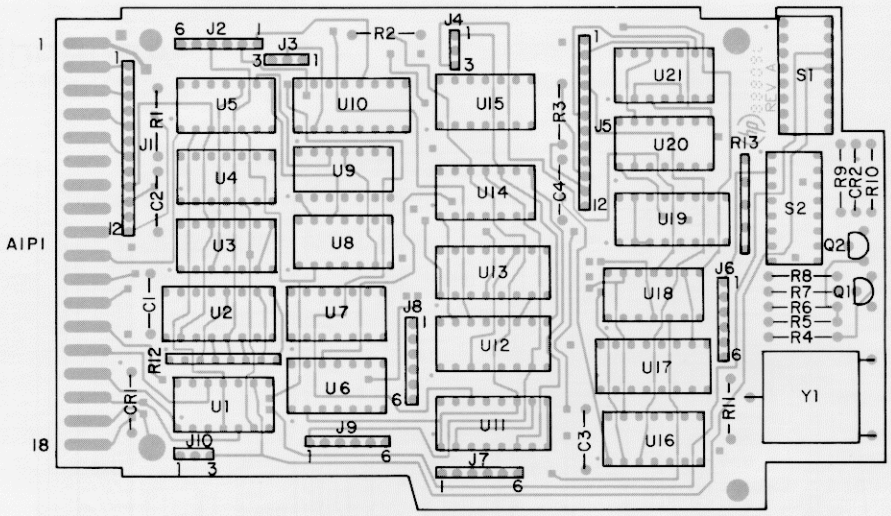
-hp- Part No. 98036-66502 Rev A



CIRCUIT SIDE

A2

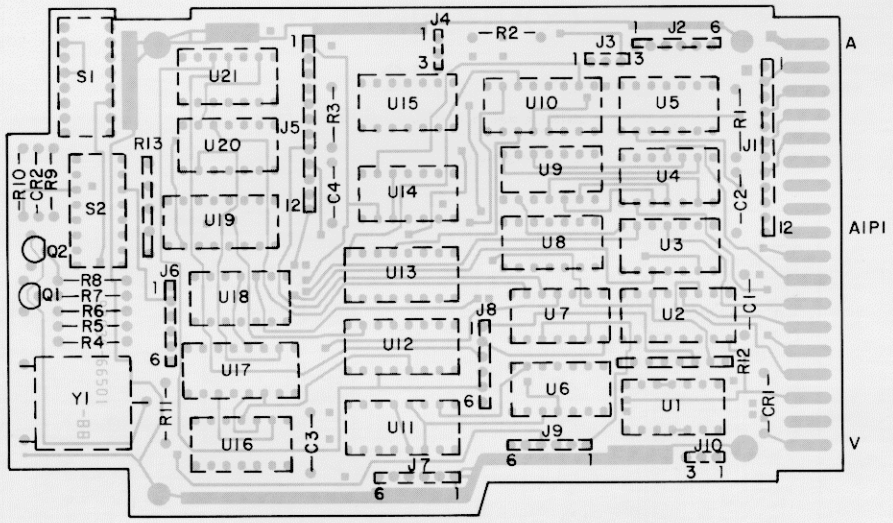
-hp- Part No. 98036-66502 Rev A



COMPONENT SIDE

A1

-hp- Part No. 98036-66501 Rev A



CIRCUIT SIDE

A1

-hp- Part No. 98036-66501 Rev A

98036A Interface Schematic Diagram

HP 98036A Serial I/O Interface

Installation and Service Manual

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