DISPLAY DRIVER CHIP — CHAPTER 5

This chapter contains a description of the 1LF3 display driver chip. The 1LF3 is designed to support the 1LF2 CPU and future processors that operate on the HP-71 bus. The display driver chip is divided into 4 functional areas:

1) An 8-way multiplexed Liquid Crystal Display (LCD) driver capable of functioning with other 1LF3's in a multi-chip display driver system.

2) 1K nibbles of RAM.

3) A 24 bit, quartz-crystal controlled timer.

4) A low battery indicator.

5.1 Pin Designations

The display driver's external pins are as follows:

PIN	DESCRIPTION
VDD	Power supply.
GND	System ground.
BUS[0:3]	System bus.
*STR	*STROBE
*CD	*CONTROL-DATA
OD	OUTPUT DISABLE - When high the bus is tristated; pulled low by an internal resistor.
CB(0,1)	CONFIGURATION BITs - 2 bits used for address configuration.
*CLK	Display-Timer clock; driven by MASTER.

*DON	*DISPLAY ON - Driven by MASTER; active low.
VREF	LCD voltage reference; driven by MASTER.
C[1:40]	40 LCD column drivers.
R[1:8]	8 LCD row drivers on MASTER; 8 LCD column drivers on SLAVE.
OSC(A,B)	2 pins used for quartz crystal connection.

5.2 Bus Commands

The display driver is a hard configured chip with service request capability. It responds to the bus commands listed in section 2.1.2 with the following exceptions:

1	ID	Same as NOP
8	CONFIGURE	Same as NOP
9	UNCONFIGURE	Same as NOP
A	POLL	If the timer has timed out (MSB=1) BUS0 is pulled high during the next *STR low (see section 2.4).
C	BUSCC	Same as NOP
E	SHUTDOWN	If the timer has timed out or times out during shutdown, *CD is pulled low to wake up the CPU (see section 2.4).
F	RESET	Same as NOP

5.3 Addressing

The 1K nibble of RAM requires 10 bits of address space, leaving 10 bits of configuration address. The most significant 8 bits of the RAM configuration are hard programmed. The other 2 bits are specified by CB0 and CB1.

The display RAM and timer are configured together and require 8 bits of address space, leaving 12 bits of configuration address. The most significant 10 bits of the display-timer configuration are

hard programmed and the other 2 bits are specified by CB0 and CB1.

The address space is mapped as shown below in hex. The reserved space contains no memory and cannot be used elsewhere in the system.

	SLAVE1	SLAVE2	MASTER
RAM (1024 nibbles)			
Starting addr =	2F400	2F800	2FC00
Ending addr =	2F7FF	2FBFF	2FFFF
Display RAM (96 nibbles)			
Starting addr =	2E100	2E200	2E300
Ending addr =	2E15F	2E2FF	2E35F
RESERVED (152 nibbles)			
Starting addr =	2E160	2E260	2E360
Ending addr =	2E3F7	2E2F7	2E3F7
Timer (6 nibbles - least significant first)			
Starting addr =	2E1F8	2E2F8	2E3F8
Ending addr =	2E1FD	2E2FD	2E3FD
Contrast Control Nibble (1 nibble - active only on MASTER)			
Addr location =	2E1FE	2E2FE	2E3FE
Display-Timer Control Nibble (1 nibble)			
Addr location =	2E2FF	2E2FF	2E3FF

5.4 Display Interface

The display driver chips function in one of 2 modes: MASTER or SLAVE. The MASTER has both CB1 and CB0 tied high by the PC board. It drives the timing signal *CLK, the control signal *DON, and the LCD voltage reference VREF. The MASTER's outputs R[1:8] drive the 8 rows of the LCD and it's outputs C[1:40] drive the 40 LCD columns on the right side of the display. The SLAVE chips accept *CLK, *DON, and *VREF as inputs. SLAVE1 has CB0 tied high and CB1 tied low and it's outputs R[1:8] and C[1:40] drive the 48 LCD columns in the center of the display. SLAVE2 has CB0 tied low and CB1 tied high and it's outputs R[1:8] and C[1:40] drive the 48 LCD columns on the left side of the display.

Each dot of the LCD has a corresponding bit in the display RAM. If that bit is a 1 and the display is on, the corresponding dot will be on.

16 nibbles of the MASTER's display RAM are allocated to row driver data used to control the row driver waveforms. The following data pattern is loaded by the operating system beginning at the hex address 2E350 of the MASTER.

Hex data (low addressed nibble first) = 8001400220041008

If the above data pattern has been loaded, the least significant bit of the low addressed nibble of the display RAM will correspond to the upper-left dot of the display; the next bit of that nibble will be mapped to just below that dot; and dot addresses will continue to increase down and to the right.

The data pattern shown is not the only valid pattern. For example, try entering : POKE '2E350','0180024004200810'. This pattern defines the rows in reverse order and will result in characters (and annunciators) being displayed upside-down. This can be fixed be either poking the correct pattern or by an INIT:1.

5.5 Contrast Control Nibble

A contrast control nibble is located at address 2E3FE of the MASTER. This nibble adjusts the LCD drive voltage, VREF and thus can be used to control the contrast of the display. The higher the value of the contrast control nibble the darker the dots appear. This nibble can be both read and written and has no effect if the chip is configured as a SLAVE.

5.6 Display-Timer Control Nibble

A display-timer control nibble is located at address 2EnFF of both MASTER and SLAVE chips. The bits of this control nibble are defined as follows. Note that some bits have different meanings for read and write.

BIT0 - READ & WRITE : DISPLAY ON; MASTER only; 1=on.

BIT1 - READ & WRITE : DISPLAY BLINK; MASTER only; 1=blink if BIT0 is set.

BIT2 - READ : VERY LOW BATTERY INDICATOR; MASTER only; 1=very low.
WRITE : DISPLAY TEST; WARNING !!! DO NOT SET THIS BIT ON MASTER, IT MAY FORCE DISPLAY OUT OF SYNC. MASTER only; When set *CLK is synchronized with *STR (for testing).

BIT3 - READ : LOW BATTERY INDICATOR; MASTER only; 1=low.
WRITE : TIMER ENABLE; 1=enable.

5.7 RAM

The 1LF3 RAM consists of 4096 bits of static hard configured memory arranged as 1024 4-bit nibbles.

5.8 Timer

The timer is a 6 nibble read/writeable binary counter located at addresses 2EnF8-2EnFD. The timer is decremented 512 times per second by the *CLK signal. The *CLK signal is derived from the MASTER's 32768 Hz quartz crystal oscillator and is also used to time display output signals. The MASTER chip requires a 32768 Hz crystal connected between OSCA and OSCB.

IMPORTANT: Because the timer decrement is asynchronous with the timing on the HP-71 bus, it is possible that a decrement will occur between the reading or writing of nibbles to the timer. This can cause erroneous values to be read from or written to the timer. It can be avoided by reading the timer twice within 1/512 second and verifying that both values are the same. If the values are not the same, immediately read the timer a third time. To write the timer, repeatedly read the least significant nibble until it decrements, then immediately write the timer value.

If the timer's most significant bit is a 1 and it is enabled by BIT3 of the display-timer control nibble the chip will respond to a service POLL by pulling BUS[0] low and it will wake up the CPU during shutdown by pulling *CD low. After waking the CPU the chip will not wake the CPU again until either the MSB of the timer or BIT3 of the control nibble has been cleared and set again.

The HP-71 operating system uses the timers to implement the real time clock system. For information on the clock system see the HP-71 software IDS, Volume 1.

5.9 Low Battery Indicator

The low battery indicator senses 2 power supply levels: low battery and very low battery. The 2 bits LBI and VLBI are read from BIT2 and BIT3 of the display-timer control nibble and are valid only on the MASTER. After each read of the control nibble a

new sample of the supply voltage begins. This sample requires 100us. After the sample is complete the LBI and VLBI bits are updated. If the control nibble is read before the sample is complete the old low battery values are read and a new sample begins.

The HP-71 operating system samples the LBI bit once each minute. If it is true, the BAT annunciator will be lit. The operating system ignores the VLBI bit.

ROM CHIP — CHAPTER 6

The 1LG7 ROM is designed to support the 1LF2 CPU and future processors that operated on the HP-71 bus. The ROM core consists of 128K bits of memory arranged as 32,768 four-bit nibbles.

6.1 Pin Designations

The pins of the 1LG7 ROM chip are as follows:

PIN	FUNCTION
VDD	Power Supply.
GND	System Ground.
BUS[0:3]	System bus.
*STR	*STROBE
*CD	*COMMAND-DATA
OD	OUTPUT DISABLE - when driven high, the ROM tri-states the BUS[0:3]; OD is passively pulled low on-chip by an internal resister.
DIN	Daisy chain input.
DOUT	Daisy chain output.

In the HP-71 system, the OD pins of the 4 system ROMs are tied together. This signal is available at PORT1, and with special hardware, at PORT3 and the HP-IL port. By pulling the OD line high, all 4 system ROMs are effectively removed from the bus.

6.2 Bus Commands

The 1LG7 ROM can be either hard or soft configured and has no service request capability. The ROM responds to the bus commands

described in section 2.1.2 with the following exceptions:

1	ID	If hard configured : same as NOP.
4	PC WRITE	The ROM increments its local program counter once each data strobe. No write is performed.
5	DP WRITE	The ROM increments its local data pointer once each data strobe. No write is performed.
8	CONFIGURE	If hard configured : same as NOP.
9	UNCONFIGURE	If hard configured : same as NOP.
A	POLL	Same as NOP.
C	BUSCC	Same as NOP.
E	SHUTDOWN	Same as NOP.
F	RESET	If hard configured : same as NOP.

The ROM's ID code is hard programmed (if soft configured). Generally, the ID code will be either 0010A, for one ROM of a multiple ROM set, or 8010A for an individual ROM or the last ROM of a multiple ROM set.

6.3 Addressing

The 32K nibbles of ROM require 15 bits of address space, leaving 5 bits of configuration address. The chip is selected when the upper 5 bits of the PC or DP (whichever is active) match the 5 bits stored in its configuration register and its configuration flag is set. The chip uses the remaining 15 bits to address its memory.

The ROM chip is manufactured in both soft and hard configured options (see section 2.2). In the hard configured option the 5 bits of the configuration register as well as the configuration flag are mask programmed to configure the ROM chip to a fixed address. The HP-71 operating system is stored in 4 mainframe ROMs configured as follows:

	ROM0	ROM1	ROM2	ROM3
Starting addr =	00000	08000	10000	18000
Ending addr =	07FFF	0FFFF	17FFF	1FFFF

Some plug-in ROMs are soft configured. In the soft configured option, the configuration register latchs the configuration address under software control as described in section 2.2.1.

RAM CHIP — CHAPTER 7

The 1LG8 RAM is designed to support the 1LF2 CPU and future processors that operate on the HP-71 bus. The RAM core consists of 8K bits of static memory arranged as 2048 four-bit nibbles.

7.1 Pin Designations

The pins of the 1LG8 RAM chip are identical to the pins of the 1LG7 ROM chip (see section 6.1) with the following addition:

ID	If tied high on the hybrid PC board (last chip) the most significant bit of the most significant nibble of the 5-nibble ID code will be set to a 1.

7.2 Bus Commands

The 1LG8 RAM is soft configured and has no service request capability. It responds to the bus commands as described in section 2.1.2 with the following exceptions:

A	POLL	Same as NOP.
C	BUSCC	Same as NOP.
E	SHUTDOWN	Same as NOP.

The RAM ID code is n000E, where n=0 if the ID pin is tied low and n=8 if the ID pin is tied high. The ID pin is tied high only on the last chip of the 4-chip hybrid.

7.3 Addressing

The 2K nibbles of RAM require 11 bits of address space, leaving 9 bits of configuration address. The chip is selected when the upper 9 bits of the PC or DP (whichever is active) match the 9 bits stored in its configuration register and its configuration flag is

set. The chip then uses the remaining 11 bits to address its memory. As an example of addressing, if a 4-chip RAM hybrid has been configured contiguously starting at 30000 hex, the following would apply:

	RAM0	RAM1	RAM2	RAM3
Starting addr =	30000	30800	31000	31800
Ending addr =	307FF	30FFF	317FF	31FFF

SYSTEM DIAGRAMS	CHAPTER 8

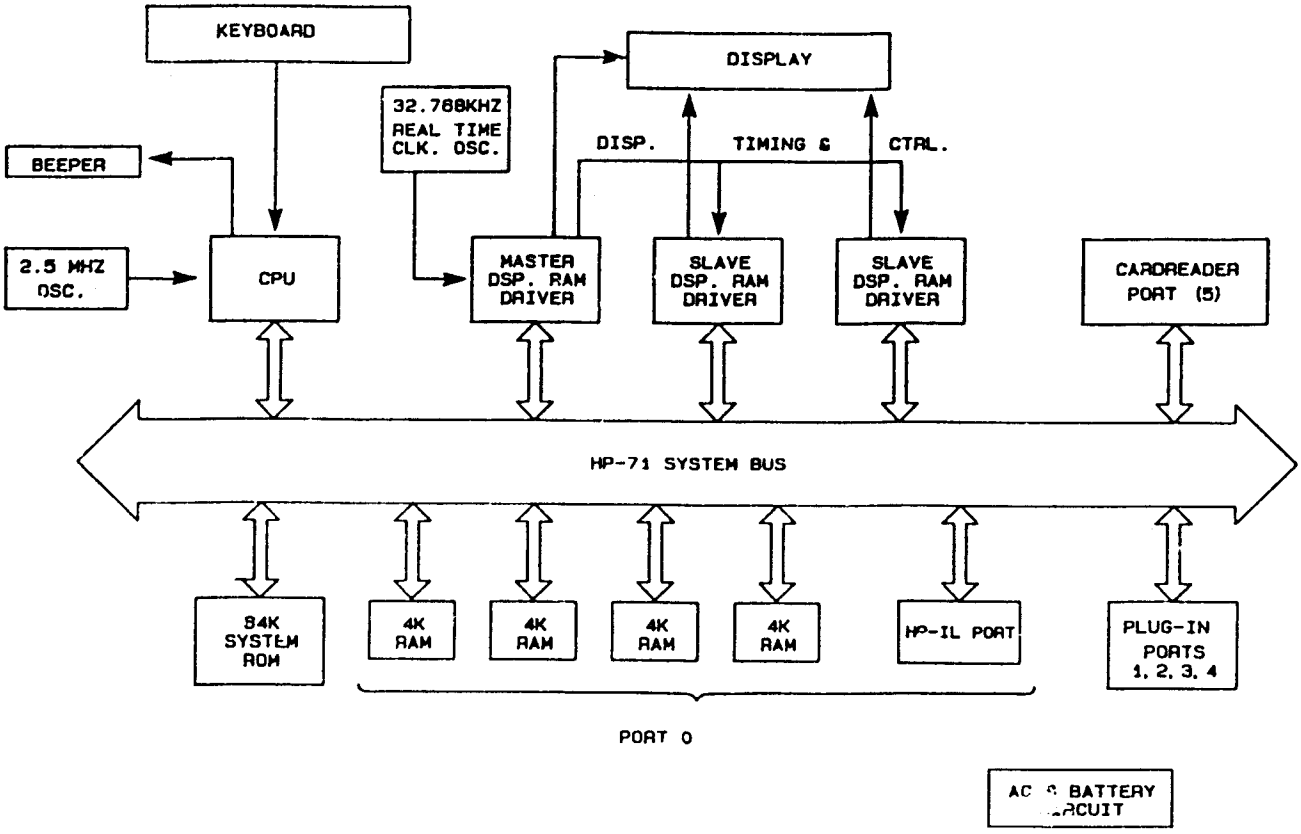

Figure 8-1. System Block Diagram

Table 8-1. Top-Case Assembly Replaceable Parts

INDEX NUMBER, FIGURE 7-1	HP PART NUMBER	DESCRIPTION	QUANTITY
C4,C5	0160-5789	CAPACITOR, 33 pF, 50V, 5%	2
C6,C7	0160-5790	CAPACITOR, 0.1 uF, 25V, 20%	2
C9,C10	0160-5787	CAPACITOR, 1000 pF, 5V, 20%	2
C11,C14	0160-5788	CAPACITOR, 220 pF, ±5%	2
L1	9140-0802	INDUCTOR, 180 uH, 5%	1
R20,R21	0699-1141	RESISTOR, 10K, 5%, 1/8W	2
Y1	0410-1381	CRYSTAL, quartz	1

Table 8-2. I/O Assembly Replaceable Parts

INDEX NUMBER, FIGURE 7-2	HP PART NUMBER	DESCRIPTION	QUANTITY
C1	0180-3351	CAPACITOR, 470 uF, 10V, 20%	1
C2	0180-3352	CAPACITOR, 330 uF, 16V, 20%	1
C8	0160-0576	CAPACITOR, 0.1 uF, 50V, 20%	1
C12	0160-3879	CAPACITOR, 0.01 uF, 20%	1
C13	0160-4441	CAPACITOR, 0.47 uF, 10%	1
CR2	1901-0999	DIODE, Schottky	1
CR3	1906-0069	DIODE, bridge, full-wave, 400V	1
CR7	1901-0704	RECTIFIER, silicon	4
L2	9140-0794	INDUCTOR, 56 mH, 10%	1
Q1	1854-0932	TRANSISTOR, NPN	1
Q2	1854-0973	TRANSISTOR,	1
R22	0683-3915	RESISTOR, 390 ohms, 5%, 0.25W	1
R23,R24	0683-1035	RESISTOR, 10 K-ohms, 5%, 0.25W	2
VR7	1902-1390	DIODE, Zener	1

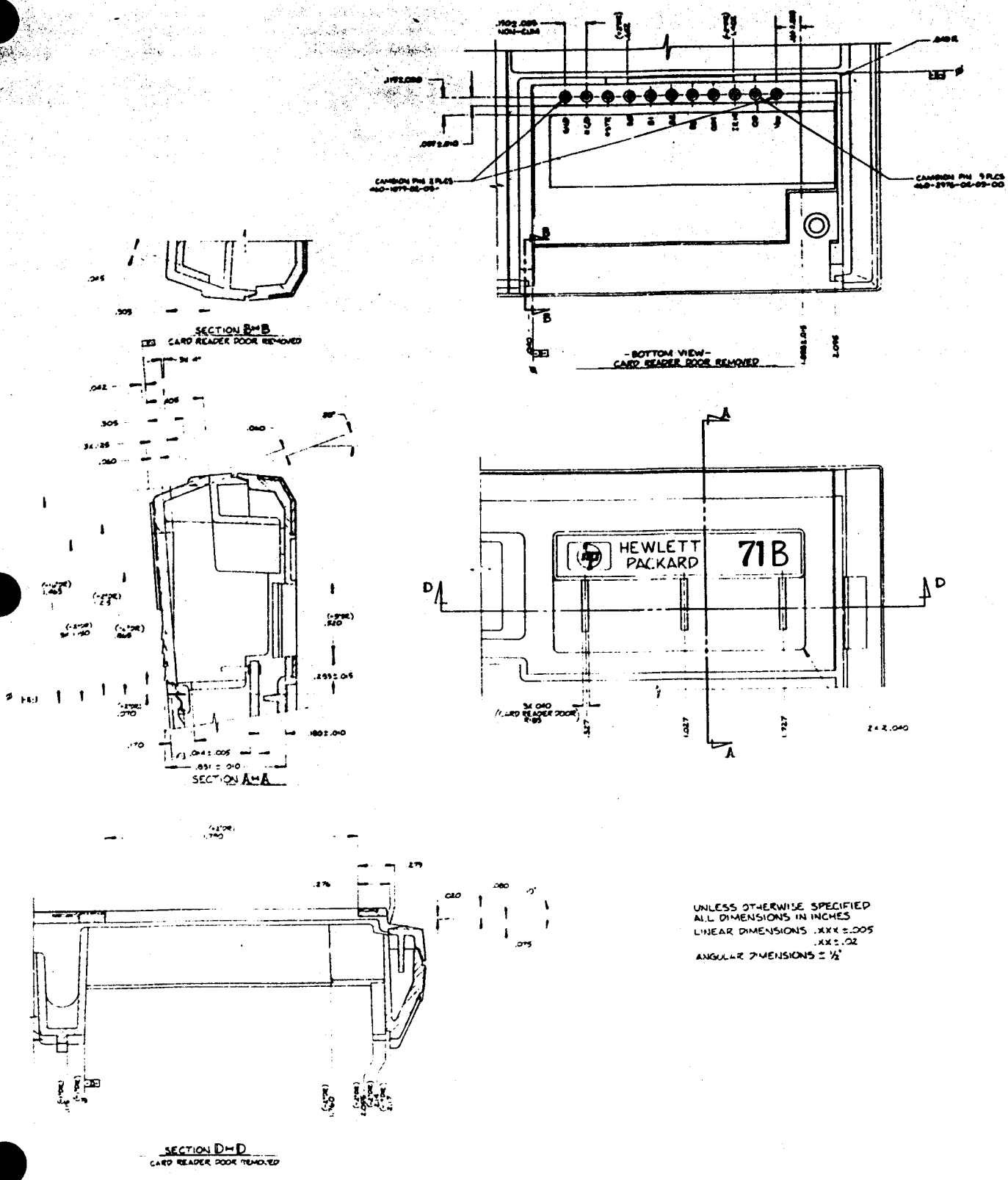

Figure 8-13. HP-71 Card Reader Port

SYSTEM ELECTRICAL SPECIFICATION	CHAPTER 9

IC ABSOLUTE MAXIMUM RATINGS:

Supply Voltage Vdd	Vss + 7.5V
Maximum Voltage at any Input or Output	Vdd + 0.3V
Minimum Voltage at any Input or Output	Vss - 0.3V
Operating Free-Air Temperature	0C to +45C
Storage Temperature	-40C to +55C
Humidity	0 to 95% RH

TEST CONDITIONS: Test conditions are such that the following parameters are guaranteed for Vdd = 4.25V to 6.5V and Temperature = 0C to 45C unless a different supply voltage or temperature is noted.

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Vss	Ground	0.0	0.0	0.0	V	
Vdd	Supply voltage	4.25	-	6.5	V	
Iddop	Idd operating current	-	-	15.0	mA	Display on, CPU running, T0=1.5uS.
Iddls	Idd light sleep current	-	-	0.5	mA	Display on, CPU shutdown.
Iddds	Idd deep sleep current	-	-	50	uA	Display off CPU shutdown.

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
POWER SUPPLY						
Vac	AC adapter input voltage	9.0	-	14.0	V	See Note 1.
Vreg	AC adapter voltage at Vdd	5.6	-	6.5	VDC	
Iac	AC adapter current drain	-	-	30	mADC	Over mainframe requirements.
Vbat	Battery voltage at Vdd	4.25	-	6.0	VDC	Unregulated.
Ibat	Battery current drain	-	-	100	mADC	Over mainframe requirements.
BUS PARAMETERS						
Vih	Input logic level '1'	Vdd-.65	-	-	V	
Vil	Input logic level '0'	-	-	Vss+.65	V	
Voh	Output logic level '1'	Vdd-.5	-	-	V	
Vol	Output logic level '0'	-	-	Vss+.5	V	
Cout	Output capacitance drive capability (surplus)					
	BUS0-3	50	-	-	pF	See Notes 2 & 3.
	*CD,*STR	50	-	-	pF	See Notes 2 & 3.
	DIN	10	-	-	pF	With no pulldown, See Note 4.
	DIN	50	-	-	pF	With Rpd = 50Kohm, See Note 4.

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Ioh	High level output source current capability					
	BUS0-3	1.0	-	-	mADC	See Note 3.
	*CD,*STR	1.0	-	-	mADC	See Note 3.
	DIN	100	-	-	uADC	
Iol	Low level output sink current capability					
	BUS0-3	1.0	-	-	mADC	See Note 3.
	*CD,*STR	1.0	-	-	mADC	See Note 3.
	DIN	2	-	-	uADC	
Cin	Input capacitance loading					
	BUS0-3	-	-	300	pF	See Note 2.
	*CD,*STR	-	-	250	pF	See Note 2.
	*INT	-	-	1200	pF	
	IR14	-	-	250	pF	
	HALT	-	-	250	pF	
	OD	-	-	.012	uF	
Iih	High level input current loading					
	BUS0-3	-	-	50	uADC	Internal pulldown
	*CD	-	0.0	-	uADC	Internal pullup
	*STR	-	0.0	-	uADC	Internal pullup
	*INT	-	0.0	-	uADC	10K pullup
	IR14	-	-	50	uADC	Internal pulldown
	HALT	-	-	1.0	mADC	10K pulldown
	OD	-	-	50	uADC	Internal pulldown

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Iil	Low level input current loading					
	BUS0-3	-	0.0	-	uADC	Internal pulldown
	*CD	-	-	50	uADC	Internal pullup
	*STR	-	-	50	uADC	Internal pullup
	*INT	-	-	1.0	mADC	10K pullup
	IR14	-	0.0	-	uADC	Internal pulldown
	HALT	-	0.0	-	uADC	10K pulldown
	OD	-	0.0	-	uADC	Internal pulldown

BUS TIMING PARAMETERS

T0	*STR cycle time	1.0	-	-	us	Current HP-71's operate at 600KHz to 650KHz, future HP-71's will run at up to 1MHz.
Tpwl	*STR low	0.5	-	-	us	
Tpwh	*STR high	0.5	-	-	us	
Tdwc	Data-in valid to *STR high	200	-	-	ns	Command cycle
Tdwd	Data-in valid to *STR high	100	-	-	ns	Write cycle
Tdh	*STR high to data-in invalid	100	-	-	ns	
Tacc	*STR low to data-out valid	-	-	200	ns	BUS precharged low
Toh	*STR high to data-out tristated	20	-	100	ns	

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Tc1	*CD low to *STR low	30	-	-	ns	
Tc2	*STR high to *CD high	50	-	-	ns	
Tc3	*CD high to *STR low	100	-	-	ns	
Tr	Rise time					
	*STR	-	-	100	nS	
	*CD	-	-	100	nS	
	BUS0-3	-	-	100	nS	
Tf	Fall time					
	*STR	-	-	100	nS	
	*CD	-	-	100	nS	
	BUS0-3	-	-	100	nS	

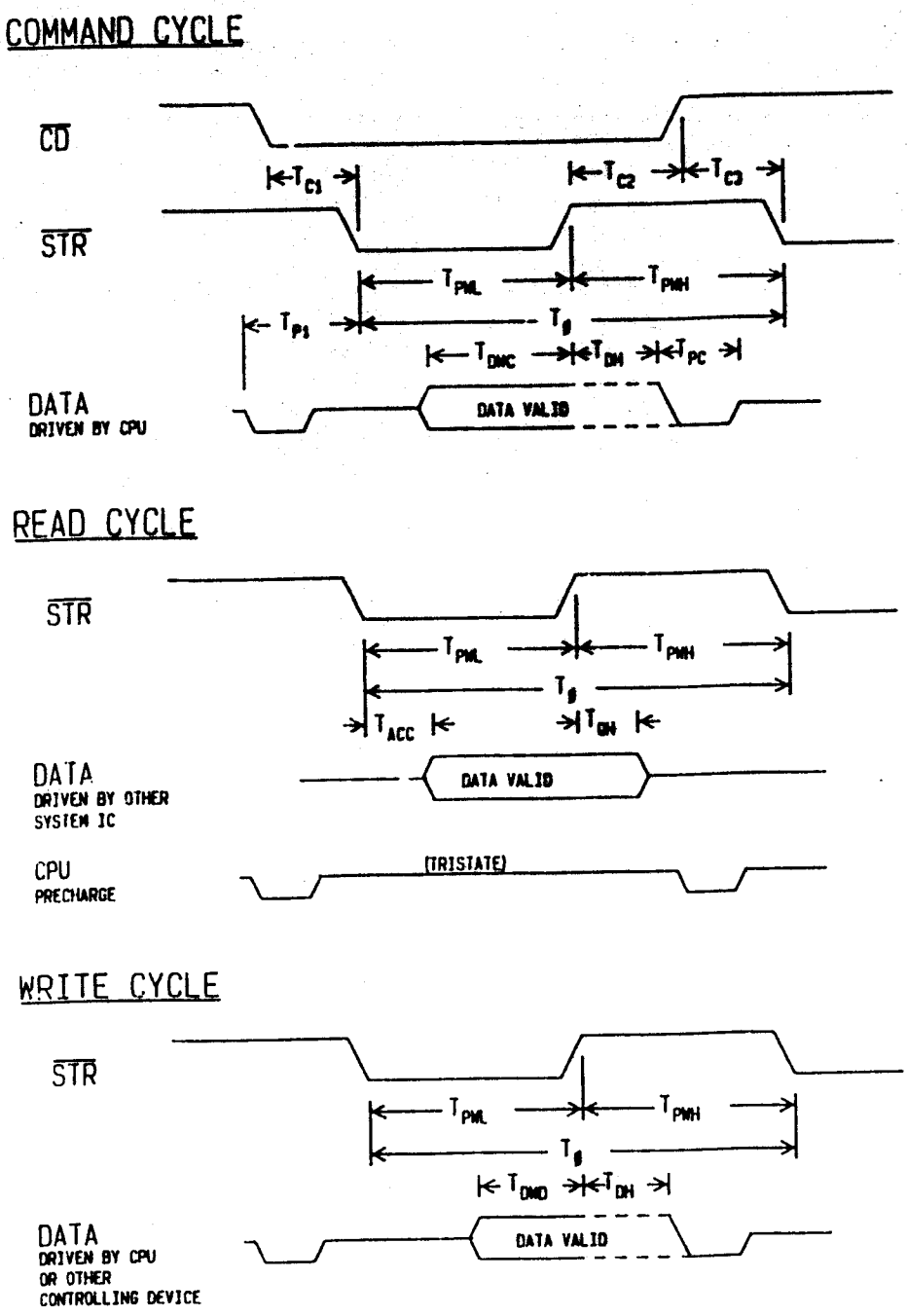

Figure 9-1. Bus Timing Relationships

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Fclk	Display *CLK frequency	-	512	-	Hz	+- 40 PPM Real time base.
LOW BATTERY INDICATION						
Vlbi	Low battery trip point	4.3	-	4.5	V	Low battery bit high when Vdd < Vlbi.
Vdta	Vlbi - Very low battery trip point	.08	-	.12	V	Very low battery bit high when Vdd < Vlbi-Vdta.

NOTES :

1) The values specified for Vac limit the peak voltage that may be applied between the 2 AC adapter input pins. This voltage may be either an AC peak voltage or a DC voltage. If a voltage less than 9.0V is applied the unit's batteries may be discharged. This minimum value for Vac (9.0V) can be reduced to 7.5V if the batteries are removed from the unit.

2) The values specified under Cout and Cin for BUS0-3, *CD, and *STR allow for 100pF loading by plug-in modules. This can be broken down as:

   a) RAM or ROM modules = 20pF x 4
   b) HP-IL module = 12pF
   c) Card reader module = 8pF

   A HP-71B with no plug-in modules could drive 100pF more than specified and would load these lines 100pF less than specified.

3) Reduce Cout (output capacitance drive capability) by 25 pF/mA of the larger of Ioh and Iol (high level source and low level sink current capability) required of BUS0-3, *CD, and/or *STR. Under no condition should the minimum current capability specified for Ioh and Iol be exceeded.

4) The DIN lines of the I/O ports are driven by the CPU output register (OR). The OR lines are also used to form the keyboard matrix and therefore excessive loading of a DIN line will prevent proper keyboard operation. The maximum capacitive loading of a DIN line may be increased to 50pF if a pulldown resistor, Rpd, of 50 Kohm (+-10%) is tied from DIN to ground. For most of the time when the HP-71 is turned on all lines of the OR are high and thus Rpd will draw current. When the HP-71 is shut off the operating system sets OR0 high and all other OR lines low. OR0 drives the DIN line of Port 1.

Portable Computer Division
1000 N.E. Circle Blvd., Corvallis, OR 97330, U.S.A.

European Headquarters
150, Route du Nant-D'Avril
P.O. Box, CH-1217 Meyrin 2
Geneva-Switzerland

HP-United Kingdom
(Pinewood)
GB-Nine Mile Ride, Wokingham
Berkshire RG11 3LL

00071-90071 English

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