Compact Digital Cassette Drive for Low-Cost Mass Storage

This portable battery-operated unit uses minicassettes to store programs and data inexpensively for HP-IL systems.

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THE HP 82161A Digital Cassette Drive (Fig. 1) is a portable, programmable, mass storage peripheral for the Hewlett-Packard Interface Loop (HP-IL).[1] The storage medium is a removable minicassette that can store up to 128K bytes of information. Portability is achieved by the use of a four-cell nickel-cadmium battery pack, recharger, and power supply system similar to that used in other portable HP products. The 82161A is styled to fit in a family of compact peripheral devices such as the 82143A and 82162A Printer/Plotters, and to fit nicely in a system controlled by an HP-41 Handheld Computer or an HP-75 Portable Computer. The 82161A makes use of much of the package design of the 82143A Printer/Plotter,[2] producing a unit 178 mm wide by 133 mm deep by 57 mm high. Replacing the 82143A's printer mechanism on the top right side is a transport mechanism with a **REWIND** key and a door **OPEN** key located in front. To the left of these keys is the power switch and indicators **POWER**, **LOW BATTERY**, and **BUSY**. The top left side of the package offers a compartment to store two minicassettes. The two HP-IL cables and the recharger cable are connected to the 82161A via plug receptacles on its back panel.

Electronic System

Fig. 2 is a block diagram of the electronic system of the 82161A. An internal microcomputer controls the head and motor drive electronics for the transport assembly and interacts with the HP-IL interface logic and data buffers.

The criteria for microcomputer selection for the 82161A included low cost, ready availability, low power consumption, and adequate I/O. To limit the number of electrical parts in the 82161A, a microcomputer that also contained ROM, RAM, and a timer, and could generate the encoded bit timing during a write operation was needed. A 3870 microcomputer with 2K bytes of ROM and 64 bytes of RAM was selected.

The logical interface of the 82161A is a generalized mass storage driver that provides the capability to execute operations such as initializing the tape, seeking a record, reading or writing a record, and rewinding the tape (see Table I).

Fig. 1. *The HP 82161A Digital Cassette Drive is a compact battery-operated mass-storage unit designed for use in portable HP-IL systems.*

Table I
HP 82161A Digital Cassette Drive Commands

DDL0	Write buffer 0	DDT0	Read buffer 0
DDL1	Write buffer 1	DDT1	Read buffer 2
DDL2	Write	DDT2	Read
DDL3	Set byte pointer	DDT3	Read address
DDL4	Seek	DDT4	Exchange buffers
DDL5	Format	DDT5	Transfer buffer 0→1
DDL6	Partial write		
DDL7	Rewind		
DDL8	Close record		
DDL9	Transfer buffer 0→1		
DDL10	Exchange buffers		

Buffer space for two 256-byte records of data is provided. Buffer 0 is used for data transfers between the HP-IL and the minicassette tape, and buffer 1 can be used by the HP-IL controller as virtual memory. The intent is to provide space to store a page of the tape directory and thereby reduce the number of seeks to the directory at the beginning of the tape. The DDL3 (set byte pointer), DDL8 (close record), and DDL6 (partial write) commands allow a memory-limited controller such as the HP-41 Handheld Computer to modify parts of a record without having to buffer the entire record in its mainframe. The record is read into buffer 0, modified, and written back to the tape with only the modification information passing around the HP-IL.

The ability to use the 82161A for extended remote data gathering tasks has been enhanced by the addition of the power-up/down commands. When the power switch on the front-panel keyboard is in the **STANDBY** position and a loop-power-down (PWRDN) command is received, the drive's power supply is turned off. When the HP-IL controller requires the loop to be active again, it sends a string of identify message frames, which turns the drive's power supply back on.

Software

The 2K bytes of machine code in the ROM of the microcomputer can be divided into three major areas: the power-on idle routine, the HP-IL routine, and the device control routines. The power-on idle routine, which uses approximately 160 bytes of code, sets up the initial state of the 82161A at power on and then alternates between testing for a cassette to be inserted into the drive, the **REWIND** key to be pressed, and calling the HP-IL routine. This routine also executes the device-clear and power-down functions. If either command is received, the HP-IL routine flags that fact and the drive responds after it finishes its latest task and returns to the idle routine loop.

The HP-IL routine, which takes approximately 460 bytes, provides the 82161A with basic talker and listener capabilities. This routine takes care of all communication with the HP-IL interface chip and passes all necessary information to the device control routines, primarily through a set of flag registers and one data register. This polled solution to HP-IL, in contrast to an interrupt-driven solution, is required because most of the device control routines need exclusive use of the microcomputer and can only give up control at specific times.

The device control routines, which take the remaining 1420 bytes of ROM, can be further divided. One part is the command decode portion. The device control is done with device-dependent commands (DDCs). When the HP-IL routine receives a DDC that it decides is of interest to the 82161A, it passes the DDC on to the command decode routine. Either the command is executed immediately, as in the case of a read or exchange buffer operation, or flags are set to control future actions, such as write and set byte pointer where the flags control where data bytes are put. A one-byte command buffer is used to hold a DDC received when the drive is busy. The HP-IL ready-for-command (RFC) message frame following this command is not retransmitted until the present task has been completed and the new command has been decoded.

The DDL5 (format) command initializes the record positions on the tape by recording all 512 records on both tracks. Each record contains a sync byte, a byte for the record number, a second sync byte, 256 bytes of data (each data byte initialized to 255), a checksum, and a final sync byte. Only during initialization is the first sync byte and the record number written. In all following write operations, the record number is read before the remaining part of the

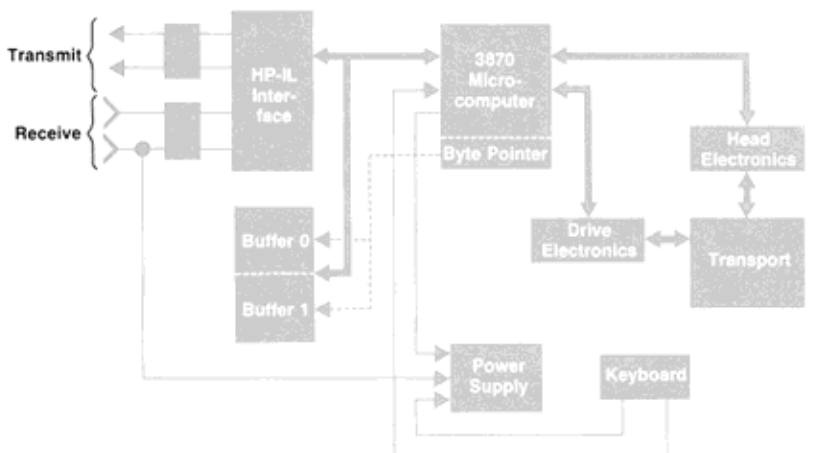


Fig. 2. *Block diagram of electronic system of the 82161A Digital Cassette Drive.*

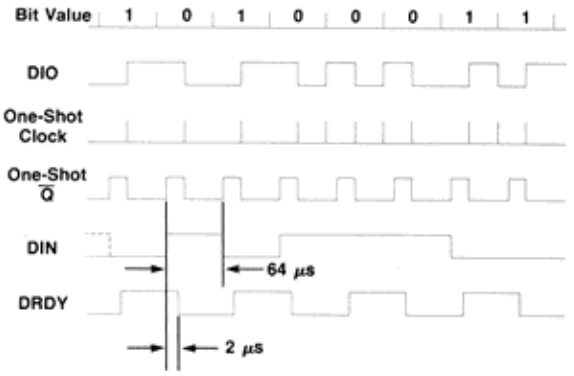


Fig. 3. *Timing diagram for signal lines and one-shot multivibrator states used to decode bit values stored on the 82161A tape cassette.*

record is written. This serves two purposes. The first is to verify that the proper record is being written and the second is to fix the record position on the tape so that it does not move along the tape when it is overwritten.

The major criterion in selecting an encoding method for the 82161A was reliability. The tape drive system requires that the method have a large speed-variation tolerance and use a microcomputer to generate the encoded bit stream during a write operation. The tape lengths required to record a one and a zero should be the same so that the length of a record does not depend on the ratio of ones to zeros within the record. Also, the code should be self-clocking for easy decoding.

The method best qualified is the biphase-level or Manchester code. The rules of this code are 1) there is always a transition in a bit cell center, and its direction specifies the value of the bit, and 2) there is a transition on a bit cell edge only when the two bits on either side have the same value (see Fig. 3).

In a write operation, the time between transitions, bit cell midpoint to bit cell edge, is 64 μs. During this time the transport status (stall, cassette present, and end of tape) is checked, the next nibble is read from the buffer and added to the checksum, and the next transition is calculated. The bit stream generated is sent to the sense amplifier on the DIO line.

There are two signals used in a read operation, DIN (data in) and DRDY (data ready). DRDY is the extracted clock and DIN is the latched data derived from the signal read from the tape. The microcomputer reads DIN and DRDY simultaneously and checks for DRDY to change state. When it does, the value of DIN is shifted into the register building the data. While it is in the read loop, the microcomputer also checks the transport status, stores the complete nibbles in the buffer, adds them to the checksum, and maintains a counter to detect when signal dropouts occur.

When the read/write routine is entered, the motors are turned on, the record number is read and verified, and the data portion of the record is then read or written. If a record number error and/or (in the case of a read) a checksum error is detected, the drive attempts the read or write operation a second time. If the microcomputer still detects an error, it stops the drive and reports the error to the HP-IL controller.

Seek operations are always attempted in a relative manner first. When the new record number is received, it is checked to see if it is in range (i.e., <512), and the difference between the present position and the desired position is calculated. The transport is turned on to move in the appropriate direction, and by watching the DRDY line, the microcomputer counts interrecord gaps until the transport reaches the record immediately before the desired record. This record is read, and the record number is checked. If it is correct, the transport is stopped with the desired record next. If an error is detected, the tape is rewound, and the seek is attempted again, but this time from the beginning of the tape. This gives four chances of reading the record correctly and ensures accurate seeks.

Data Storage and Retrieval

The microcomputer handles digital information to and from the read/write electronics on a bit-by-bit basis using three data-related lines (DIN, DIO, and DRDY, see Fig. 3) and two control lines (REC and TRK). DIO is a bidirectional data line whose transfer direction is controlled by the state of the REC line. In the read mode (REC low), DIO is driven by the sense amplifier, while in the write mode (REC high), the sense amplifier goes into a high-impedance state and DIO is driven directly by the microcomputer. Both DIN and DRDY are generated by the decoder circuitry and are derived solely from DIO level changes. The TRK line is driven by the microcomputer to select which tape track (0 or 1) is read from or written to.

The sense amplifier is a custom bipolar integrated circuit. It contains the signal conditioning and logic circuits to drive the magnetic head during a write operation and to translate the low-level analog signals at the head to time-related digital signals at DIO during a read operation.

Writing to the tape is accomplished by controlling the current flowing through the windings of the magnetic head. These currents produce a magnetic field across the gap at the front of the head. Three wires (two ends and a center tap) are attached to each winding (track) on the head. During a write operation, the center tap is connected to a constant-current sink, and each end of the winding is alternately driven high to control the direction of the current and thus the polarity of the magnetic field at the gap. The use of a current sink allows maximum rate of change of current, yet limits the peak direct current to 150% of that required to completely magnetize the tape.

During a read operation, the voltage at the terminals of the head is proportional to the rate of change of the magnetic flux across its gap and reaches a peak value when the gap is directly opposite a flux reversal on the tape. To decode recorded information properly, a digital signal with level changes corresponding in time to these voltage peaks must be generated. The sense amplifier generates this signal by amplifying and then differentiating the analog signal from the head. A zero crossing at the output of the differentiator corresponds to a peak of the amplified signal and is used to clock DIO level changes. The DIO level (high or low) is related to the polarity of the amplified signal at clock time and indicates the direction of the flux transition. Hysteresis is included to provide protection from unwanted transitions caused by electrical noise.

Data content is encoded by the direction of the DIO level transition at the midpoint of a bit cell. Transitions at bit cell edges are used only as required to set up DIO for the proper change at the next midpoint (see Fig. 3). The decoder hardware ignores these edge transitions and provides the microcomputer with two signals—DRDY and DIN. A change at DRDY notifies the microcomputer that the signal at DIN represents valid data.

For every DIO transition a 100-ns pulse is generated and appears at the trigger input of a nonretriggerable one-shot multivibrator. The timing period of the one-shot multivibrator is set so that, if triggered by a midcell transition, the next edge transition, when it exists, will occur during the cycle and thus be ignored. When the timing cycle expires, the level of DIO, which corresponds to the encoded bit value, is latched into the DIN flip-flop. Approximately 2 μs later, the output of the DRDY flip-flop changes, notifying the microcomputer that data is valid (see Fig. 3).

To ensure that the one-shot multivibrator is triggered only by midcell transitions and that it ignores any cell edge transitions, a sync byte is included at the beginning of each record. This special bit pattern maps to a stream of level changes that includes only midcell transitions. Thus, the one-shot multivibrator is set up to be triggered only at midcell, and, if speed stays within allowable limits, synchronization is maintained throughout the entire record.

The encoder hardware can tolerate timing variations in DIO of ±30%. Electronic jitter, aliasing, phase shift in the amplifiers, external electromagnetic noise, and true speed variations all contribute to the total timing variance at DIO. Fortunately, the wide acceptability range of the decoder easily overcomes these factors and ensures good unit-to-unit compatibility.

Transport Mechanism

The 82161A's mechanical design uses an 8 × 34 × 56 mm minicassette designed especially for digital applications. The cassette contains nominally 24 meters of usable tape 3.81 mm wide, allowing two tracks of data 1.45 mm wide. This tape is hub-driven as opposed to capstan-driven, meaning that the only way the tape can be moved is by turning the appropriate stack of tape directly.

The selection of a hub-driven cassette was the key step in a "simplicity" approach to the design of the 82161A mechanism. It allows the use of a two-motor drive (one per hub) and eliminates additional motors or controlled actuator devices that would be required by capstan mechanisms or single-motor drives. Another key to simplicity is the use of a two-track magnetic head. This eliminates having to move the cassette, either by the user or by a mechanism, to access both tracks. Other factors contributing to a straightforward design are the extensive use of injection-molded thermoplastics, cost-effective fasteners such as adhesives and press fits, and a low part count.

Aside from simplicity, another goal of this mechanism design was modularity. This produced a drive system module that can be removed from the 82161A and designed into other products with a minimum of change, electrical or mechanical.

The primary part of this device is the headframe assembly (Fig. 4). This assembly consists of a molded plastic frame into which a magnetic head is aligned and glued, and an optoelectronic device which forms half of the beginning-of-tape/end-of-tape (BOT/EOT) sensor. The single-gap, two-track head's coil winding parameters were chosen for both read and write functions. The headframe is molded from glass-filled polycarbonate, a very stable compound that allows some key dimensions to be held within a tolerance of 0.025 mm. Two posts on the headframe position the cassette housing relative to the head and two tape guides on the frame guide the tape relative to the head. These features are molded into the headframe.

The headframe assembly is joined with a door, window, and cassette pressure springs to form a door assembly very similar to that used in many conventional cassette tape recorders. The cassette is loaded into a slot in the door and the action of closing the door positions the cassette in the mechanism. When the door is released by pressing the **OPEN** key, a spring pulls it open so that the cassette can be easily removed.

When the door containing a cassette is shut, it pushes a pin, closing a switch spring located directly on the drive printed circuit assembly and informing the electronics that a cassette is present. A 45-degree mirror located within each cassette completes the optical BOT/EOT detection path. The optoelectronic device and the head in the headframe are connected to the drive's printed circuit assembly by a flexible ribbon cable.

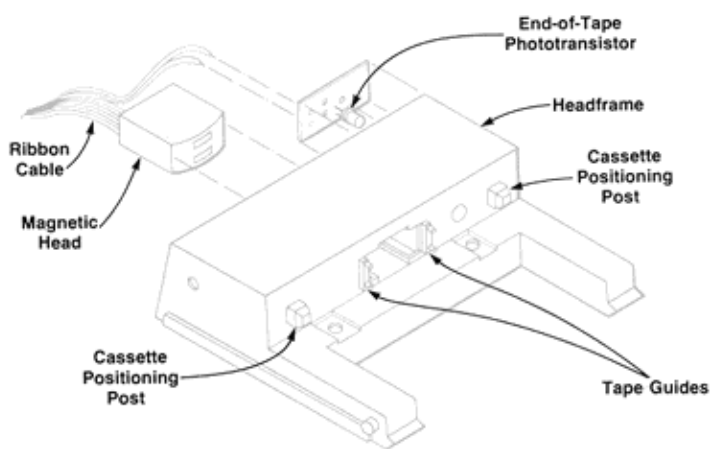


Fig. 4. *Exploded view of the 82161A headframe assembly.*

The backbone of the transport is the mainframe. It is a precision part made of glass-filled polycarbonate formed by injection molding. All of the key subassemblies, including the door/headframe assembly, the motors and gear systems, the door latch, and the printed circuit assembly are fastened to the mainframe to form a complete modular transport mechanism.

Two identical drive motors are used. One drives the left stack of tape and is called the forward motor. The other drives the right stack and is called the reverse motor. The use of two motors coupled directly to the tape stacks in this fashion makes possible a simple speed control scheme for reading and writing data. The motor selection involved a tradeoff between motor performance (hence cost) and product capability (primarily data capacity). Ironless-rotor motors with their low inertia/torque ratio were selected. The software definition requires interrecord gaps long enough to allow the tape velocity to change between zero and read/write speed between records. Selecting low-inertia motors allows record length to interrecord gap ratios of around 3:1. If higher-inertia motors had been used, this ratio, as well as data capacity, would have been lower. Another important characteristic of ironless-rotor motors in this application is their linear tachogenerator feature. The construction of the motors is such that their EMF, with the commutation ripple filtered out, can be used to detect motor speed changes typically within 2 percent. Perhaps the most important result of the selection of low-inertia motors is the reduction of dynamic tape tension. With the two-motor, hub-drive technique, the driving motor must pull the tape against the other motor's inertia. When accelerating, the trailing motor's inertia is multiplied by the square of the gear reduction as it is reflected into the tape. Hence, peak tape tensions are very sensitive to motor inertia. Tape life was found to be dominated by dynamic tape tensions and so the long tape life achieved in the 82161A is strongly related to the selection of low-inertia motors.

Motors could not be found that would go slow enough while maintaining the torque required to drive the tape hubs directly. Therefore, a speed reducer is required. Many methods were considered, beginning with the logical choice of motor/gearbox combinations, but these proved to be too expensive. O-ring and toothed-belt drive designs were tried, but both exhibited a common problem of requiring increased belt tension to avoid slipping. The higher belt tension produced higher shaft friction, which in turn, led to increased tape tension and reduced tape and bearing life.

The 82161A uses a custom gear drive (Fig. 5) consisting of a pinion and drive gear for each motor with a ratio of 1:4 (15 teeth to 60 teeth). Both gears are injection-molded at a custom gear-molding house and exceed AGMA* quality No. 7. The diametral pitch is 96 and the gear material is lubricated acetal resin. The pinions are pressed on the motor shafts and the drive gears run free on ground stainless-steel shafts pressed into the mainframe (Fig. 5a). The motors are positioned by concentric collars fastened also to the mainframe. Precision molding of the mainframe allows the motor-to-drive-gear-shaft dimension to be held to within 0.025 mm. Also running on the drive gear shafts, and axially coupled to the drive gears, are the drive splines (see Fig. 5b). These splines fit into the cassette hubs and transmit torque to them from the driven gears. In the event that a cassette hub does not align with the spline when the door is closed, the spline is spring-loaded and can be pushed down, allowing the door to shut. When that particular side of the drive moves, spline relative to hub, the spring pushes the spline up to engage it with the hub. These spline springs also produce a braking action or a drag friction. This drag was optimized for system speed performance by adjusting the spring constant and preload.

*American Gear Manufacturers' Association

Head Alignment

Accurate alignment of the magnetic head in the headframe is crucial to give unit-to-unit read/write compatibility for systems using multiple transports. This alignment is done electrically, with the head actually reading signals

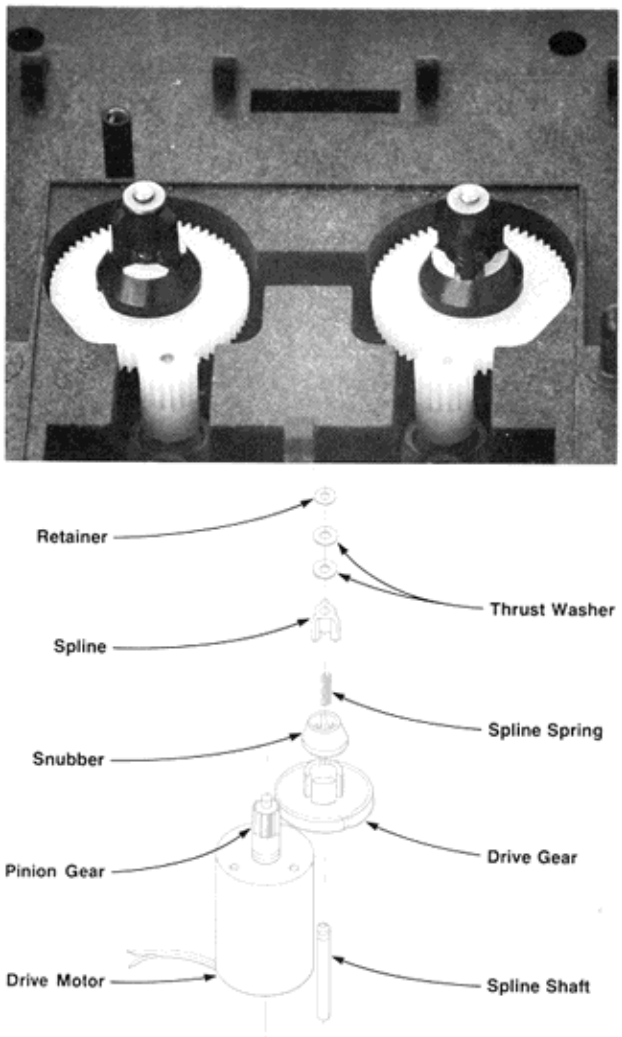


Fig. 5. *The tape drive system in the 82161A uses two identical motors, each driving a spring-loaded spline. (a) Close-up photograph of drive gear and motor assembly. (b) Exploded drawing of motor and drive gear system.*

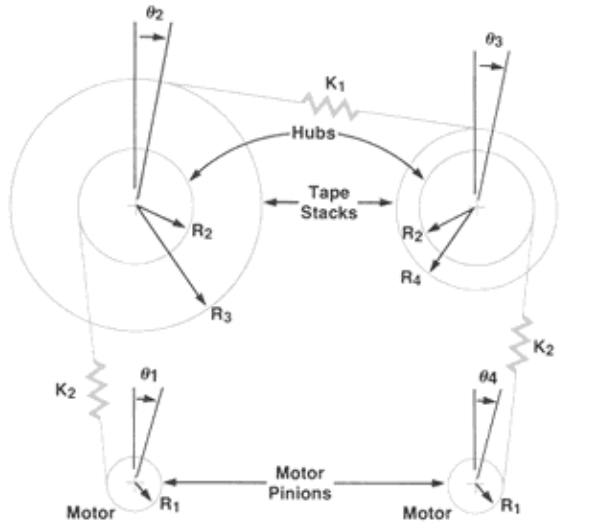
from two tracks simultaneously, rather than aligning optically as has been done by HP in the past.[3,4] The head aligner tool consists of an endless-loop tape deck, an oscilloscope, and an ac voltmeter. A master head on the tape deck is used to write perfectly phased signals on both tracks of a tape loop. This loop is then read by a head requiring alignment. The head is held inside a headframe by a tooling fixture that sets penetration and varies azimuth (perpendicularity of the head gap relative to tape motion) and tracking (vertical position of the head poles relative to tape position). The two signals read are observed on the oscilloscope and the azimuth is adjusted until both tracks are in phase and the combination of signals with maximum amplitudes has been found. This ensures that the azimuth has been "perfectly" aligned in the fixture. Next, the tracking is adjusted by moving the head up and down until the sum of the signals from both tracks is a maximum as measured by the voltmeter. This ensures that the pole spacing on the head optimally matches the track positions on the alignment tape. The two adjustments are practically decoupled on the alignment fixtures, so convergence is not necessary. After the head is aligned, the assembly and tooling fixture is removed, and the head is glued in place with a fast-curing acrylic adhesive. The headframe assembly can then be removed from its fixture and the alignment rechecked to observe any movement caused by glue cure. This procedure produces azimuth alignment better than ±5 arc-minutes, and tracking alignment, relative to the headframe, better than ±0.05 mm. The master head is periodically used to monitor the accuracy of the alignment tape. To check the master head, a Möbius tape is installed on the tape deck. This tape alternately presents front and back sides to the master head. A signal is written on the front side and read from the back side. The amplitude is reduced, but only the track-to-track phase is important. If the master head is "perfectly" aligned in azimuth, no phase difference will occur. An iterative process is used to align the master head if necessary.

System Modeling

The electromechanical system of the 82161A tape transport was modeled to allow studies of tape velocities and the effects thereon of motor parameters and mechanism inertias and frictions. The basic model is shown in Fig. 6 and the basic equations of motion are

$$
\begin{aligned}
I_1\Theta_1 &= R_1\left[K_2(R_2\theta_2 - R_1\theta_1)\right] \\
I_2\Theta_2 &= -R_2\left[K_2(R_2\theta_2 - R_1\theta_1)\right] + R_3\left[K_1(R_4\theta_3 - R_3\theta_2)\right] \\
I_3\Theta_3 &= -R_4\left[K_1(R_4\theta_3 - R_3\theta_2)\right] + R_2\left[K_2(R_1\theta_4 - R_2\theta_3)\right] \\
I_1\Theta_4 &= -R_1\left[K_2(R_1\theta_4 - R_2\theta_3)\right]
\end{aligned}
$$

This multi-degree-of-freedom system was studied by identifying different motor-to-tape-stack and motor-to-motor modes whose frequencies depend on the reduction method (belts or gears) and tape stack ratios. Many of the natural frequencies found by this model can be satisfactorily filtered out by altering the servo design, but one mode consistently showed up in the analysis that cannot. This was identified as a "tape mode" or the opposing oscillation of both hub stacks with the spring being the length of tape between the two stacks. During read/write operation, when the servo is controlling tape speed, this tape mode, if excited, is superimposed on the steady-state tape velocity and becomes what was found to be the major cause of tape speed jitter. In all of the configurations studied, this jitter frequency is near 500 Hz. This tape mode cannot be effectively corrected by the servo because it is totally isolated from the motors and hence is "invisible" to the servo. This tape mode creates oscillations in tape tension, but the magnitude of the oscillations was found to be less than the steady-state tape tension. Thus, the treatment of the tape as a linear spring was not negated by the fact that the tape cannot be put into compression. This phenomenon will be discussed further in reference to the slow-start circuitry in the motor drive.



θ_1 = Left motor position
θ_2 = Left stack position
θ_3 = Right stack position
θ_4 = Right motor position
I_1 = Motor inertia
I_2 = Left-hub-and-tape-stack inertia
I_3 = Right-hub-and-tape-stack inertia
K_1 = Connecting tape stiffness
K_2 = Gear mesh stiffness
R_1 = Pinion radius
R_2 = Hub radius
R_3 = Left stack radius
R_4 = Right stack radius

Fig. 6. *Diagram defining tape motor drive parameters used to model 82161A transport system behavior.*

The tape mode oscillations would not be a major difficulty if there was no 500-Hz excitation in the mechanism to get them going. Unfortunately, because of the size of the transport, the gear pitch selection was limited, and 500-Hz perturbations caused by gear backlash are unavoidable. Hence, two methods are used to damp the tape mode. First, friction is added by using the spline spring as described previously, and second, viscous rubber snubbers are added between the drive gear and the spline (see Fig. 5). In this position, the snubbers serially provide a viscoelastic element between the perturbation (gear backlash) and the elements (the cassette stacks) producing the tape mode oscillations. The combination of these two damping schemes reduces speed jitter by approximately 50% to a range of 10% of average tape speed.

Motor Drive

The 82161A mechanism combines software, electronics, and mechanics to control both the position and the velocity of the tape. TTL-compatible inputs to the motor drive circuitry allow the microcomputer to select any of five possible modes of operation.

The fast forward and rewind modes move the tape at 76 to 152 cm/s, during which time the microcomputer counts interrecord gaps to determine tape position (record number). Once the desired position has been reached, the slow forward mode is activated for a data read/write operation. Forward and reverse braking is accomplished by using the back EMF of the trailing motor to generate a reverse torque to decelerate the system.

The fast forward, rewind, and slow forward modes use the leading motor as the actuator and the trailing motor is "pulled" by the tape. The no-load friction of the trailing motor and its associated gears provides tape tension to aid speed control and help keep the tape in contact with the magnetic head. The forward and reverse braking modes use the trailing motor as the actuator and the tape as the mechanical link to decelerate the leading motor.

The heart of the motor drive electronics is the velocity control circuitry (Fig. 7). To ensure read/write compatibility, linear tape velocity past the magnetic head must be a controlled, repeatable function of tape position. Although holding the angular velocity of one motor constant would satisfy this objective, tape capacity would be severely limited because the linear tape speed would vary over a wide range as the radii of the takeup and supply reels, respectively, increase and decrease. However, holding the sum of the angular velocities of both motors constant not only satisfies the above requirements, but dramatically increases data capacity by maintaining a more uniform linear tape velocity.

The input to the servo is a controllable reference voltage. The servo acts to hold the sum of the back EMFs of the two motors equal to this reference. As shown in Fig. 7, the forward transfer path consists of an error amplifier, a power stage, and the mechanical system. The back-EMF summer forms the feedback path. All necessary frequency compensation is implemented in the error amplifier and includes a pole at the origin to integrate out dc errors, a low-frequency zero at 4 Hz to compensate a pole of the mechanical system, and a second pole at ≈40 Hz to filter out unwanted motor commutation noise that appears in the feedback signal. At frequencies within the range of interest (40 Hz), the open-loop transfer function of the system, including compensation, consists of a single pole at the origin. Local feedback for the error amplifier is derived from the output of the power stage to minimize crossover distortion. As discussed earlier, the transfer function of the mechanical system is quite complex and includes several oscillatory modes. Fortunately, these modes are either at frequencies well outside the bandwidth of the servo or are invisible to the servo so that no serious electronic stability problems arise.

A novel feature of this servo is the speed sensor which sums the back EMF from each motor. Since no current flows through the trailing motor, the back EMF is simply its terminal voltage and is readily available to determine motor speed. However, the current required to produce drive torque generates a voltage across the rotor resistance of the leading motor which is superimposed on its back EMF. In the past, this speed measurement problem has been avoided by using either pulse-width modulators, which sample back EMF by momentarily removing power, or transducers which do not rely on back EMF. For this application, low-frequency pulse-width modulators would dissipate additional power in the motor and generate electrical and mechanical noise caused by their switching transients. Transducers are too expensive, too large, and require too much additional hardware.

The chosen scheme dynamically sums the terminal voltage of each motor and subtracts the voltage caused by the drive currents in the leading motor. Referring to Fig. 7,

$$V_0 = EMF_L + I_M R_M - \left[(EMF_L + I_M R_M + I_M R_S) - (EMF_L + I_M R_M)\right](R3/R2) + \left[(EMF_L + I_M R_M) - (EMF_L + I_M R_M - EMF_T)\right](R3/R1)$$

If R1=R3, and canceling terms,

$$V_0 = EMF_L + I_M R_M - I_M R_S (R3/R2) + EMF_T$$

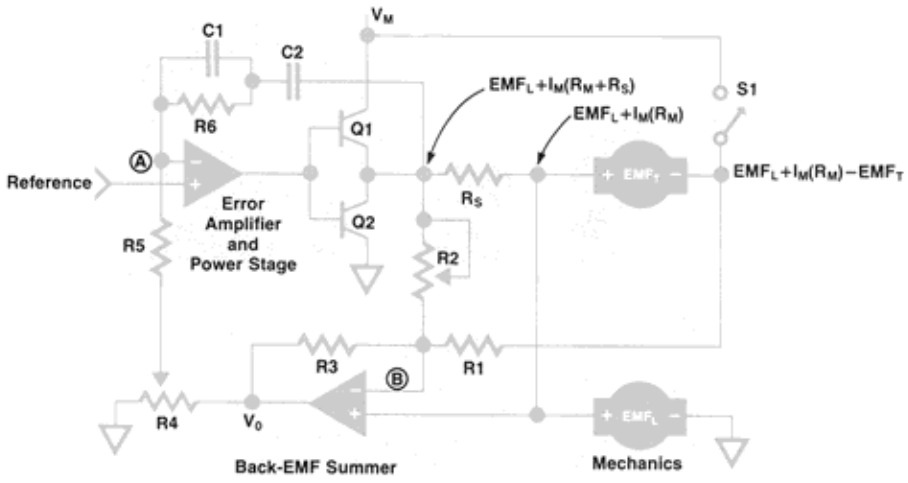


Fig. 7. *Simplified schematic of velocity control servo.*

Then, if R2 is adjusted such that $R_M/R_S=R3/R2$,

$$V_0=EMF_L+EMF_T$$

As can be seen from the derivation above, if resistance matching is done (using potentiometer R_2), the output of the feedback amplifier is the true sum of the back EMF of the motors. R_S is specified as a copper wirewound resistor so that its temperature coefficient of resistivity will match that of the motor's ironless rotor, thus holding the ratio of R_M to R_S constant and ensuring consistent speed control over the full operating temperature range.

The fast forward and rewind modes are implemented by "fooling" the servo. Grounding point A in Fig. 7 eliminates the feedback and causes the output of the error amplifier to go high and drive the motor at high forward speed. Forcing point B low causes V_0 to be high, thus forcing the output of the error amplifier low. This, in combination with closing switch S1 and lifting the ground on the leading motor (using transistor switches), results in the rewind mode.

To use the feedback from both motors to control speed, it is essential that the motors be mechanically linked in a predictable, linear fashion. In the 82161A, this link is the tape. Because the tape cannot support compressive forces, slack in the tape can occur and totally uncouple the leading and trailing motors. The typical result is a "bang-bang" servo action. The leading motor is driven until its back EMF equals the reference value. Suddenly the tape slack is taken up and the trailing motor begins to move and injects a step function into the feedback signal. The error amplifier responds by slowing the leading motor, which allows the trailing motor to spool up and form another loop. This starts the process all over again.

Once the 82161A has attained stable slow forward operation, this problem is prevented by the tape tension generated by system friction. However, when the slow-forward mode is initiated, there is always some amount of slack in the tape, and this slack must be eliminated first before accelerating to full speed. In addition, since overshoot can cause the same problem, the rate of change of the speed reference voltage must be slowed to the point where the servo can keep up.

The slow-start circuit performs these functions by controlling the reference voltage to the servo. When the slow forward mode is selected, the reference is held to a low value for approximately 130 ms, during which time the slack is removed from the tape. Then, the reference voltage rises exponentially towards an asymptotic value, allowing a smooth acceleration to read/write speed without overshoot.

Acknowledgments

The authors would like to thank Roger Quick and Tom Braun for their direction and leadership in the development of the 82161A, and George Custer for the product package design, head sourcing, and innumerable other design details. Also greatly appreciated is the work of Mark Matsler in developing the head alignment process, and the hard work of everyone else who helped bring the 82161A Digital Cassette Drive to production.

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