HEWLETT-PACKARD JOURNAL

The 'Powerful Pocketful': an Electronic Calculator Challenges the Slide Rule

This nine-ounce, battery-powered scientific calculator, small enough to fit in a shirt pocket, has logarithmic, trigonometric, and exponential functions and computes answers to 10 significant digits.

By Thomas M. Whitney, France Rodé, and Chung C. Tung

WHEN AN ENGINEER OR SCIENTIST NEEDS A QUICK ANSWER to a problem that requires multiplication, division, or transcendental functions, he usually reaches for his ever-present slide rule. Before long, however, that faithful 'slip stick' may find itself retired. There's now an electronic pocket calculator that produces those answers more easily, more quickly, and much more accurately.

Despite its small size, the new HP-35 is a powerful scientific calculator. The initial goals set for its design were to build a shirt-pocket-sized scientific calculator with four-hour operation from rechargeable batteries at a cost any laboratory and many individuals could easily justify. The resulting nine-ounce product surprises even many who are acquainted with what today's large-scale integrated circuits can achieve.

The HP-35 has basically the same functions and accuracy of other HP calculators, and it is portable. It is a close cousin to the many four-function electronic calculators which have appeared in recent years, initially from Japan and now from many U.S. manufacturers. However, three features set the HP-35 apart from four-function calculators. First, none of the four-function calculators has transcendental functions (that is, trigonometric, logarithmic, exponential) or even square root. Second, the HP-35 has a full two-hundred-decade range, allowing numbers from 10^{-99} to $9.999999999 \times 10^{+99}$ to be represented in scientific notation. Third, the HP-35 has five registers for storing constants and results instead of just one or two, and four of these registers are arranged to form an operational stack, a feature found in some computers but rarely in calculators (see box, page 5). On page 7 are a few examples of the complex problems that can be solved with the HP-35.

Data Entry

The photograph of the calculator on this page shows how the keys are arranged. Numbers enter the display, which is also called the X register, from left to right exactly as the keys are pressed. Entry is entirely free-field, that is, digits will be displayed exactly as they are entered, including leading or trailing zeros.

The enter-exponent key, EEX, is used for entering numbers in scientific notation. For example, the number 612,000 may be entered as 6.12 EEX 5 or 612 EEX 3 or .0612 EEX 7 as well as 612000. The change-sign key, CHS, changes the sign of the man-

tissa or, if pressed immediately following EEX, the sign of the exponent. Mistakes during data entry can be corrected by use of the clear x key, CLx. A special key is provided for entering π.

Display

The display consists of 15 seven-segment-plus-decimal-point light-emitting-diode (LED) numerals. Answers between 10^{10} and 10^{-2} will always be displayed as floating-point numbers with the decimal point properly located and the exponent field blank. Outside this range the HP-35 displays the answer in scientific notation with the decimal point to the right of the first significant digit and the proper power of 10 showing at the far right of the display. To make the display more readable, a separate digit position is provided for the decimal point.

The display is always left justified with trailing zeros suppressed. For instance, the answer to $3 \div 4$ appears as .75 instead of 0.750000000.

Cover: *Our thanks to Dr. Dennis R. Clark of the Stanford University Department of Pharmacology for allowing us to photograph him at work with his HP-35 Pocket Calculator.*

In this Issue:

Answers greater than 10^{100} (overflow) are displayed as $9.999999999 \times 10^{99}$, and answers smaller than 10^{-99} are returned as zeros. These are the HP-35's 'closest' answers. Improper operations, such as division by zero or the square root of a negative number, cause a blinking zero to appear.

Single-Operand Function Keys

The function keys operate on the number displayed in the X register, replacing it with the function of that argument. The trigonometric functions, sin, cos, tan, arc sin, arc cos, and arc tan operate in degrees only. For inverse trigonometric functions the function key is preceded by the arc key. The angle obtained will be the principal value.

The functions log x and ln x compute the logarithm of x to base 10 and base e respectively. The exponential function e^x is also provided. Other single-operand functions are the square root of x, $\sqrt{x}$, and the reciprocal of x, 1/x.

Arithmetic Keys: Two-Operand Functions

The arithmetic functions, $+$, $-$, $\times$, and $\div$, and the power function x^y, operate on the X and Y registers, with the answer appearing in X. Numbers are copied from X into Y by use of the ENTER↑ key. Thus to raise 2 to the 7th power the key sequence is 7, ENTER↑, 2, x^y and the answer 128 is displayed immediately after x^y is pressed. This is a general principle: when a key is pressed, the corresponding operation is performed immediately.

Although raising x to a power can be accomplished via the formula $x^y = e^{y \ln x}$ and in fact is done this way internally, the single-keystroke operation is much more convenient. The power, y, can be any positive or negative integer or fraction, while x must be positive.

Registers and Control Keys

Five registers are available to the user. Four of these, called X, Y, Z, and T, form an operational stack. The fifth, S, is for constant storage. (For clarity, capital letters refer to the registers and lower-case letters refer to the contents of the registers.)

Five keys are used to transfer data between registers. The ENTER↑ key pushes the stack up, that is, x is copied into Y, y into Z, z into T, and t is lost. This key is used as a separator between consecutive data entries, such as in the power example just described. Roll down, R↓, is used to view the contents of X, Y, Z, and T. Four consecutive operations of this key return the registers to the original state with no loss of data.

		①	②	③	④	⑤	⑥	⑦	⑧	⑨
	T									
	Z						12	12		
	Y		3	3		12	5	5	12	
DISPLAY	X	3.	3.	4.	12.	5.	5.	6.	30.	42.
KEY ⟶		3	↑	4	×	5	↑	6	×	+
STEP NUMBER ⟶		①	②	③	④	⑤	⑥	⑦	⑧	⑨

① 3 in display (X register)

② 3 duplicated into Y register by ENTER↑

③ 4 in display.

④ Product (12) appears in X and stack drops.

⑤ Automatic ENTER↑ pushes 12 into Y. Display shows 5.

⑥ ENTER↑ pushes y into Z, x into Y. x is unchanged.

⑦ 6 in display.

⑧ Product (30) appears in X and stack drops.

⑨ Sum (42) appears in X and stack drops.

Fig. 1. *HP-35 Pocket Calculator has a four-register operational stack (last-in-first-out memory). Here's how the stack works to solve (3 × 4) + (5 × 6). Answers appear in display register X, in floating-point or scientific notation, to 10 significant digits.*

Fig. 2. *Instruction panel on back of calculator answers most frequently asked questions.*

The contents of X and Y can be exchanged using $x \rightleftarrows y$; this is useful if the operands have been entered in the improper order for x^y, $-$, or $\div$. The constant storage location, S, is accessed via the two keys store, STO, and recall, RCL.

The operational stack is automatically pushed up for data entries following any operation other than ENTER↑, STO, and CLx. This saves many uses of the ENTER↑ key. The stack automatically drops down following any two-operand function ($+$, $-$, $\times$, $\div$, x^y). For example, to do the problem $(3 \times 4) + (5 \times 6)$ the key sequence is: 3, ENTER↑, 4, ×, 5, ENTER↑, 6, ×, + (see Fig. 1). ENTER↑ is unnecessary between × and 5 because the answer to the first term, 12, is automatically transferred to Y when the 5 is entered. Also, no R↓ is necessary after the second × since the first term, 12, is automatically transferred from Z to Y after the multiplication.

The clear-all key, CLR, clears all registers including storage. Initial turn-on of the calculator has the same effect.

On the back of the calculator is an instruction panel that provides the user with quick answers to the most commonly asked 'how-to-do-it' questions (Fig. 2). The panel also shows an example of a problem solution.

System Organization

Now let's go inside and see what makes it work. The HP-35 contains five MOS/LSI (metal-oxide-semiconductor/large-scale-integration) circuits: three read-only-memories (ROMs), an arithmetic and register circuit (A&R), and a control and timing circuit (C&T). The logic design was done by HP and the circuits were developed and manufactured by two outside vendors. Three custom bipolar circuits are manufactured by HP's Santa Clara Division: a two-phase clock driver, an LED anode driver/clock generator, and an LED cathode driver. Fig. 3 is a block diagram of the calculator.

The HP-35 is assembled on two printed circuit boards (see Fig. 4). The upper board contains the display and drivers and the keyboard. The lower and smaller board has all the MOS logic, the clock driver, and the power supply.

The calculator is organized on a digit-serial, bit-serial basis. This organization minimizes the number of connections on each chip and between chips, thereby saving area and cost and improving reliability. Each word consists of 14 binary-coded-decimal digits, so each word is 56 bits long. Ten of the 14 digits are allocated to the mantissa, one to the mantissa sign, two to the exponent, and one to the exponent sign.

Three main bus lines connect the MOS circuits. One carries a word synchronization signal (SYNC) generated by a 56-state counter on the control and timing chip. On another bus, instructions (I_s) are transmitted serially from the ROMs to the control and timing chip or to the arithmetic and register

Operational Stacks and Reverse Polish Notation

In 1951, Jan Lukasiewicz' book on formal logic first demonstrated that arbitrary expressions could be specified unambiguously without parentheses by placing operators immediately before or after their operands. For example, the expression

$$(a + b) \times (c - d)$$

is specified in operator prefix notation as

$$\times + ab - cd$$

which may be read as multiply the sum a plus b by the difference c minus d. Similarly, the expression can be specified in operator postfix notation as

$$ab + cd - \times$$

with the same meaning. In honor of Lukasiewicz, prefix and postfix notation became widely known as Polish and reverse Polish, respectively.

During the following decade the merits of reverse Polish notation were studied and two simplifications in the execution of computer arithmetic were discovered. First, as reverse Polish notation is scanned from left to right, every operator that is encountered may be executed immediately. This is in contrast to notation with parentheses where the execution of operators must be delayed. In the above example, $(a + b) \times (c - d)$, the multiply must wait until $(c - d)$ is evaluated. This requires additional memory and bookkeeping. Second, if a stack (that is, a last-in-first-out memory) is used to store operands as a reverse Polish expression is evaluated, the operands that an operator requires are always at the bottom of the stack (last operands entered). For $(a + b) \times (c - d)$, the reverse Polish, $ab + cd - \times$, is evaluated as follows.

	T							
	Z					a + b		
↑	Y		a		a + b	c	a + b	
stack	X	a	b	a + b	c	d	c − d	(a + b) × (c − d)
Reverse Polish		Enter a	Enter b	+	Enter c	Enter d	−	×

These properties have made the notation a valuable tool in the computer industry. All modern computer compilers for languages such as FORTRAN and ALGOL convert statements to reverse Polish in some form before producing a program that can be executed. Some computer manufacturers have even designed their machines with special instructions to perform stack operations to facilitate execution of reverse Polish. However, the HP-35 is the first scientific calculator to fully exploit the advantages of reverse Polish and automatic stack operations to provide user convenience seldom found in calculators.

Control and Timing Circuit

The control and timing (C&T) circuit performs the major nonarithmetic, or housekeeping functions in the calculator. These include interrogating the keyboard, keeping track of the status of the system, synchronizing the system, and modifying instruction addresses.

The keyboard is arranged as a five-column, eight-row matrix. It is scanned continuously by the C&T chip. When contact is made between a row and a column by pressing a key, a code corresponding to that row and column is transmitted over the I_A line to the read-only memory (ROM). This code is the starting address of a program in ROM to service that key. Key bounce and lockout are handled by programmed delays.

In all digital systems, status bits or flags are used to keep track of past events. In the HP-35 there are twelve status bits, all located on the C&T chip. They can be set, reset, or interrogated by microinstructions.

ROM addresses are updated on the C&T chip and sent serially to the ROMs over the I_A bus. During execution of a branch instruction, the appropriate signal—arithmetic carry or status bit—is tested to determine whether the incremented address or the branch address should be selected next.

A powerful feature of the serial organization is the ability to operate on just a single digit of a number as it flows through the arithmetic unit. On the C&T chip are a pointer register and a word-select circuit which issue a word-select signal (WS) corresponding to the time slot being operated upon. The value of the pointer register can be set, incremented, and decremented by microinstructions.
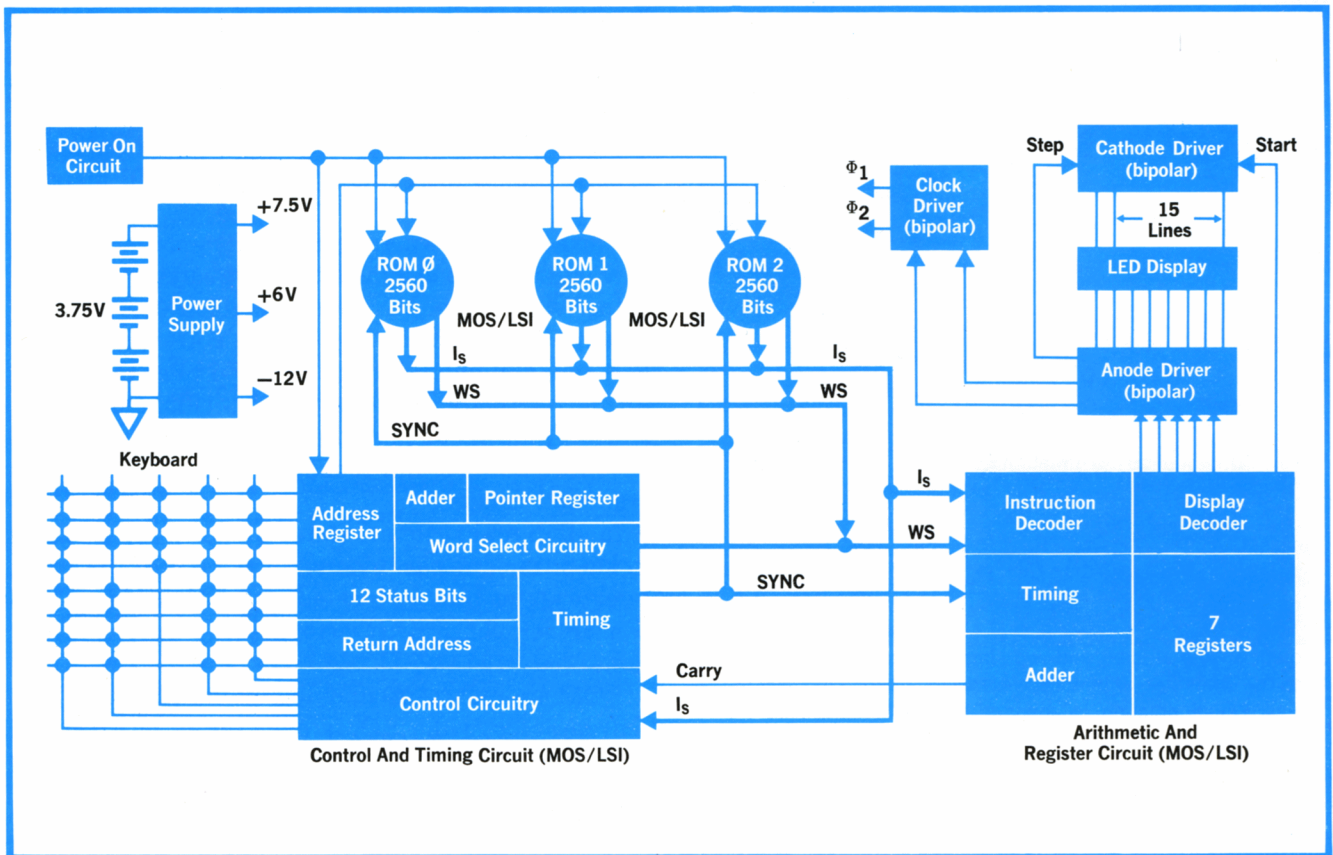
Read-Only Memory

Preprogrammed mathematical routines are stored in three ROM chips, each of which contains 256 instructions of 10 bits each. A specific select code is assigned to each ROM chip. Only one of the three ROM chips is used at any time. When a ROM selection instruction is issued, a decoder inside each ROM checks the select-code field of the instruction. In case of a match, the selected ROM turns on. Unselected ROMs turn off.

A timing circuit on each ROM is synchronized to the SYNC signal issued by the C&T chip as the calculator is turned on. This circuit then keeps the ROM chip running synchronously with the rest of the system.

A ROM address register on each ROM chip receives the address sent out by the C&T chip. The corresponding instruction is placed on the instruc-

chip. The third bus signal, called word select (WS), is a gating signal generated on the C&T chip or by the ROMs; it enables the arithmetic unit for a portion of a word time, thereby allowing operations on only part of a number, such as the mantissa or the exponent.

Fig. 3. *Five MOS/LSI circuits, developed by HP, are manufactured by outside vendors. Three custom HP-developed bipolar IC's are manufactured by HP. SYNC, I_s, and WS are three main bus lines connecting the MOS circuits.*

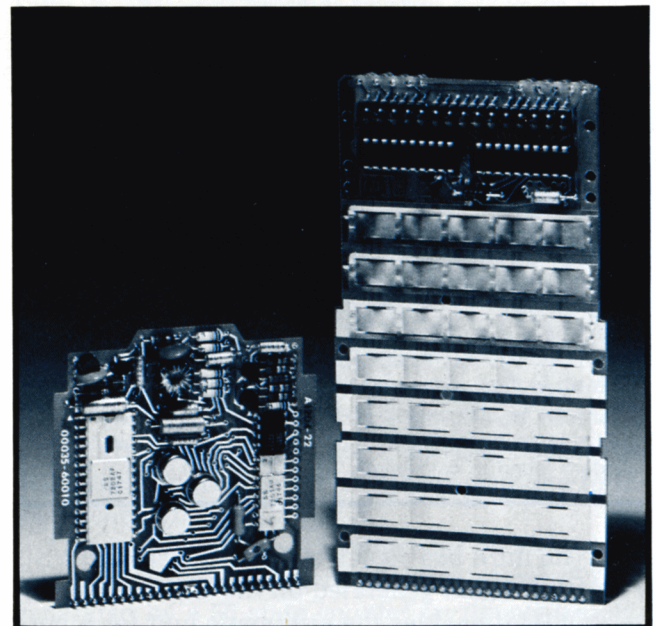tion line, I_s, provided the ROM chip is turned on.

The ROM chip also issues word-select signals for certain classes of instructions.

Arithmetic and Register Circuit

The arithmetic and register circuit executes instructions coming in bit-serially on the I_s line. Most arithmetic instructions must be enabled by WS, the word-select signal. Data to be displayed is sent to the LED anode drivers on five lines, and one carry line transfers carry information back to the C&T chip. The BCD output is bidirectional and can carry digits into and out of the A&R chip.

The A&R circuit is divided into five areas: instruction storage and decoding circuits, a timing circuit, seven 56-bit registers, an adder-subtractor, and a display decoder.

Three of the registers are working registers. One of these and three of the remaining four registers form the four-register stack. The seventh register is an independent register for constant storage. There are numerous interconnections between registers to allow for such instructions as exchange,
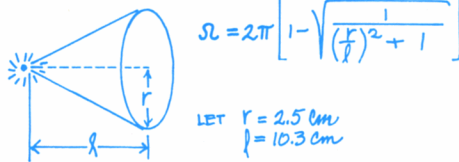

Fig. 4. *Two printed-circuit boards contain all circuits. Metal humps on the larger board are pressed down by the keys to make contact with printed traces underneath.*

6

How the HP-35 Compares with the Slide Rule

These comparisons were made by engineers who are not only highly proficient in slide rule calculation, but were also familiar with the operation of the HP-35. Thus, the solution times should not be taken as typical. They do, however, serve to indicate the relative time advantage of the HP-35 and to point up the still more significant advantage of its accuracy.

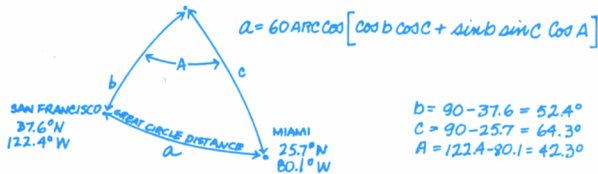*PROBLEM 1: COLLECTION SOLID ANGLE FROM A POINT SOURCE.*

$$\Omega = 2\pi \left[1 - \sqrt{\frac{1}{\left(\frac{r}{\ell}\right)^2 + 1}} \right]$$

LET $r = 2.5\,cm$
$\ell = 10.3\,cm$

HP-35 SOLUTION:

2.5 [÷] 10.3 [+] [+] [×] 1 [+] [1/x] [√x] [CHS] [+] 1 [+] 2 [×] [π] [×] → .1772825509

SLIDE RULE SOLUTION: .1776

TIME ON HP-35: 20 seconds with answer to ten significant digits.

TIME ON SLIDE RULE: 3 minutes, 15 seconds with answer to three decimal places.

PROBLEM 2: GREAT CIRCLE DISTANCE BETWEEN SAN FRANCISCO AND MIAMI.

$$a = 60 \text{ ARCCOS} \left[\cos b \cos C + \sin b \sin C \cos A \right]$$

SAN FRANCISCO 37.6°N 122.4°W   GREAT CIRCLE DISTANCE   MIAMI 25.7°N 80.1°W

$b = 90 - 37.6 = 52.4°$
$C = 90 - 25.7 = 64.3°$
$A = 122.4 - 80.1 = 42.3°$

HP-35 SOLUTION:

52.4 [cos] 64.3 [cos] [×] 52.4 [sin] 64.3 [sin] [×] 42.3 [cos] [×] [+] [arc] [cos] 60 [×] → 2254.093016

SLIDE RULE SOLUTION: 2255 mm.

TIME ON HP-35: 65 seconds with answer to ten significant digits.

TIME ON SLIDE RULE: 5 minutes with answer to four significant digits.

PROBLEM 3: pH OF A BUFFER SOLUTION.

$$\alpha_H = 1 + \sum C_B K_A, \quad H^+ = \sqrt{\frac{1}{\alpha_H} \sum \frac{C_A}{K_A}}$$

FOR A MIXTURE OF $Na_2 HPO_4$ @ $0.3\,m/\ell$ AND NaH_2PO_4 @ $8.7 \times 10^{-3}\,m/\ell$

$$\alpha_H = 1 + \left[3 \times 10^{-2} \right] \left(10^{7.21} \right) + \left[8.7 \times 10^{-3} \right] \left(10^{2.16} \right)$$

$$-H^+ = LOG \sqrt{\frac{1}{\alpha_H} \left(\frac{3 \times 10^{-2}}{10^{11.7}} + \frac{8.7 \times 10^{-3}}{10^{7.21}} \right)}$$

HP-35 SOLUTION:

7.21 [↑] 10 [xʸ] .03 [×] 1 [+] 2.16 [↑] 10 [xʸ] .0087 [×] [+] [STO] .03 [↑]
11.7 [↑] 10 [xʸ] [÷] .0087 [↑] 7.21 [↑] 10 [xʸ] [÷] [+] [+] [RCL] [÷] [√x] [log] → −7.47877778

SLIDE RULE SOLUTION: 7.43

TIME ON HP-35: 65 seconds with answer to ten significant digits.

TIME ON SLIDE RULE: 5 minutes with answer to three significant digits.

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transfer, rotate stack, and so on. An advantage of the bit-serial structure is that interconnections require only one gate per line.

Transfers into or out of the stack or the constant register are always whole-word transfers. All other arithmetic instructions are controlled by the word select signal, WS. Thus it's possible to interchange only the exponent fields of two registers, or to add any two corresponding digits of two registers.

The adder-subtractor computes the sum or difference of two decimal numbers. It has two data inputs, storage for carry or borrow, and sum and carry/borrow outputs. For the first three clock times, the addition is strictly binary. At the fourth clock time the binary sum is checked, and if the answer is more than 1001 (nine), then the sum is corrected to decimal by adding 0110 (six). The result is then entered into the last four bits of the receiving register and the carry is stored. A similar correction is done for subtraction. Carry information is always transmitted, but is recorded by the control and timing chip only at the last bit time of the word-select signal.

Simulation and Test of the MOS Circuits

In designing elaborate integrated circuits like the C&T, A&R, and ROM chips, two questions that have to be answered at the very beginning are: How is the design to be checked? and How is the final integrated circuit to be tested?

The first question has two answers. One is to build a breadboard and compare its operation with the desired operation. A second answer is a computer simulation of the circuit. When the MOS circuits (C&T, A&R, and ROMs) for the HP-35 were being designed, the computer simulation approach was chosen over a TTL or MOS breadboard. It was felt that the hardware breadboard wouldn't be an exact model of the final circuits anyway, and two or three months of development time could be saved by computer simulation because people could work in parallel rather than serially on a breadboard.
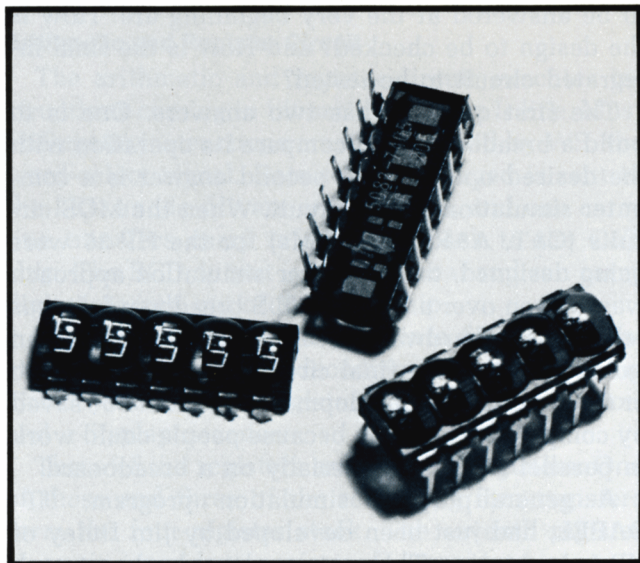
A general-purpose simulation program, HP-DABEL, had just been developed by Jim Duley of HP Laboratories. This was used to check out each gate, each circuit, each chip, and finally all the chips together. Each MOS circuit is designed as a network

of gates and delay elements. For each gate output an algebraic equation was written as function of the inputs to the gate. This produced a large set of algebraic equations to be evaluated every clock time. A printout was available so the operation of any of the gates or delay outputs could be observed, as if with an oscilloscope probe. In this respect the computer simulation was much better than a hardware breadboard.

Because of the large number of equations to be evaluated each clock time the general-purpose simulation program was too slow to use for evaluating the algorithms implemented in the ROMs. For this a higher-level simulation was used, so only the input/output functions of each subsystem had to be specified. This was fast enough that all the algorithms could be checked, even the transcendental functions. If anything went wrong it was always possible to stop the program and step through it until the trouble was found. Correcting a problem was a simple matter of changing a punched card or two. These are advantages a hardware breadboard doesn't have.

The simulation approach proved very successful. It saved a lot of time not only in logic design, but also in generating the test patterns to be used for testing the final integrated circuits. After a simulation is running successfully a pattern for each input is specified such that virtually every circuit element will be exercised. By running the program and recording all the inputs and outputs a complete test pattern is generated. This is recorded on tape, ready for final test of the IC.

Fig. 5. *Light-emitting-diode cluster was specially developed for the HP-35. Magnifying lenses are built in.*

Display and Drivers

It was apparent early in the HP-35 planning that new display techniques would be required. Existing light-emitting-diode products used too much power and cost too much. HP Associates developed a magnified five-digit cluster which saves both power and cost and is packaged in a convenient 14-pin package (Fig. 5). Each digit has a spherical lens molded in the plastic over it. A slight reduction in viewing angle results, but for the handheld calculator this is not a problem.

LED's are more efficient if they are pulsed at a low duty cycle rather than driven by a dc source. In the HP-35, energy is stored in inductors and dumped into the light-emitting diodes. This drive technique allows a high degree of multiplexing; the digits are scanned one at a time, one segment at a time.

Customized bipolar anode and cathode driver circuits incorporating the required features were developed and are manufactured by HP. The anode driver generates the two-phase system clock and the segment (anode) drive signals, decodes the data from the arithmetic and register chip and inserts the decimal point, sends shift signals to the other axis of the multiplex circuitry (the cathode driver), and senses low battery voltage to turn on all decimal points as a warning that about 15 minutes of operating time remains. The cathode driver contains a 15-position shift register which is incremented for each digit position.

Keyboard

Requirements for the HP-35's keyboard were particularly difficult. The keyboard had to be reliable, inexpensive, and low-profile, and have a good 'feel'. The solution is based on the 'oilcan' or 'cricket' principle, that is, curved metal restrained at the edges can have two stable states. The larger board in Fig. 4 shows the etched metal keyboard strips running horizontally. At each key location the metal is raised to form a hump over a printed-circuit trace running underneath. Depressing a key snaps the metal down to make contact with the trace. The keys have a definite 'fall-away' or 'over-center' feel so that there is no question when electrical contact is complete.

Acknowledgments

The many people who contributed to the HP-35 did so with great energy and enthusiasm. There was a feeling throughout the project that we had a tremendous winner. Appreciation is due the particularly important contributors below:

Tom Osborne for the initial product definition and continued guidance on what a calculator was and for whom it was intended.

Paul Stoft for providing technical direction and an environment where wild ideas can flourish and for keeping our unbounded optimism in check.

Dave Cochran for initial system design, algorithm selection, and sophisticated and clever microprogramming.

Chu Yen for a super-efficient power supply and work on the recharger/ac adaptor, with the able assistance of Glenn McGhee.

Ken Peterson for the automatic logic board tester and for devising novel methods to test the elusive dynamic MOS circuitry.

Rich Marconi and Charlie Hill for the design of the display board tester and to Rich for patience through many redesigns of the PC boards.

Bill Misson and Dick Osgood for an inexpensive, reliable and producible keyboard.

Clarence Studley and Bernie Musch for creative and durable packaging and for not yelling, 'There's no more room' too often.

Jim Duley, Margaret Marsden, and John Welsch for assistance in computer programs for test patterns, simulation, and microassemblers.

Ed Liljenwall for exceptionally creative industrial design work including the improbable result that 35 easily operated keys can exist in a three-by-five-inch area.

Tom Holden and Neil Honeychurch for providing a close liaison with the manufacturing division to speed the design of the fabricated parts.

And lastly to our behind-the-scenes project leader, Bill Hewlett, who initiated the project and kept the fires burning whenever needed. 🗲

Thomas M. Whitney
Tom Whitney holds BS, MS, and PhD degrees in electrical engineering, all from Iowa State University, received in 1961, 1962, and 1964, respectively. With HP Laboratories since 1967, he has served as digital systems section leader and as section manager for the HP-35 Pocket Calculator. He's also a lecturer at Santa Clara University, currently teaching a course in microprogramming. Away from electronics, Tom spends as much time as possible outdoors, with skiing, tennis, and camping the major activities.

France Rodé
France Rodé came to HP in 1962, designed counter circuits for two years, then headed the group that developed the arithmetic unit of the 5360 Computing Counter. He left HP in 1969 to join a small new company, and in 1971 he came back to HP Laboratories. For the HP-35, he designed the arithmetic and register circuit and two of the special bipolar chips. France holds the degree Deploma Engineer from Ljubljana University in Yugoslavia. In 1962 he received the MSEE degree from Northwestern University. When he isn't designing logic circuits he likes to ski, play chess, or paint.

Chung C. Tung
Chung Tung received his BS degree in electrical engineering from National Taiwan University in 1961, and his MSEE degree from the University of California at Berkeley in 1965. Late in 1965 he joined HP Laboratories. He was involved in the design of the 9100A Calculator and was responsible for the design and development of two of the MOS/LSI circuits in the HP-35 Pocket Calculator: the control and timing chip and the read-only-memory chips. Now working for his PhD at Stanford University, Chung still manages to find time now and then to relax with swimming or table tennis.

Algorithms and Accuracy in the HP-35

A lot goes on in that little machine when it's computing a transcendental function.

By David S. Cochran

THE CHOICE OF ALGORITHMS FOR THE HP-35 received considerable thought. Power series, polynominal expansions, continued fractions, and Chebyshev polynominals were all considered for the transcendental functions. All were too slow because of the number of multiplications and divisions required. The generalized algorithm that best suited the requirements of speed and programming efficiency for the HP-35 was an iterative pseudo-division and pseudo-multiplication method first described in 1624 by Henry Briggs in 'Arithmetica Logarithmica' and later by Volder[1] and Meggitt[2]. This is the same type of algorithm that was used in previous HP calculators.

An estimate of program execution times was made, and it became apparent that, by using a bit-serial data word structure, circuit economies could be achieved without exceeding a one-second computation time for any function. Furthermore, the instruction address and instruction word could be bit-serial, too.

The complexity of the algorithms made multilevel programming a necessity. This meant the calculator had to have subroutine capability, as well as special flags to indicate the status and separations of various programs. In the HP-35, interrogation and branching on flag bits—or on arithmetic carry or borrow—are done by a separate instruction instead of having this capability contained as part of each instruction. This affords a great reduction in instruction word length with only a slight decrease in speed.

The arithmetic instruction set was designed specifically for a decimal transcendental-function calculator. The basic arithmetic operations are performed by a 10's complement adder-subtractor which has data paths to three of the registers that are used as working storage. Partial word designators (word select) are part of the instruction word to allow operating on only part of a number—for example, the mantissa or the exponent field.
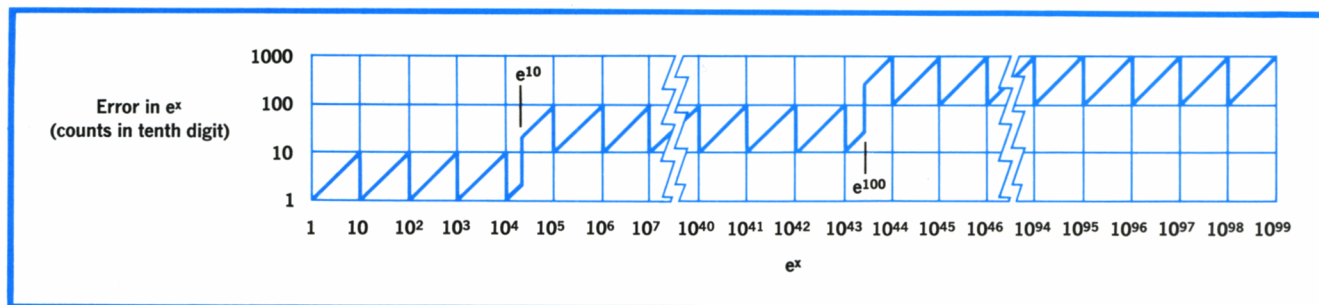
Sine Algorithm

The sine routine illustrates the complexities of programming a sophisticated calculator. First, degrees are converted to radians by multiplying by $2\pi/360$. Then integer circles are removed by repeatedly subtracting 2π from the absolute value of the argument until the result is less than 2π. If the result is negative, 2π is added to make it positive. Further prescaling to the first quadrant isn't required. The resulting angle is resolved by repeatedly subtracting $\tan^{-1} 1$ and counting until overdraft, then restoring, repeatedly subtracting $\tan^{-1} 0.1$ and counting until overdraft, and so on. This is very similar to division with a changing divisor. Next the resulting pseudo-quotient is used as a multiplier. Beginning with an X vector of 1 and a Y vector of 0 a fraction of X is added to Y and a fraction of Y is subtracted from X for the number of times indicated by each multiplier digit. The fraction is a negative power of 10 corresponding to that digit position. The equations of the algorithm are:

$$\text{pseudo-division} \begin{cases} \theta_{n+1} = \theta_n - \tan^{-1} k \end{cases}$$

$$\text{pseudo-multiplication} \begin{cases} X_{n+1} = X_n - Y_n k \\ Y_{n+1} = Y_n + X_n k \end{cases}$$

$$\begin{aligned} & X_0 = 1, Y_0 = 0 \\ & k = 10^{-j} \qquad j = 0,1,2\ldots \end{aligned}$$

The pseudo-multiplication algorithm is similar to multiplication except that product and multiplicand are interchanged within each iteration. It is equiva-

Fig. 1. *Accuracy of exponential function in HP-35 Calculator. Error bound is approximately δe^x, where δ is the error due to prescaling and the algorithm itself. δ is estimated to be equivalent to one count in the tenth significant digit of the argument x.*

lent to a rotation of axes. The resultant Y and X vectors are proportional to the sine and cosine respectively. The constant of proportionality arises because the axis rotation is by large increments and therefore produces a stretching of the unit circle. Since this constant is the same for both sine and cosine their ratio is identically equal to the tangent. The signs of each are preserved. The sine is derived from the tangent by the relationship

$$\sin \theta = \frac{\tan \theta}{(1+\tan^2\theta)^{1/2}}.$$

Accuracy and Resolution

Determination of the accuracy of the HP-35 is as complex as its algorithms. The calculator has internal roundoff in the 11th place. In add, subtract, multiply, divide, and square root calculations the accuracy is $\pm\frac{1}{2}$ count in the 10th digit. In calculating the transcendental functions many of these elementary calculations are performed with the roundoff error accumulating. In the sine computation there is a divide, a multiply, and a subtract in the prescale operation, and there are two divides, a multiply, an addition, and a square root in the post-computation. Roundoff errors in these calculations must be added to the error of the basic algorithm to get the total error.

Accuracy and resolution are sometimes in conflict; for example, the subtraction of .9999999999 from 1.0 yields only one digit of significance. This becomes very important, for example, in computations of the cosines of angles very close to 90°. The cosine of 89.9° would be determined more accurately by finding the sine of 0.1°. Similarly, the sine of 10^{10} wastes all ten digits of significance in specifying the input angle, because all integer circles will be discarded.
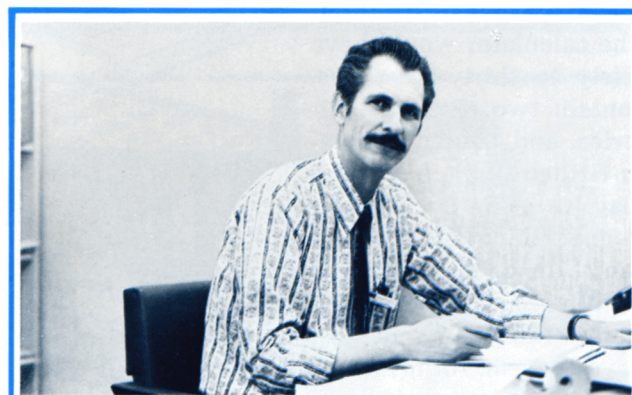
For many functions there is no simple exact expression for the error. The exponential function is a good example. Let δ be the accumulated prescal-

ing error and computational error in the algorithm, referred to the input argument x. Then for $\delta \ll 1$,

$$e^{x+\delta} - e^x = e^\delta e^x - e^x = e^x(e^\delta - 1) \approx \delta e^x.$$

Fig. 1 shows the error bound for the exponential function for various arguments, assuming that δ is equivalent to one count in the tenth significant digit of x.

References

1. Jack E. Volder, 'The CORDIC Trigonometric Computing Technique.' IRE Transactions on Electronic Computers, September 1959.
2. J. E. Meggitt, 'Pseudo Division and Pseudo Multiplication Processes,' IBM Journal, April 1962.

David S. Cochran
Dave Cochran is HP Laboratories' top algorithm designer and microprogrammer, having now performed those functions for both the 9100A and HP-35 Calculators. He was project leader for the HP-35. Since 1956 when he came to HP, Dave has helped give birth to the 204B Audio Oscillator, the 3440A Digital Voltmeter, and the 9120A Printer, in addition to his work in calculator architecture. He holds nine patents on various types of circuits and has authored several papers. IEEE member Cochran is a graduate of Stanford University with BS and MS degrees in electrical engineering, received in 1958 and 1960. His ideal vacation is skiing in the mountains of Colorado.

11

Packaging the Pocket Calculator

The industrial design of the HP-35 was of primary importance, often taking precedence over electrical considerations.

By Edward T. Liljenwall

THE INDUSTRIAL DESIGN OF THE HP-35 was unusual not only for Hewlett-Packard, but for the electronics industry in general. Usually, the mechanical and electrical components of a product are determined before the exterior is designed. The HP-35 took the opposite approach.

Since the calculator was to be pocket-sized, size was the overriding constraint on the design. In addition to size three other parameters were established. The calculator would have thirty to thirty-five keys, contain two or three batteries, and have a twelve-to-fifteen-digit LED display.

The industrial design began with an investigation of keyboard, packaging, and overall shape concepts. Several basic form factors were studied using sketches and simple three-dimensional models. The models were particularly valuable at this stage of development. They allowed a good evaluation of the shapes and sizes being considered.

Once the preferred direction had been established a detailed model was built. The model was well accepted and approval was given to develop the concept into a reality.
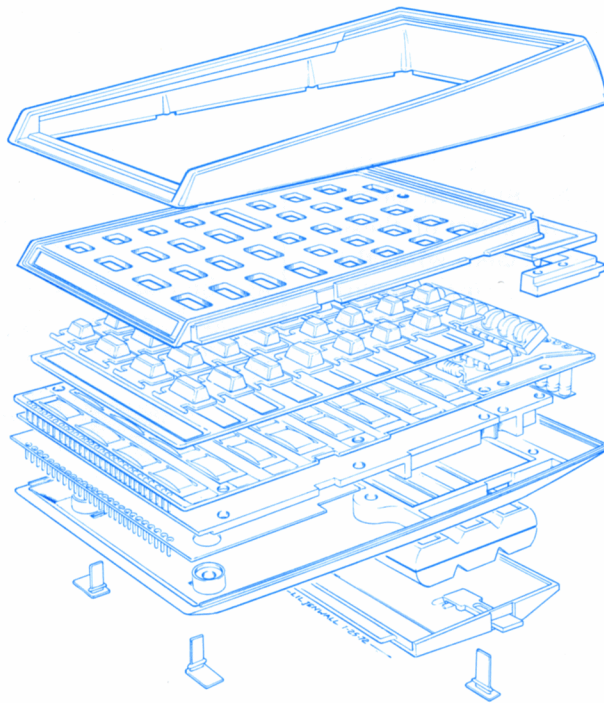
Only a general idea of the electronic design was known at this point. Designing and packaging all necessary electrical and mechanical components into the tiny product became a tremendous challenge for electrical, mechanical, and industrial designers alike.

From a human-engineering standpoint, the keyboard was the most critical area of the design. The problem was to place thirty-five keys in an area approximately 2½ inches by 4½ inches and retain the ability to operate the keys without striking more than one at a time. It became apparent that the industry standard of ¾-inch center-to-center key spacing could not be maintained. A successful compromise was to use $^{11}/_{16}$-inch center-to-center spacing for the numeric keys, and ½-inch spacing for all others. This was made possible by reducing the size of each key, thereby increasing the space between the keys.

The keys are divided into groups according to functions. The groups are separated by size, value contrast, color, and placement of nomenclature. The numeric keys, which are most frequently used, are larger and have the strongest value contrast. They have their nomenclature directly on the keys. The next group of keys accord-

12

ing to frequency of use are identified by their blue color. The ENTER↑ key and arithmetic keys are separated within this group by placement of nomenclature on the keys. The less frequently used keys have the least value contrast, and the nomenclature is placed on the panel just above the key.

The keys have an over-center or snap feel when they are pressed. This comes from special spring contact developed by HP. The electrical and mechanical parts of the keyboard are less than ⅛ inch high.

The spring contacts are mounted on a printed-circuit board along with several other components including the fifteen-digit LED display. The display is tilted toward the operator for optimum viewing.

A second printed-circuit board carries the majority of the electronic components. The two boards are attached by a series of pin connectors.

The external package was developed from a human-engineering approach, with aesthetic appeal of major importance. The sculptural wedge shape permits the calculator to be comfortably held in the palm of one hand. It also allows the product to slide easily into a pocket. The keyboard and display slope upwards for a better viewing angle in desk-top use. The sculptural sides visually break up the total mass of the package. The top half of the case is highlighted while the bottom half is in shadow. This gives the product the appearance that it is thinner than it actually is. The product appears to be floating when viewed from a normal operating position in desk-top use. The use of textures that complement each other contribute significantly to the overall finesse and appearance. The texture on the case provides a non-slip surface, important when the calculator is being hand-held.

Viewed from the bottom, the calculator retains a clean appearance. There are no exposed screws or other fastening devices. This is aesthetically important to a product that is hand-held and viewed from all sides.

The polyvinyl-chloride feet prevent the calculator from sliding during desk-top use. The rear feet also serve as the battery-door latches, aiding in the overall cleanness of the product.

The HP-35 couldn't have been developed without an outstanding working relationship between laboratory, industrial design, manufacturing, and tooling. Everyone involved in the project shared a common desire to retain the original size and shape, and many innovative engineering concepts resulted. Many of the problems encountered during development could have been easily solved by using more conventional methods, but the result would have been a larger package. Now that the calculator is a reality, everyone feels that the extra efforts required were worthwhile.

SPECIFICATIONS
HP-35
Pocket Calculator

FUNCTIONS:
ARITHMETIC: Add, Subtract, Multiply, Divide and Square Root.
TRIGONOMETRIC: Sin x, Cos x, Tan x, Arc Sin x, Arc Cos x, Arc Tan x.
LOGARITHMIC: Log_{10} x, Log_e x, and e^x.
OTHER FUNCTIONS: x^y, $1/x$, π and data storage and positioning keys.

SPEED OF OPERATION (typical):

Add, Subtract	60 milliseconds
Multiply, Divide	100 milliseconds
Square Root	110 milliseconds
Logarithmic & Exponential	200 milliseconds
x^y	400 milliseconds
Trigonometric	500 milliseconds

POWER:
ac: 115 or 230 V ±10%, 50 to 60 Hz, 5 watts.
Battery: 500 mW derived from Nickel-Cadmium rechargeable Battery Pack.

WEIGHT:
Calculator: 9 oz., Recharger: 5 oz.
Shipping weight: approx. 2 lbs.

TEMPERATURE RANGE:
OPERATING: 0°C to 40°C (32°F to 104°F).
STORAGE: −40°C to +55°C (−40°F to 131°F).

PRICE IN USA: $395, including battery pack, 115/230 V adapter/recharger, carrying case, travel case, name tags, operating manual.
Note: At press time, orders for the HP-35 have exceeded expectations to such an extent that a waiting list has been established. Deliveries should improve in the next few weeks.

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Edward T. Liljenwall
Ed Liljenwall, industrial designer of the HP-35 Pocket Calculator, is a 1967 graduate of the Art Center College of Design in Los Angeles. He holds a BS degree in industrial design. Ed joined HP's corporate industrial design group in 1960 after two and one-half years as an automotive designer. As a result of his work on the HP-35, he's filed for several design patents. Away from HP, Ed likes to ski or water-ski, and is currently putting another hobby, woodworking, to good use in redecorating his home.

New Capabilities in Digital Low-Frequency Spectrum Analysis

*A new Fourier analyzer and two fast-transform periph-
erals adapt to a wide range of applications.*

By Stephan G. Cline and Norman D. Marschke

SPECTRUM ANALYSIS, a powerful technique
of signal and system analysis, is the process of
resolving a physical waveform into sinusoidal com-
ponents having appropriate phase relationships.
That this can be done was shown by J.B.J. Fourier
in the 18th century. The reason for its great utility
is that a simple statement of spectrum content or
bandwidth often makes possible engineering judg-
ments about a problem that couldn't be made on the
basis of observations of the waveform itself.

In spite of its usefulness, applications of spec-
trum analysis were concentrated for many years in
the radio and electronic sciences, where the fre-
quencies encountered are in the megahertz range
and higher. Now, however, the use of spectrum
analysis at low and moderate frequencies is on the
increase, partly because many more people realize
its power as an engineering tool, but mainly because
accurate and stable instrumentation has recently
become available for this frequency range. Prob-
lems in mechanical vibrations, underwater sound,
biomedicine, communications, machine mainte-
nance, feedback control systems, speech, and acous-
tics are now yielding to spectrum analysis. The in-
struments being used are mostly digital analyzers
which compute spectra by means of one form or
another of the fast-Fourier-transform (FFT) algo-
rithm.[1]

Within the last year, faster computers and hard-
ware FFT processors have significantly increased
the speed of Fourier analysis, to the point where
real-time spectrum analysis to beyond 10 kHz can
be done using entirely digital instruments. Among
Hewlett-Packard's second-generation Fourier-anal-
ysis instruments are a new Fourier Analyzer, a new
plug-in FFT Arithmetic Unit for HP computers, and
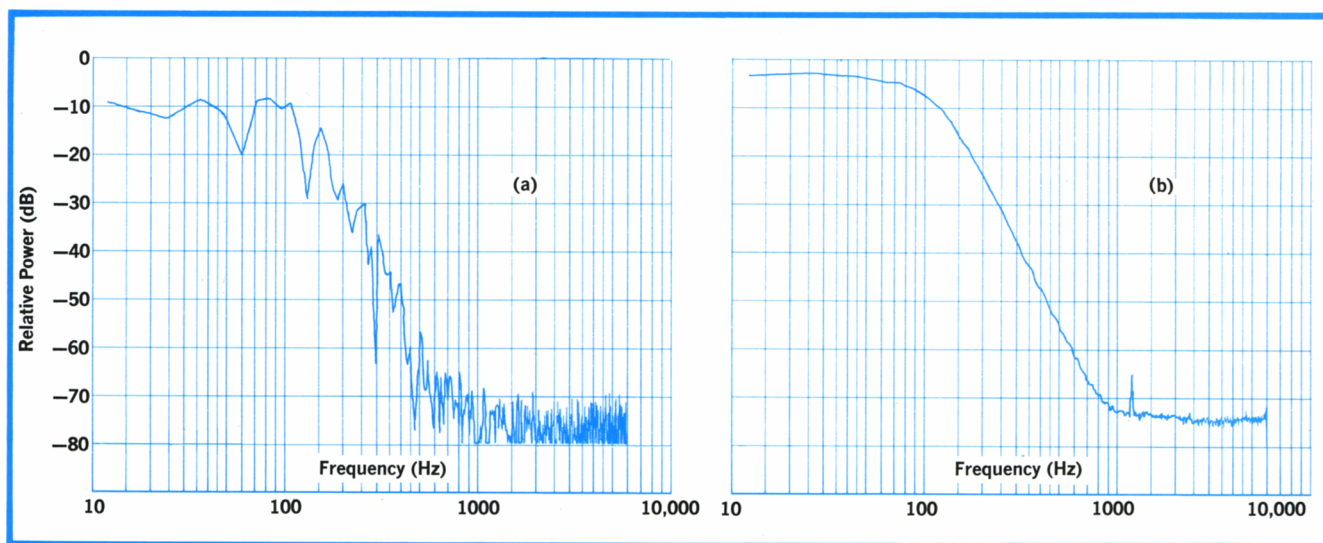a new peripheral Fast Fourier Processor.

Why Digital?

Why did the use of spectrum analysis at low fre-
quencies have to wait for the development of digital
instruments before becoming widespread? The an-
swer can be seen by comparing digital analyzers
with previously available instruments.

The simplest way to resolve a waveform into its
spectral components is to use a narrow bandpass
filter and a voltmeter. Measuring the portion of the
signal passed by the filter gives an approximation
to the size of the sinusoidal component at the filter
center frequency. If the filter is tunable, spectrum
analysis can be carried out over a range of frequen-
cies. This is the principle of the wave analyzer, the
most elementary spectrum analyzer.

The wave analyzer has the basic limitation of all
spectrum analyzers. The bandwidth of the filter,
and therefore its resolution, determines its response
time. A period of time approximately equal to the
reciprocal of the analyzer passband must be spent at
each frequency to get an accurate estimate of the
spectral content at that frequency. This isn't a seri-
ous problem at frequencies in the megahertz range
and higher, but at low frequencies, where the reso-
lution needed may be on the order of one hertz, a
single-frequency measurement may take as much as
one second.

If the signal being analyzed is random, each read-
ing must be averaged over an even longer period of
time to get a statistically stable or smooth result. A
measurement made in this way may correctly meas-
ure the spectrum at 1.0 kHz while missing a short
term event at 1.5 kHz.

For these reasons, wave analysis is suitable only
when the signal being analyzed is stationary and
when comparatively long periods of time are avail-
able to sweep over the band of interest. Heterodyne

Fig. 1. *Power spectra of random noise illustrate resolution, dynamic range, and flexibility of digital analyzers. (a) Spectrum computed from one 102.4 ms record. (b) Average of 200 records has same 512-channel resolution as single record. Dynamic range is 80 dB. Note 1.2-kHz component at about −70 dB which is not visible in unaveraged spectrum.*

techniques which translate the measurement to higher frequencies make for better accuracy, better display, and less cost, but they don't solve the time-bandwidth limitation at low frequencies. Spectrum analyzers of this type are still basically single-filter wave analyzers.

The measurement time-bandwidth problem can only be alleviated if some form of parallel filtering is employed. The most direct way to build a spectrum analyzer that is real-time at all frequencies is to use a set of parallel filters. Such a method is most effective when filters of constant percentage bandwidth, such as ⅓ octave or full octave, are employed. Octave-band analyzers of this type are very useful and effective instruments.

Speed-Up Analyzer

However, when higher resolution or constant-bandwidth filters are needed, this approach has proved impractical. The nearest solution to parallel filtering using constant-bandwidth, narrow-band filters is a digital-analog hybrid approach called the speed-up analyzer. In this analyzer an analog-to-digital converter samples the waveform to be analyzed at a rate F_s and loads a memory with a record of N samples over a period of time $T = N/F_s$. The data gathered in this way is analyzed by re-circulating it in the memory at a much higher rate. The data time scale is thus reduced and the speeded up digital data is applied to a digital-to-analog converter, resulting in a new signal with scaled-up frequency. This new signal is then analyzed by the

equivalent of a high-frequency wave analyzer. At the higher frequency the analyzer sweep time is greatly reduced and near-real-time analysis can be carried out*. It isn't quite real-time, though, because there's a 20-to-100-millisecond gap between the processing of one T-second record and the processing of the next, so some of the signal information is lost.

All-Digital Analyzer

An important limitation on the performance of speed-up analyzers is the loss of dynamic range and resolution introduced by the analog circuitry of the final wave analyzer. Better dynamic range and resolution and greater flexibility in data processing can be obtained with a purely digital analyzer.

Like the speed-up analyzer, the all-digital analyzer samples the input signal at a rate F_s for T seconds and loads $N = TF_s$ sample values into its memory. Certain measurement limits imposed by the sampling process are shared by the digital analyzer and the speedup analyzer. First, the highest frequency that can be analyzed without ambiguity is $1/2 F_s$. This maximum frequency is the Nyquist folding frequency; above it, aliasing error occurs[2]. Second, the resolution is determined by the record length. A record length of T seconds implies that the frequency resolution is $\Delta f = 1/T$.

This smallest frequency element is a result of the fact that for a record of length T seconds no discrete

*Real-time analysis is defined here as the analysis of contiguous records of data with no gaps.

15

Fourier transform can be defined with a resolution narrower than Δf Hz. It has nothing to do with any other hardware constraint such as filter bandwidths.

The digital analyzer transforms the N digitized values stored in its input memory to a set of N/2 Fourier coefficients spaced 1/T Hz apart. The result of this Fourier transform is a set of real and imaginary coefficients, which may be used directly or further processed to obtain the magnitude and phase of the spectrum, or the power (magnitude squared) spectrum, or many other functions.

The measurement time-bandwidth limitation of wave analyzers isn't a problem with digital analyzers. From a single T-second sample record of N samples, the digital analyzer computes a complete spectrum equivalent to N/2 wave-analyzer measurements each 1/T Hz apart. The same spectrum would take at least N/2 times as long to measure with a wave analyzer.

If the data being analyzed is random or has a random component, so that several separate sample records must be averaged to smooth the result, this is easily done in digital spectrum analysis by summing the results of one sample record into the accumulated result from past samples. One of the advantages of digital computation of the spectrum is that averaging may be done digitally without the use of analog integrators, which have limited dynamic range and linearity.

An Example

Fig. 1 illustrates some of the capabilities of the latest digital analyzers. It shows the power spectrum of a band-limited random noise signal computed in real time. Each record used to compute the spectrum is 102.4 milliseconds long and consists of 1024 samples of the noise signal.

Fig. 1(a) is the spectrum computed from one record, and the variance caused by the randomness of the signal is evident. Fig. 1(b) is the average of the spectra computed from 200 sample records. Besides being much smoother, this spectrum reveals the presence of a periodic component at 1.2 kHz. These results, computed from only 20.48 seconds of data, are good examples of the resolution, dynamic range, and processing flexibility of a digital analyzer.

New Fourier Analyzer

Fig. 1 was produced by the new Model 5451A Fourier Analyzer, Fig. 2. Like earlier HP Fourier analyzers[3], the new analyzer is a keyboard-controlled computer-based system capable of sampling one or more input signals and computing power
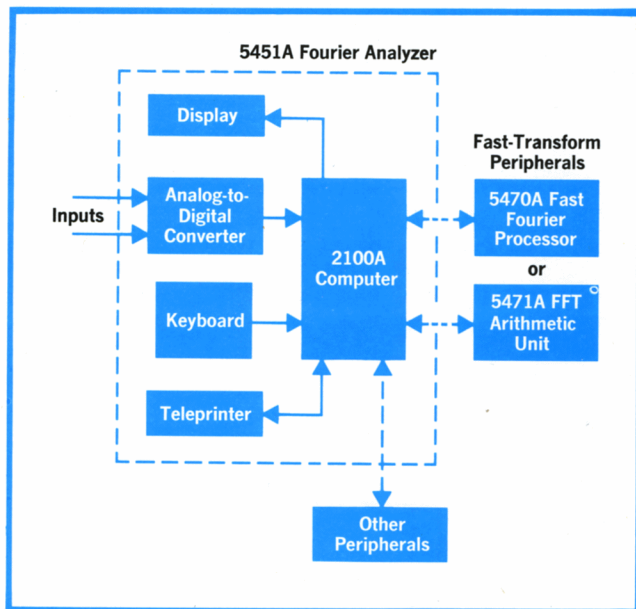

Fig. 2. New Model 5451A Fourier Analyzer, a minicomputer-based, keyboard controlled, dual-channel analyzer, can do spectrum analysis, correlation, coherence analysis and many other complex data manipulations. New capabilities are 80-dB dynamic range, relocatable software, buffered input, and a faster computer.

spectra, cross power spectra, transfer functions, coherence functions, correlation functions, and many other functions. These computations and other complex data manipulations are performed in the computer by software routines which are initiated by pushing buttons on the keyboard. The user can choose to add his own routines to the software supplied. He can also use the integral minicomputer separately as a general purpose computer. Fig. 3 is a block diagram of the Fourier analyzer system.

Differences between the new 5451A and earlier models are a new faster computer, Model 2100A[4], greater dynamic range (80 dB for both amplitude and power spectrum), relocatable software which simplifies adding and modifying user-written programs, and a buffered input mode which improves processing efficiency.

Fig. 4 shows the difference between the new buffered input mode and the ordinary input mode. Ordinarily, an input record is read into the computer memory and then processed, and while the power spectrum is being computed no new input data is collected. Without its optional hardware processors, the 5451A Fourier Analyzer may take as long as 1.5 seconds to complete these processing steps for a 1024-point record. Considerable improvement is realized when the buffered input mode of operation is used. In this mode data is read into a buffer

Fig. 3. *Analog-to-digital converter samples input signals at rates to 50 kHz. Keyboard controls data manipulations done by software in basic 5451A Fourier Analyzer. Fast-processor options add hardware transform capability.*

block while the previous record is being processed. With this parallel input-while-processing scheme it is possible to achieve real-time spectrum analysis to 300 Hz using a 5451A Fourier Analyzer with only a software Fourier transform.

Faster Fourier Analysis

Further improvements in processing speed are realized with special-purpose hardware which speeds up the required computations. Either the 5470A Fast Fourier Processor or the 5471A Fast Fourier Transform Arithmetic Unit can be added as options to the 5451A Fourier Analyzer for this purpose.

Increases in processing speed increase the analyzer's upper frequency limit for real-time analysis. Increased speed also saves machine time, which is important in test situations of limited duration, such as vibration testing of a spacecraft which might be fatigued in a long test.
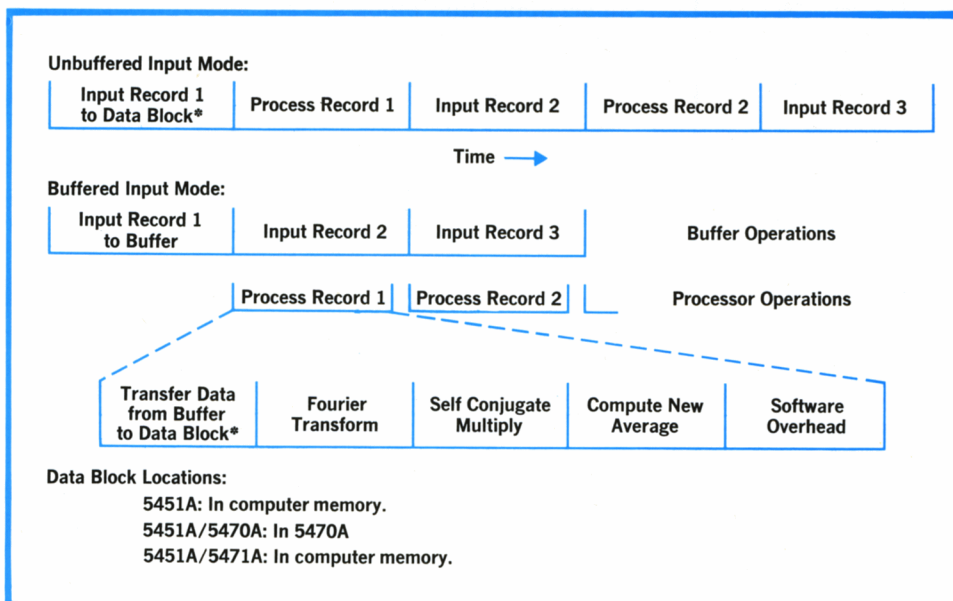
The 5470A Fast Fourier Processor (Fig. 5) is an external peripheral which has its own data memory and function control memory. It takes only 15 milliseconds to compute a Fourier transform for a 1024-point block size, compared to one second for the standard 5451A Fourier Analyzer.

The four-card 5471A FFT Arithmetic Unit (Fig. 6) fits into four contiguous I/O slots in the computer and speeds up computations while continuing to use the computer for data storage and function control. With the 5471A a 1024-point transform can be computed in 160 ms.

The software drivers for the 5470A and 5471A are written so analyzer operation is exactly the same as the standard 5451A Fourier Analyzer, except that the execution times are much faster.

The following array operations are performed by the 5470A or the 5471A options in the 5451A.
- Forward and inverse fast Fourier transform.
- Time-domain weighting by Hanning.
- Self-conjugate block multiplication in single or double precision.
- Block addition/subtraction and scaling in single or double precision.

Fig. 4. *Timing diagrams for computation of power spectrum average. New buffered input mode is capability of 5451A Fourier Analyzer with or without fast-processor options. Parallel input-while-processing operation in buffered mode increases system efficiency.*

17

Multiple array operations are used to perform complete spectrum analysis functions such as:

- Auto and cross power spectrum average.
- Auto and cross correlation.
- Convolution.
- Transfer and coherence functions with the aid of division routines in the host computer.

Fig. 5. New Model 5470A Fast Fourier Processor used with 5451A Fourier Analyzer lowers time for 1024-point transform to 15 milliseconds. Processor can also add Fourier-transform capability to other computer systems.

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The Where and How of Fourier Analyzers

Here are examples of how HP Fourier Analyzers are being used in various locations around the world:

Massachusetts. Used aboard a research ship for sea floor exploration in search of oil fields.

Canada. Underwater Acoustics. Extensive use of coherence and transfer function analysis to determine optimum sonar bubble shape.

Germany. Acoustic and vibration analysis of linear servo systems.

California. Civil Engineering. Used to study dynamic characteristics of large structures, such as resonant frequencies and damping factors, to determine how they will withstand earthquakes.

Sweden. Biomedical. Electromyography. Used in studying types of signals transmitted on various types of nerves for designing automatic prostheses.

Michigan. Vibration analysis on vehicle drive trains in production environment to determine correct/incorrect operation of gears and other parts.

Iowa. Vibration analysis on tractors to aid in design of drive train and frame components.

Belgium. Vibration analysis on machinery used in the application of emulsion to film to determine effect of vibrations on emulsion.

New York. Vibration analysis on cutting tools to determine wear characteristics.

France. Vibration studies of helicopters aimed at noise reduction.

Netherlands. Civil Engineering. Analysis of vibrations of tunnels, dikes and other large structures to determine dynamic characteristics.
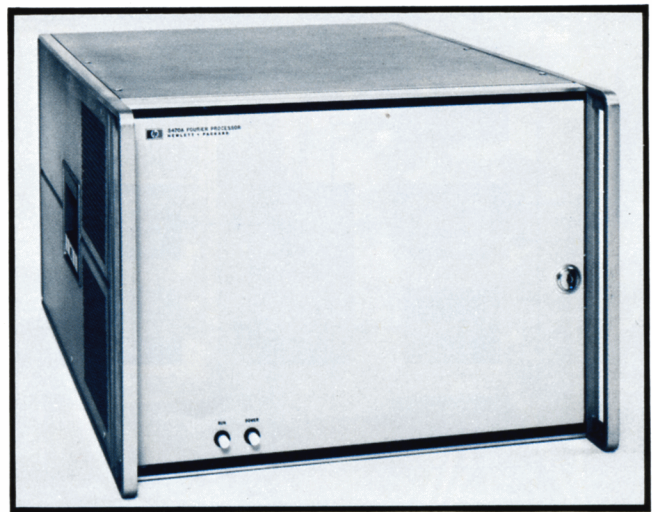
Michigan. Vibration analysis of production power tools to determine wear and efficiency.

Michigan. Vibration analysis of axles and axle housings to improve design and for production testing.

Michigan. Vehicle crash studies. Used to design automobile components such as steering wheels.

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Fast Fourier Processor

The 5470A Fast Fourier Processor is a digital processor designed to perform the Fourier analysis routines rapidly and at reasonable cost. As a peripheral to the 5451A system, the 5470A operates under functional control of the host computer which provides it data, microprograms, and execution command parameters.
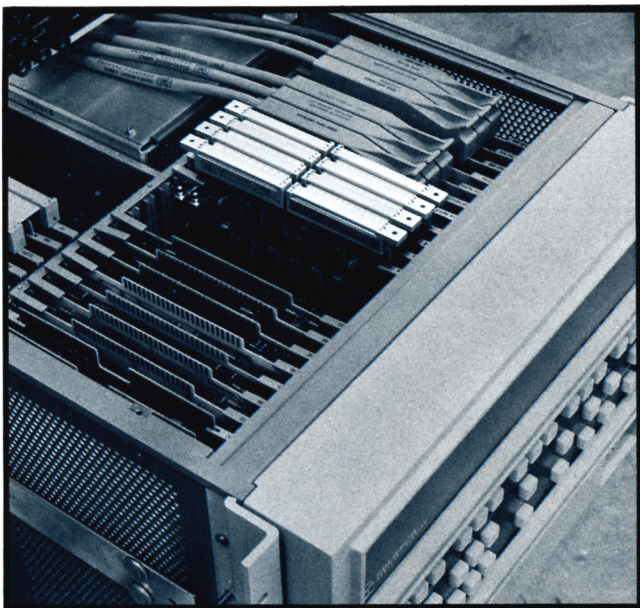
Nearly all data-array manipulations normally needed for spectrum analysis are performed in the Fast Fourier Processor. It has either a 4096-word data memory or an optional 8192-word data memory, and data blocks may range in size from 64 to 2048 words (4096 optional).

When a power spectrum average is being computed, data flow in the combined 5451A/5470A system is similar to that in the analyzer alone. After the buffer in the computer is filled with input data from the analog-to-digital converter, the data is transferred to the data memory in the 5470A. For each data record a time-to-frequency Fourier transform, a self-conjugate multiply, and an addition into the accumulation block are successively performed in the 5470A. While these operations are in progress the computer is free to load the next data record into the buffer section of its memory from the analog-to-digital converter, and send output to the display if time permits.

All block operations on data in the 5470A are controlled by microprograms from the computer. For each operation a microprogram from the software driver is loaded into the processor's function control memory and then executed. Each user command may call for multiple 5470A operations.

The Fast Fourier Processor is linked to the computer in the 5451A Fourier Analyzer by two I/O channels which use standard 16-bit TTL microcircuit interface cards. Since the interface cards are standard, the fast processor doesn't have to be used with a Fourier analyzer; it can add Fourier-analysis capability to other computer systems as well.

Fig. 6. *New Model 5471A Fast Fourier Transform Arithmetic Unit plugs into four I/O slots in HP computers. 1024-point transform time is 160 milliseconds.*

Fast Fourier Transform Arithmetic Unit

The 5471A Fast Fourier Transform Arithmetic Unit speeds up by a factor of 6 or more many of the operations required in Fourier analysis. The FFT Arithmetic Unit is a hardware-software package. The hardware consists of four printed-circuit boards with plug into any four contiguous I/O slots in a Hewlett-Packard 2100-series computer.

The software consists of a driver written in HP assembly language. The driver has been incorporated into the Fourier analyzer software so to the user the operation is the same as the standard analyzer except for the faster speed. Another assembly language driver allows the 5471A to be used with a stand-alone computer by those users who need Fourier arithmetic capability but don't want a complete Fourier analyzer system.

Data is stored in the computer, not in the arithmetic-unit hardware. The 5471A memory is simply a small scratchpad. Memory addressing and read/writing are done by software while the arithmetic operations are done by the 5471A hardware.

SPECIFICATIONS
HP Model 5451A
Fourier Analyzer

ANALOG INPUT
AMPLITUDE RANGE: 0.1 V to 10 V full scale.
RESOLUTION: 10 bits with sign.

DISPLAY UNIT
Data may be displayed on the 8 × 10 cm CRT display or output to a plotter or remote display.

AMPLITUDE SCALE: Data in memory is automatically scaled to give a maximum on-screen calibrated display.
LINEAR DISPLAY RANGE: ±4 divisions with scale factor ranging from 1×10^{-512} to $5 \times 10^{+512}$ in steps of 1, 2, 5, and 10.
LOG DISPLAY RANGE: 4 decades with a scale factor ranging from 0 to ±998 dB.

DIGITAL ACCURACY AND RESOLUTION
All calculations use floating point arithmetic on a block basis. Data overflow does not occur. Amplitude resolution is 1 part in 16,000 worst case.
DATA WORD SIZE: 16-bit real and 16-bit imaginary or 16-bit magnitude and 16-bit phase. 32 bits real is preserved for auto power spectra. Division, addition, and subtraction operations performed in 16 bits or 32 bits depending on data.
TRANSFORM ACCURACY: 0.1% of full scale worst case error during forward or inverse calculation.
TRANSFORM SIZE: From 64 to 4096 time points.
TRANSFORM SPEED: 1 s for 1024 time points.

SPECTRAL RESOLUTION
The element of spectral resolution is the frequency channel width —the maximum frequency divided by ½ the data block size.
MAXIMUM FREQUENCY: 25 kHz single channel; 10 kHz dual channel. Adjustable in steps of 1, 2.5, 5, and 10 down to 0.1 Hz.
DYNAMIC RANGE: 80 dB for voltage magnitude spectrum and auto power spectrum.

POWER SOURCE: 115/230 volts ±10%, 50/60 Hz. 1400 watts typical for basic system (excluding teleprinter).

ENVIRONMENTAL CONDITIONS: 0°C to 55°C.
Relative Humidity: To 95% at 40°C (104°F).

PRICE IN USA: 5451A System prices start at $35,000.

HP Model 5470A
Fast Fourier Processor

TRANSFORM BLOCK SIZE: 64 to 2048 real points standard. Up to 4096 points optional.

DATA MEMORY:
4096 16-bit words, optional 8K available.

SINGLE PRECISION OPERATIONS:
Fast Fourier transforms—forward and inverse.
Interval centered Hanning.
Self multiply; real, complex, and conjugate.
Cross multiply; real, complex, and conjugate.
Scale and add.

DOUBLE PRECISION OPERATIONS:
Self conjugate multiply.
Scale and add.

FOURIER TRANSFORM TIME (based on a 1024 real point block size): 15.2 ms.

ENVIRONMENTAL: 0°C to 55°C.

PRICE IN USA: 5470A prices start at $25,000.

HP Model 5471A
Fast Fourier Transform Arithmetic Unit

ARRAY SIZES
TRANSFORM BLOCK SIZE: 64 to 2048 points in powers of 2.
ADDITION BLOCK SIZE: 64 to 2048 points in powers of 2.

SINGLE PRECISION OPERATIONS
Forward and inverse fast Fourier transforms.
Interval centered Hanning.
Real, complex, and complex conjugate multiply.
Block scaling and block addition.

DOUBLE PRECISION OPERATIONS
Self complex conjugate multiply.
Block scaling and block addition.

FOURIER TRANSFORM TIME (based on 1024 word block size): 160 ms with 2100A Computer.

ENVIRONMENTAL: 0° to 55°C.

PRICE IN USA: 5471A prices start at $4500.

MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050

The 5471A must be microprogrammed for each type of arithmetic operation (i.e., Fourier transform, complex multiply, double-precision self-conjugate-complex multiply, Hanning, etc.). For each operation a microprogram from the software driver is loaded into the program memory on the 5471A program board and then the 5471A is ready to start.

The design philosophy of the 5471A is analogous to the concept of impedance matching for optimal power transfer. The 5471A matches times instead of impedance. It makes the time required for the hardware to perform its arithmetic tasks approximately equal to the time required for the software to output 16-bit data words to the 5471A, generate the next data addresses, and then input 16-bit data words from the 5471A to the computer. The arithmetic operations consume approximately 85% of the machine time required to do a Fourier transform. The 5471A hardware actually processes the data faster than the computer can calculate the next addresses. Thus the 5471A is able to speed up the transform time by a factor of 6 to 7.

Acknowledgments

The 5451A systems development has been under the capable leadership of Skip Ross, Ago Kiss, and Pete Roth. Chuck Hershkowitz has written most of the 5451A software.

The 5470A has had many contributors. Hans Nadig designed the arithmetic unit. Dick Grote had responsibility for the memory unit. The program unit was designed by Webb McKinney. Product design was handled by Chuck Lowe and technician assistance by Bill Katz. Dave Snyder has written the software to drive the 5470A.
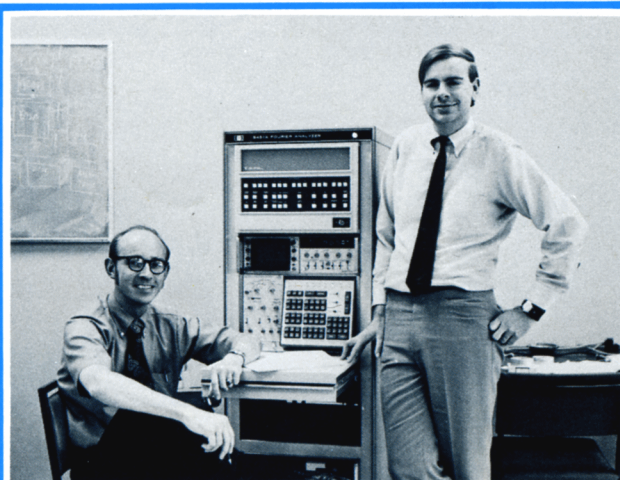
5471A hardware and software development was assisted by Dolores Solorio.

Credit for getting the 5451A, 5470A, and 5471A into production must go to Walt Noble, our very capable production engineer. ●

References

1. G. D. Bergland, 'A Guided Tour of the Fast Fourier Transform.' IEEE Spectrum, Vol. 6, pp. 41–52, July 1969.
2. Hewlett-Packard Application Note 140-0.
3. A. Z. Kiss, 'A Calibrated Computer-Based Fourier Analyzer,' Hewlett-Packard Journal, June 1970.
4. Hewlett-Packard Journal, October 1971.

Stephan G. Cline
Steve Cline (right) is project leader for the 5471A FFT Arithmetic Unit. He's been working with Fourier Analyzers ever since he first came to HP in 1968. He wrote much of the software for the 5450A Fourier Analyzer and was involved in the design of the 5470A Fast Fourier Processor. Steve received his BS degree in electrical engineering from Michigan State University in 1967 and his MSEE from Stanford University in 1968. In his spare time, he expresses his concern for others in a tangible way by working in the Big Brother program. Golf is his main recreation, but he's also into model railroading and biking, both very useful, no doubt, in his Big Brother activities.

Norman D. Marschke
Norm Marschke, project leader for the 5470A Fast Fourier Processor, came to HP in 1964 soon after receiving his MS degree in electrical engineering from the University of Michigan. His BSEE degree is also from Michigan. At HP, Norm has helped design elements of the 5245 Counter system, and has served as project leader for the digital processor in the 5400A/5401A Multichannel Analyzers and for an analyzer/calculator interface. Norm says that a new home now dominates his spare time, but he always makes the annual migration to the mountains when ski season rolls around.