This document was scanned from a much earlier photocopy which already had several issues:

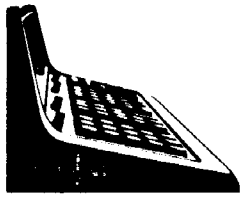
- Some text pages were cut off slightly at the sides.
- The schematics were photocopied on to 11x17 pages. However, the original schematics may have been on sheets larger than 11 x17 and so the collection of schematics appears incomplete.

This file shows the pages as received and is the best scan available at this time. We hope it will be useful.

MODELS 46 & 81 AND 9805A CALCULATOR

REPAIR MANUAL

-hp- Part No. 09805-90029



HEWLETT-PACKARD CALCULATOR PRODUCTS DIVISION
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Table 1-1. General Specifications

Calculator	Calculator Specifications	Packaging Specifications
Model 5	**Operating Temperature:** 0-45°C **Power:** 120V (-10, +5%) 48-66 Hz 240V (-10, +5%) 48-66 Hz 40 VA Maximum **Weight:** Opt 005 16 lbs., 8 oz. (7.48 Kg) **Dimensions:** 10.9 in. wide (27.6 cm) 15.5 in. deep (39.3 cm) 5.5 in. high (14 cm)	**Weight:** 28 lbs. (12.7 Kg) **Dimensions:** 19 in. deep (47.5 cm) 16.5 in. wide (41.3 cm) 8.5 in. high (21.3 cm)
Model 46 & Model 81	**Operating Temperature:** 0-45°C **Power:*** 100V, 120V, 220V or 240 Vac (-10,+5%) 20 VA Nominal 48-66 Hz **Dynamic Range:** 10^{-99} to 10^{100} **Weight:** 13 lbs., 8 oz. (6.12 Kg) **Dimensions:** 10.9 in. wide (27.6 cm) 15.5 in. deep (29.3 cm) 5.5 in. high (14 cm)	**Weight:** 24 lbs. (10.89 Kg) **Dimensions:** 19 in. deep (47.5 cm) 16.5 in. wide (41.3 cm) 8.5 in. high (21.3 cm)

* Model 46 Calculators, S/N 1314A–04593 and below cannot be operated using the 100V or 220 Vac positions of the voltage selector-card.

CHAPTER 1
GENERAL INFORMATION

INTRODUCTION

This manual contains technical information describing the -hp-, preprogrammed, desktop calculators; the Model 5, the Model 46, and the Model 81. We have presumed that this manual will be used only by qualified -hp- service personnel located at designated repair centers. We have also assumed that those personnel who are using the manual have, and are trained to use, the special test equipment described in Chapters 5 and 6.

GENERAL DESCRIPTION

The -hp- preprogrammed, desktop calculators are expanded versions of the smaller, hand-held calculators – the Models 35, 45, and 80. The primary difference between the hand-held and the corresponding desktop calculators are the SEIKO printer and the display being optional. The Model 5 (9805A) is also somewhat different, in that it is intended for use only in the field of statistics. The Model 46, like the Model 45, is primarily a scientific and engineering machine. The Model 81, like the Model 80, is designed for use in business applications.

General Specifications

Table 1-1 lists the general specifications of each calculator for packaging and shipping purposes.

OPTIONS AND ACCESSORIES

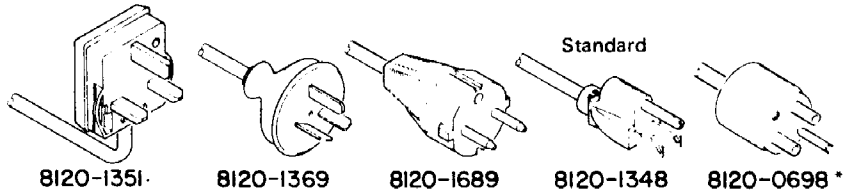
Both the Model 46 and the Model 81 have an optional display (Opt. 001). The Model 81 may also have a 'buffered keyboard' with or without a display; Opt. 002 is a buffered keyboard without a display, while Opt. 003 includes a display. The buffered keyboard allows the user to enter keys while the calculator is busy performing a previous input. Up to 64 keys may be pressed, while the calculator is busy, before subsequent inputs are ignored.

The Model 5 is available in five different configurations:

- The basic Model 5 is Option 001, which contains a printer and statistics keyblock, but has no display.
- Option 2 adds a display to the basic machine.
- Option 3 includes a display and the capability of controlling a 9862A Plotter; the plotter must be ordered separately.
- Option 4 is an Option 2 calculator with the addition of 30 data storage registers and a statistics Programmable Read-Only-Memory (PROM).
- Option 5 adds plotter control capability to Option 4; again, the plotter must be ordered separately.

Power Cords

Various power cords are available for the calculator. Their descriptions and -hp- part numbers are shown in Figure 1-1.



* UL approved for use in the United States with Calculators set for either 220V or 240V operation.

Figure 1-1. Power Cords

RELATED MANUALS

Table 1-2 lists operating manuals for the indicated calculators; Table 1-3 lists related service manuals.

Table 1-2. Operating Information

9805A STAT QUICK REFERENCE	09805-90003
9805A STATISTICS CALCULATOR OPERATING GUIDE	09805-90002
9805A STATISTICS CALCULATOR EXPANDED STAT OPERATING GUIDE	09805-90004
MODEL 46 OPERATING GUIDE	00046-90005*
MODEL 46 SERVICE CARD	00046-90010
MODEL 81 OPERATING GUIDE	00081-90000
MODEL 81 QUICK REFERENCE	00081-90001
MODEL 81 SERVICE CARD	00081-90010

* This manual replaces the previous manual 00046-90000.

Table 1-3. Service Information

9805A CALCULATOR SERVICE MANUAL (on-site only)	09805-90030
MODEL 46 and 81 CALCULATOR SERVICE MANUAL	00046-90031
ET 7083 ROM TESTER OPERATING AND SERVICE MANUAL	09805-90010†
ET 7074 BOARD-TEST SYSTEM OPERATING AND SERVICE MANUAL	00081-90030†

† These manuals can be purchased only from Calculator Products Division.

Table 2-0. Chapter 2 Quick Reference

CIRCUIT	BASIC FUNCTION	REFERENCE PAGES
CALCULATOR	Preprogrammed Calculations	2-1
CONTROL AND TIMING (C&T)	Contains keyboard scanner & maintains a record of system status reports. Generates addresses (Ia) for ROM instructions, and word-synchronization signal for system.	2-2
KEYBOARD	Matrix of user-input keys.	2-2
READ-ONLY-MEMORY (ROM)	Contains preprogrammed instructions that control system operations. The required instructions are selected by the address (Ia) outputs of the C&T. The active ROM is selected by ROM-select instructions from other ROMs.	2-2
ARITHMETIC AND REGISTER (A&R)	Accomplishes all arithmetic calculations specified by the ROM instructions. Porvides the basic system storage registers and time-shared display information.	2-3
I/O PROCESSOR	Interfaces the printer and Model 5 Options to the system. Also expands the system instruction set.	2-4
PRINTER	Primary method of outputting results.	2-4
DATA STORAGE	Provides 10 additional storage registers for the system.	2-5
MODEL 5 OPTIONS	Provides additional specialized functions.	2-5 & 2-6
DISPLAY	Secondary method of outputting results. Also provides system-clock circuits.	2-6
BLOCK DIAGRAM		2-7

CHAPTER 2
GENERAL PRINCIPLES OF OPERATION

INTRODUCTION

The information contained in this chapter describes the basic principles which govern the operation of the Models 46 and 81 and the 9805A. Figure 2-5, a block diagram of the calculator circuits, should be used while the information is being studied.

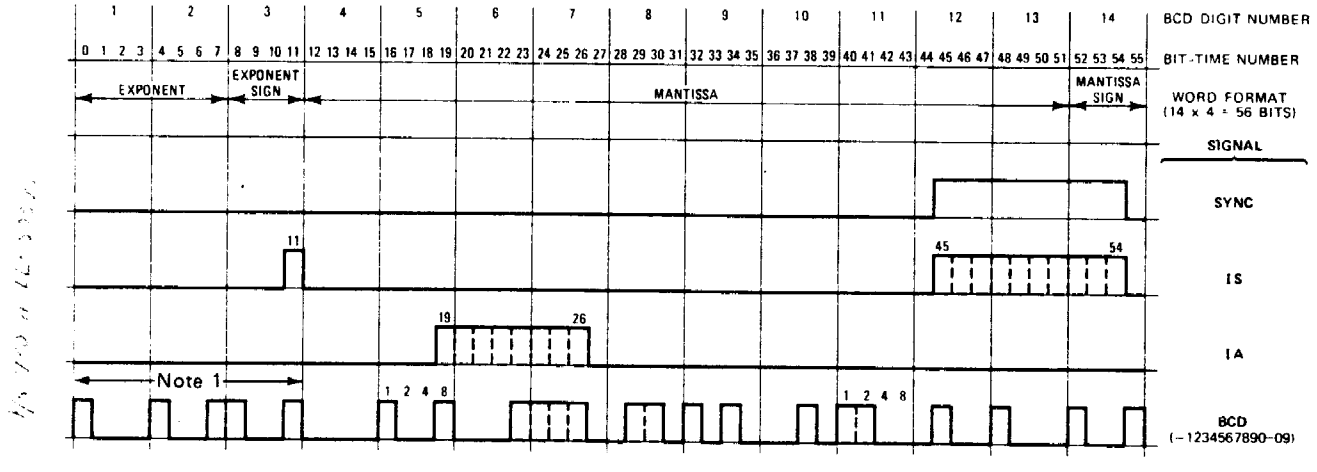
SYSTEM ORGANIZATION

Each of the calculators contains four MOS/LSI (metal-oxide-semiconductor/large-scale-integration) circuits: read-only-memories (ROMs), an arithmetic and register circuit (A&R), a control and timing circuit (C&T), and an I/O processor circuit. Also, three bipolar circuits are utilized: a two-phase clock driver, an LED anode driver/clock generator, and an LED cathode driver.

Basically, each calculator is assembled on three printed circuit boards: the keyboard, the mother board, and the father board. The mother board contains the MOS logic and power supplies. In the Model 5, the A&R and I/O processor circuits are contained on the father board. The father board contains the clock circuits and, if the display option is installed, the display and display-driver circuits. One of two different father boards must be used in each instrument: the father board or the display board. The display board is a father board with the additional display circuits. The Model 81 display and father boards may also contain the buffered keyboard circuits. The keyboard contains the keys and switches for the instrument.

The Model 5 may contain additional circuit boards, depending upon the option installed: the statistics keyblock, which is basically an additional keyboard with the ROMs and logic required to implement its use; the plotter interface, which enables control of the plotter; the data storage board, which provides 30 additional data storage registers for the calculator; the programmable-read-only-memory board (PROM), which contains keycodes for the execution of particular statistical functions. With the exception of the PROM boards, each of the optional assemblies contain the ROMs and logic required to implement its use.

Each calculator is organized on a digit-serial, bit-serial basis. This organization minimizes the number of connections on each chip, thereby saving area and cost and improving reliability. Each word consists of 14 binary-coded-decimal (BCD) digits, and thus is 56 bits long. Ten of the 14 digits are allocated to the mantissa of each number, one is for the mantissa sign, two are for the exponent, and one for the exponent sign (see Figure 2-1). The decimal-point information is included in one of the digit's display information.



NOTE 1: Negative exponents are handled by the system in the ten's-complement notation; positive exponents are handled in the normal BCD form (see Figure 3-4 in Chapter 3).

Figure 2-1. The System Bus-signals

CHAPTER 2
GENERAL PRINCIPLES OF OPERATION

Three main bus lines connect the MOS logic (see Figures 2-1 and 2-5). One carries a word synchronization signal (SY which is generated by a 56-state counter on the C&T circuit. On another bus, instructions (Is) are transmitted se from the ROMs to the C&T, A&R, and to other ROMs. The I/O processor selects one of two instruction sets, the enabling one instruction to have two different meanings. Since one instruction can be used for two different operat the instruction set of the calculator is effectively doubled. The third bus signal, called word-select (WS), is a gating s generated either by the C&T or by one of the ROMs. WS enables the A&R for a portion of a word time, the allowing operations on only part of a number (from 0 to 14 digits, but never a portion of a digit), such as the man or the exponent (see Figure 2-2).

Control and Timing Circuit

The C&T performs the major non-arithmetic (i.e., housekeeping) functions in the calculator. These functions inc interrogating the keyboard, keeping a record of the system status reports, synchronizing the system, and modif instruction addresses.

The keyboard is arranged in a five-column, eight-row (seven in the Model 5) matrix. It is scanned continually by the (circuit. When contact is made between a row and a column by pressing a key, a code, corresponding to that row column, is stored in the C&T. Then, at the appropriate time, the code is transmitted over the instruction address (Ia) to the ROMs. This code is the starting address of a program in ROM to service that key. Key bounce and lockout handled by delays programmed into the ROMs. The Model 5 keyblock is also scanned by the C&T. When a keyblock is pressed, a signal is generated on the mother board to inform the C&T that a keyblock ROM is required to service key. The I/O processor is then used to control the flow of data to ensure that the appropriate keyblock ROM is acce using the keycode from the C&T.

In all digital systems, status bits or flags are used to maintain a record of past events. In this system, there are tw status bits, all located in the C&T. They can be set, reset, or interrogated by microinstructions from the ROMs. The A also stores data which indicates the user-selected calculator modes of operation (e.g., display mode).

ROM addresses are updated in the C&T and sent serially to the ROMs over the Ia line. During execution of a bra instruction, the appropriate signal — arithmetic carry or status bit — is tested to determine whether the incremer address or the branch address should be selected next.

A powerful feature of the serial organization is the ability to operate on just a single digit of a number as it fl through the arithmetic unit. The C&T contains a pointer register and a word-select circuit which issues a word-se signal (WS) corresponding to the digit(s) being operated on (see Figure 2-2). The value of the pointer register can be incremented, or decremented by ROM instructions.

Read-Only-Memory

Preprogrammed mathematical routines are stored in the ROM circuits, each of which contains 256 instructions of 10 each (2560 total bits per ROM). A specific select-code is assigned to each ROM, and only one ROM can be active at time. When a ROM-select instruction is issued, a decoder inside of each ROM checks the select-code field of instruction. In case of a match, the selected ROM's output is switched on, and all other ROM's outputs are switched Therefore, each ROM must 'listen' to all instructions on the Is bus.

A timing circuit on each ROM is synchronized to the SYNC signal issued by the C&T as the calculator is switched (This circuit then keeps the ROM circuit running synchronously with the rest of the system.

A ROM address register on each ROM receives the address sent out by the C&T on the Ia bus. The ROM then places corresponding instruction on the instruction bus, Is, provided the ROM is active (i.e., previously selected to out instructions).

The ROM circuit also issues word-select signals, WS, for certain arithmetic instructions.

Since all ROMs in the system are connected in parallel, space is conserved by placing four ROMs in one package, cal quad-ROMs. This requires, however, not only ROM-select decoding circuits for the individual ROMs, but also group-sel decoding for pairs of quad-ROMs (two quad-ROMs or eight single-ROMs constitute one ROM group).

Arithmetic and Register Circuit

The Arithmetic and Register Circuit (A&R) executes instructions coming in bit-serially on the Is bus. All arithmetic instructions must be enabled by WS, the word-select signal. Data to be displayed is sent to the LED anode-driver on five lines, A thru E, and the START (SRT) line. One CARRY line transfers carry/borrow information back to the C&T. The BCD output is bidirectional; BCD digits are transferred into and out of the A&R to the I/O processor and data storage circuits.

The A&R circuit is divided into five areas: an instruction storage and decoding circuit, a timing circuit, seven 56-bit registers, an adder-subtractor, and a display decoder.

Three of the seven registers are working registers (see Figure 2-5). One of these and three of the remaining four registers form a four-register stack. The seventh register is an independent register for storage of calculator mode information (e.g., display mode). There are numerous interconnections between registers to allow for such instructions as exchange, transfer, rotate stack, and so on. An advantage of the bit-serial structure is that these interconnections require only one gate per data line.

Transfers into or out of the stack or the mode register are always whole-word (56-bit) transfers. All other arithmetic instructions are controlled by the word-select (WS) signal. For example, it's possible to interchange only the mantissa and sign of two registers, (see Figure 2-2) or to add any two corresponding digits of two registers.

The adder-subtractor computes the sum or difference of two decimal numbers. It has two data inputs, storage for carry or borrow, and sum and carry/borrow outputs. For the first three clock times, the addition is strictly binary. At the fourth clock time, the binary sum is checked, and if the answer is more than 1001 (nine), then the sum is corrected to decimal by adding 0110 (six). For example, the BCD equivalent of twelve (1100) is twelve (1100) + six (0110) or two (0010) with a carry to the next significant digit. The result is then entered into the last four bits of the receiving register and the carry is stored. A similar correction is done for subtraction. Carry information is always transmitted, but is recorded by the C&T only at the last bit time of the word-select signal.

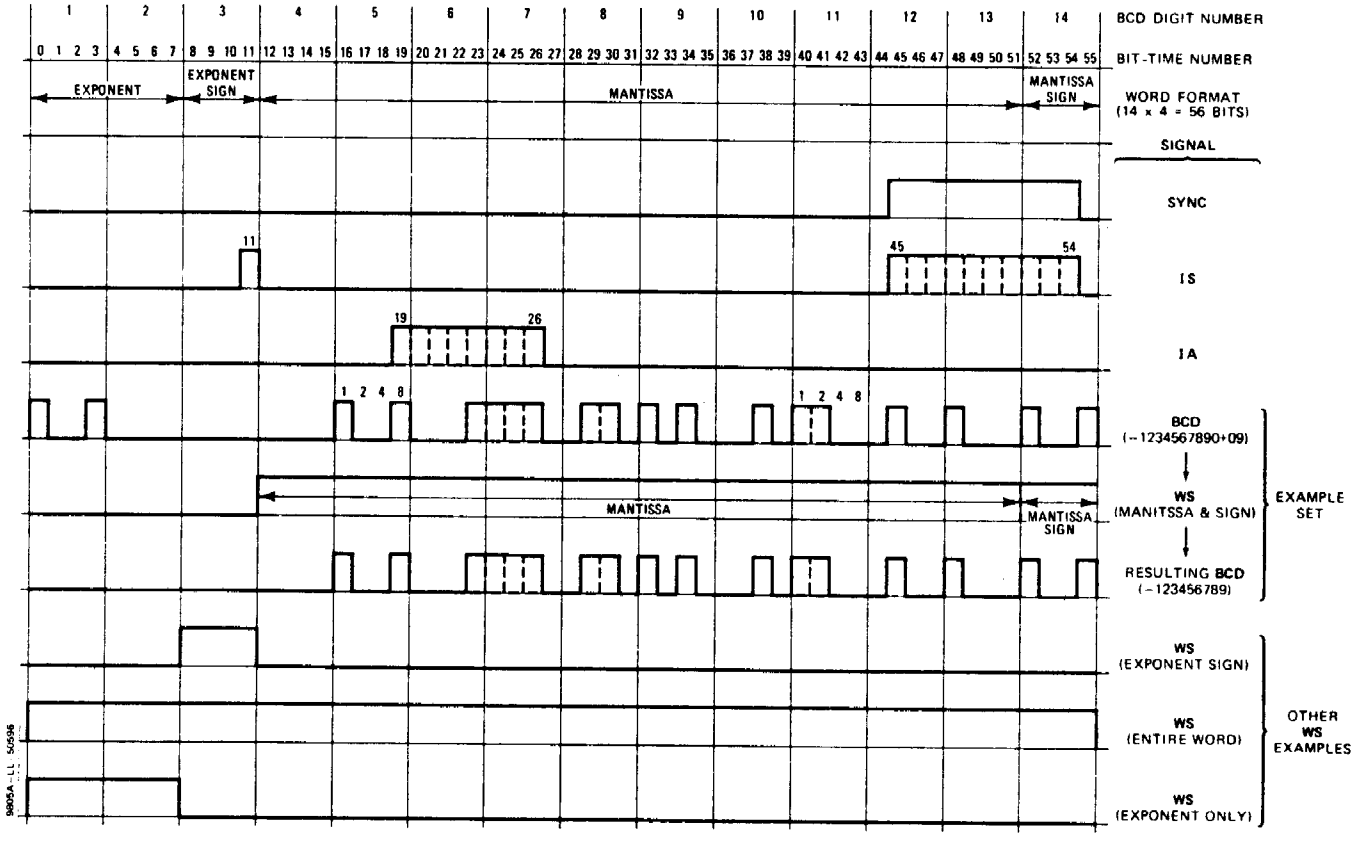


Figure 2-2. An Example of the WS Signal on BCD Data Being Operated On

I/O Processor Circuit

The I/O processor circuit has four primary functions in the calculator system:

- To expand the basic instruction set, thereby increasing the number of microinstructions available for the sy
- To provide additional timing and drive signals for the implementation of the SEIKO printer.
- To provide a binary arithmetic-unit for the system.
- To interface to the optional Model 5 circuits, which may also contain ROMs.

In this system, the Is bus is interrupted and divided into two separate lines: Is1 and Is2. The processor controls w line is being used. It is set to enable the Is1 line – the instruction line to the C&T and A&R – when power is swit ON. The processor is, however, constantly monitoring the instructions on the Is1 line. When a mainframe I instruction requires the use of the alternate instruction set, Is2, that set is enabled and instructions to the C&T and A circuits are disabled. The C&T and A&R are still operating, but are receiving no-operation instructions (all bits are lo 0s) on the Is1 bus. The processor performs the operations specified by the incoming ROM instructions until ar instruction is received, at which time instructions are again enabled to the C&T and A&R (see Figure 2-3).

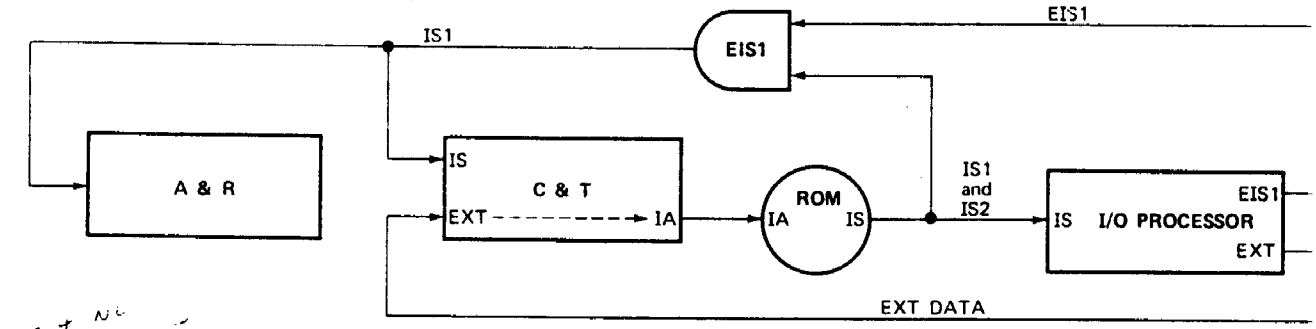


Figure 2-3. Simplified IS Bus Circuit

The processor, together with an external decoder circuit, provides the signals which enable the ROMs on the opti assemblies. Other signals are output from the decoder; these signals control the flow of data from the PROM and pl interface assemblies.

The SEIKO printer is a 'flying drum' impact printer; the printer characters are located on a cylinder (the drum) th continuously rotating. Printing occurs when a flat-faced hammer strikes the ribbon, forcing it against the paper whi immediately in front of the rotating drum.

The print-drum is organized into 18 columns and 13 rows; each row passes under the hammers approximately every msecs (see Figure 2-4). For printing to occur, the processor must actuate the desired printer electro-magnets so that necessary hammers strike the drum while the specified character, in each column, is passing through the printing area accomplish this, the processor correlates timing information from the calculator with print-drum position signals from printer. Using instructions from the ROMs, it outputs the correct signals to actuate the solenoids at the correct time.

The processor 'remembers' which row of characters is behind the hammers by incrementing a counter each time a passes through the printing area; the counter is reset after the last row passes through the area. The ROM instruct store 18 hexadecimal digits (one for each column) in two 14-digit shift-registers before the printing process begins. (of the 28 available digit-positions are not used during the printing operation.) One register is in the A&R, the other the processor. Then, after a print instruction is received, the processor actuates the hammer in each column when hexadecimal number stored in the digit position for that column matches the number in the counter. Printing will occur in any column in which the two numbers do not match. Spaces are provided when the hexadecimal number st in the associated digit position is 13 or greater. After the drum finishes one complete rotation, the processor recei then executes, an instruction to advance the paper one line.

The processor is also used to interface to the Model 5 optional assemblies by providing 10 output and 8 input/output data-lines to those assemblies. Also, by implementing an additional decoder circuit, the ROMs on the optional assemblies are enabled and the I/O-data control lines are provided. The binary arithmetic unit is mostly used in conjunction with the plotter interface assembly. When use of a PROM is necessary, the processor circuit uses ROM instructions to provide the initial PROM address, then increments the address after the keycode from the previous address has been completely serviced. The PROM output keycode is transferred, during the correct system bit times, from the processor circuit to the C&T circuit on the external (EXT) data line. The keycode is then used as a new address for the active ROM.

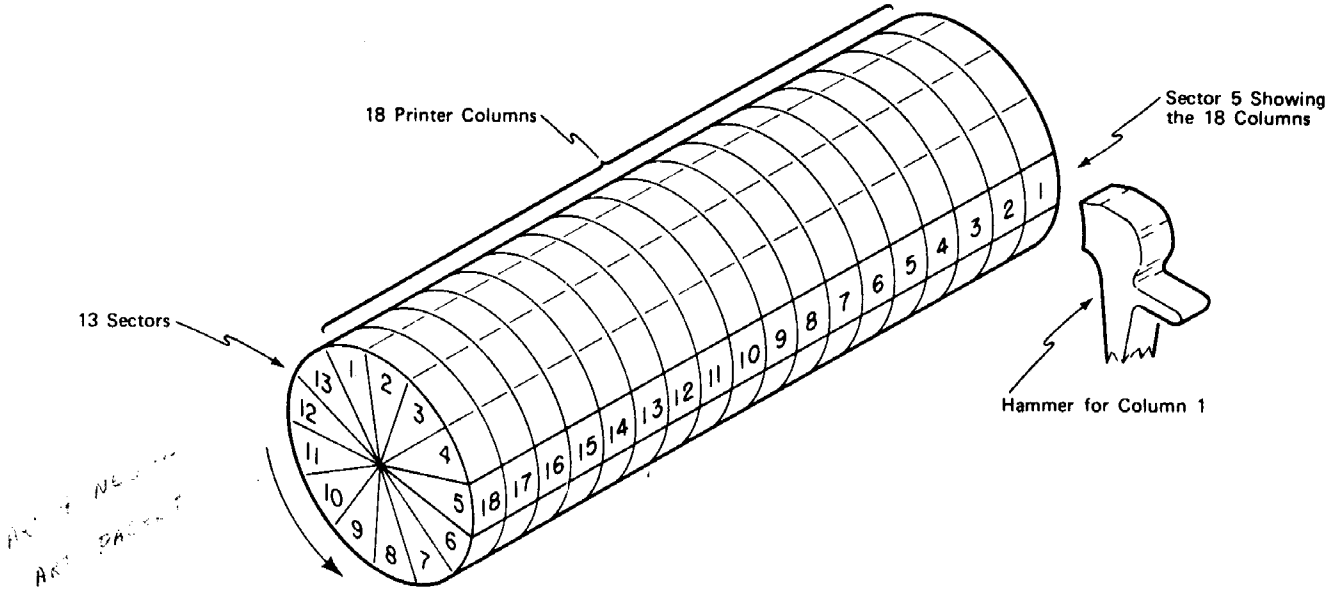


Figure 2-4. The SEIKO Print-drum

Data Storage Circuits

Each of the three MOS data storage units (ICs) contain ten, 56-bit shift registers. These circuits communicate with the A&R over the bidirectional BCD line; the storage circuits are addressed on the BCD line, they then transmit the data, in the designated register, to the A&R on the same line.

Each data storage unit has six pins which are hardwired on the circuit board to provide an individual address for that unit. Only the unit which has been correctly addressed on the BCD line will output the data from the register designated by the second part of the address.

Timing for the data storage assembly is provided by the START signal from the A&R.

9805A Optional Data Storage Board

Addresses are provided for the ROMs on the data storage board by the C&T via the processor. The data storage ROMs, in turn, provide the instructions and word-select signals to enable the use of the data in the storage registers.

Timing for the data storage ROMs is provided by the system clock signals and SYNC.

9805A Optional Plotter Interface

The eight I/O lines (C1 through C8) and four of the processor data-output lines (C10 through C13) are buffered on the interface and are then used as data inputs for the plotter. The control signals used to transfer the data to the plotter are decoded outputs of the processor, which, itself, is receiving instructions from the interface ROMs. Control is transferred to these ROMs by instructions from the main system ROMs which instruct the processor to issue a group I/O enable signal (GIOE), thus activating the interface's ROMs.

9805A Statistics Keyblock

The statistic keyblock keys are electronically overlayed on the main keyboard keys, and thus are scanned synchrono with those keys. When a stat-block key is pressed, however, an additional signal, FUNCTION BLOCK SELECT (FBS generated which sets the FLAG' signal. The processor subsequentially sets the FLAG signal which, in turn, sets statu 11 in the C&T. An ensuing system ROM instruction tests status-bit 11. When status-bit 11 is set, other instructions issued which instruct the processor to:

- disable instructions to the A&R and C&T from the main system ROMs.
- output a SELECT ROM-GROUP B (SRB) signal, thereby enabling the C&T address outputs (Ia) to the keybl ROMs.

Thus, the C&T, A&R, and processor all begin operating using the keyblock ROM instructions.

Display and Drivers

The display chip is a magnified five-digit cluster. Each digit has a spherical lens molded in the plastic cover.

The LED's are more efficient if they are pulsed at a low duty cycle rather than driven by a dc source. In this disp energy is stored in inductors then 'dumped' into the light-emitting diodes. This drive technique allows a high degre multiplexing; the digits are scanned one at a time, one segment at a time.

The anode driver generates the two-phase system clock and the segment (anode) drive-signals, decodes the data from A&R, inserts the decimal point, and sends shift signals to the other axis of the multiplex circuitry (i.e., the cath driver). The cathode driver contains a 15-position shift register which is incremented for each digit position while anode driver is scanning that digit. The entire 15-digit display is scanned once each word-time and is then reset to dig by the START signal from the A&R circuit.

The Model 81 Buffered Keyboard

The Model 81 Opt. 003 Display and Opt. 002 Father boards contain a 9x64-bit random-access buffer. This buffer rece the key-down (KD) inputs from the keyboard together with the C&T's KS outputs and, when the calculator is not bu sends the key-down (KD) information, in the same order in which they originally occurred (i.e., first in, first out), to C&T. The circuit uses the IOC1-IOC3 and SCE signals to determine when the calculator is busy.

The 9 bits of data stored for each of the 64 keys are 5 KD signals, 3 encoded KS signals, and KS0. When the calculato ready to accept a key input, the encoded KS bits together with KS0, are compared to the C&T KS bits to ensure that keycode is output to the C&T only during the correct calculator bit-times. When the current KS outputs are identical the KS outputs when the key was pressed, the previously stored KD data is input to the C&T.

Key bounce is eliminated by a 10 msec one-shot which is triggered by a key-down detector. Other circuits are required ensure that the buffer does not interfere with other C&T operations and to permit the use of either a MOSTEK or AMI C&T.

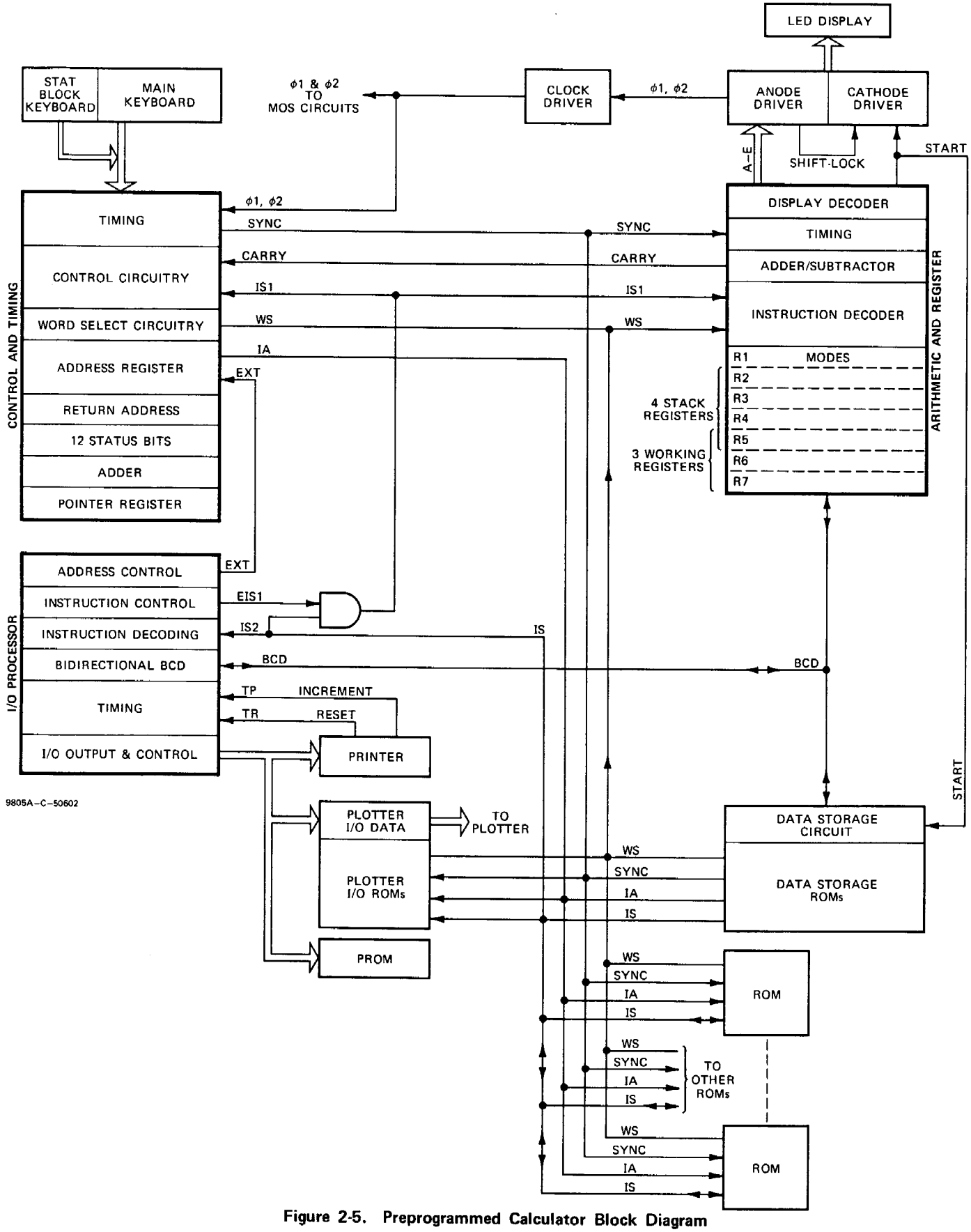


Figure 2-5. Preprogrammed Calculator Block Diagram

Table 3-0. Chapter 3 Quick Reference

SUBJECT	DESCRIPTION	REFERENCE PAGE
SYSTEM POWER-UP	Power supplies Generating PWO The power-up routine - a series of instructions that prepare the calculator for user-initiated operations.	3-3 3-3 3-3
DISPLAY-WAIT LOOP	A routine the calculator enters, whenever calculations are not being performed, during which the keyboard is tested for a key-down and the results of the previous operation are displayed.	3-3
GENERATING KEYCODES	Keyboard operation with the C&T when a key is pressed.	3-4
KEYDOWN PREPARATION ROUTINE	A sequence of ROM instructions to prepare the calculator for the acceptance of a keycode.	3-5
SERVICING KEYBOARD INPUTS	The instruction address (Ia) corresponding to the key which is down is generated in the C&T, then input to the ROMs.	3-5
THE ROM INSTRUCTIONS	The instructions (Is) output by the ROMs control the A&R, C&T, and I/O processor operations. The instructions are also input to the other ROMs so that system control can be switched back-and-forth between ROMs.	3-6
THE I/O PROCESSOR	The processor provides printer control.	3-6
THE DISPLAY CIRCUITS	The anode & cathode drivers decode the time-shared A&R outputs to provide the correct display. The anode driver also provides the system clock signals.	3-7
THE A&R BCD OUTPUTS	The A&R's BCD port is the only method of looking at data in the calculator.	3-8
THE MODEL 81 BUFFERED KEYBOARD	The keyboard buffer provides temporary storage for keycodes.	3-9

CHAPTER 3
MODELS 46 AND 81 THEORY OF OPERATION

INTRODUCTION

The information contained in this chapter describes the Model 46 and Model 81 Calculator 'system' operation rather than the operation of each individual circuit. Information contained in Chapter 2 briefly describes the individual circuits; you must have a thorough understanding of that information before continuing with this chapter. Chapter 4 provides the theory of operation for 9805A Calculators.

Figure 3-6 is a block diagram of the Model 46 and Model 81 Calculator system and shows the signals used in the system, their originating device, and destination. That information will be useful during the remainder of the chapter.

LOGIC DESCRIPTION

The logic levels used in the Model 46 and Model 81 Calculator systems are ØV and +6V, except for the clock driver outputs which are +6V (logical Ø) or -12V (logical 1).

Both negative- and positive-true logic is used in the system. Negative-true logic signals are shown as the signal name or mnemonic with a bar across the top of the characters; these signals are a logical 1 at ØV levels. Positive-true logic signals do not have the bar across the top of the characters; these signals are +6V when true.

Table 3-1 lists the mnemonics and the associated signal names which are used in the Model 46 and Model 81 Calculator systems.

Table 3-1. The System Signal Mnemonics

MNEMONIC	NAME	FUNCTION
ADV	Advance	paper advance signal to the printer
BCD	Binary-coded-decimal	BCD input/output line to A&R from all data storage circuits and the I/O processor
C1 thru C20	Data C1 thru Data C20	I/O processor data outputs to the printer electromagnets via the drivers
Col 1 thru Col 18	Column 1 thru Column 18	printer electromagnet-driver outputs to enable hammers
CRY	Carry	carry information to the C&T from the A&R
Data A thru Data E	Data A thru Data E	Encoded display information from A&R to display circuits
EIS1	Enable Instruction Set 1	signal from I/O processor used to enable instructions from the ROMs to the A&R and C&T
EXT	External data	data input line from the I/O processor to the C&T
FLG'	Flag Prime	this signal is an input to the I/O processor when a keyboard key is pressed which affects all subsequent operation (e.g., PRINT OFF)
FLG	Flag	a processor output to the C&T which is set by the processor FLG' input

Continued

Table 3-1. The System Signal Mnemonics (Cont'd)

MNEMONIC	NAME	FUNCTION
Ia	Instruction Address	an eight-bit input to the ROMs which contains the ROM-address information from the C&T
IOC1-3	Input/Output codes, bits 1 thru 3	processor outputs used as 'system busy' indicators
Is	Instruction	ROM pre-programmed outputs
Is1	Instruction Set 1	instructions which are input to the processor, C&T, and A&R
KD	Key-down	signal from keyboard to C&T indicating a key is down (LSD of Ia)
KS	Key-select	signals to the keyboard from the C&T (MSD of Ia)
DECIMAL	Manual Decimal Point	Model 81 signal used to indicate the position of the DECIMAL/AUTO· key
PWO	Power-on	logic signal used to preset the system when power is switched ON
Φ1	Phase 1	first phase of the 2-phase clock signal (170 KHz)
Φ2	Phase 2	second phase of the 2-phase clock signal
RED	Red Ribbon	red ribbon select signal which enables the appropriate printer solenoid
RESET	Reset	print-drum row 0 indicator, used to generate TR signal
SCE	Select Code Enable	strobe pulse used to enable coded I/O bits (IOC1-IOC3)
SRT	Start	word-time bit-0 indicator from A&R
SYNC	SYNC	word synchronization signal
TP/TL	Printer timing	print-drum row timing indicator, used to generate TP
TP	Printer timing/ time clocked	printer timing pulse which is phase locked to system. Used to increment row counter in the processor
TR	Timing reset	a processor input from the printer used to reset the hexadecimal counter to 0
WS	Word Select	signal from either a ROM or the C&T used to enable the portion of a word to be operated on by the A&R

SYSTEM POWER-UP

Of the four power supplies (+6V, +10V, +15V, and -12V) the +6V supply powers-up first to ensure that the system clock is operating before the MOS/LSI logic. The +10V supply, which generates the +7.5V and +3.75V supplies, is used by the display circuits. The +15V supply is used only by the printer. The +6V and -12V supplies provide power for the MOS circuits.

> **NOTE**
> The CMOS logic in the Model 46 and the Model 81 use +6V for power.

Generating PWO (Power-On)

When the C&T receives power, the two-phase system-clock inputs from the Father Board or, if installed, the Display Board cause the circuit to begin sequencing and, subsequently, the first SYNC signal is generated. The SYNC signal clocks flip-flop U18B, which generates the signal PWO. While PWO is 0 volts, the SYNC signal, together with Φ1 and Φ2, are synchronizing the system.

The PWO signal is used to:

- set the logic to a predetermined state before system operation begins.
- delay any system operations for at least 500 msec to allow time for the print-drum to obtain its normal operating speed.
- preset the ROMs; only ROM 0 of group A is activated and can output instructions when PWO is released.
- preset the I/O processor to Enable Instruction-Set One (EIS1), thereby ensuring the instruction outputs of the ROMs are input to the A&R and C&T.
- hold the C&T's Ia (address) outputs at logical 0; the C&T attempts to output incremented addresses each word time, but the Ia line is held at a logical 0 by the PWO signal.

Before PWO is released, the system is fully synchronized and the print-drum is rotating at its normal operating speed. Thus, when PWO is forced to +6V by the first SYNC signal after the 'D' input of U18B is high, the system can begin processing data.

The Power-Up Routine

Since address zero is present on the Ia line and ROM 0 of group A is selected, the instruction in address 0, of ROM 0 in group A, is the first instruction executed by the system. Together with the ensuing instructions, this instruction preconditions the system for subsequent, user-initiated operations. The preconditioning, or power-up, routine determines the display format, the information in the display (zeros), and it causes CLEAR to be printed. The final instruction in the routine branches the system to a set of instructions which are used as a 'display-wait loop'.

While the power-up routine is being executed, the calculator ignores any key which is down. The power-up instructions do, however, interrogate the status of the PRINT OFF key. Once the status of the PRINT OFF key has been tested, the system assumes that it will not be changed until after the print instructions have been completely executed. If the PRINT OFF key is pressed during any printing routine, power to the printer is removed, thereby removing the timing signals to the I/O processor circuit. Thus, the processor is disabled sometime during the print cycle (e.g., while the processor is being prepared to print CLEAR), which may 'hang-up' the system or result in otherwise unexpected operations.

THE DISPLAY-WAIT LOOP

When the power-up instructions have been completed – *or any other time the system is idle* – , the system exits to a set of ROM instructions, called the display-wait loop, during which the system continually searches for a 'key-down' condition. Until a key-down occurs, information in the A&R circuit is continuously recirculated and displayed while the remainder of the system is idle. When a key, other than the DECIMAL key or the PRINT OFF key, is pressed, a status bit (0) in the C&T is set and the octal equivalent-code for that key is loaded into the C&T's buffer register. Then, the wait loop instructions are exitted and a set of 'key-down preparation routine' instructions are accessed.

The DECIMAL and PRINT OFF keys do not affect the wait loop. These keys are tested each time a data entry or printing operation is begun.

GENERATING KEYCODES

The keyboards are electronically constructed as a 5X8 matrix of switches. When a key is pressed, it connects one of eight key-select lines (KS) to one of the five key-down lines (KD) (see Figure 3-1).

> **NOTE**
>
> Model 81 Calculators with either Option 2 or Option 3 installed contain a keyboard buffer and operate somewhat differently; see 'THE MODEL 81 BUFFERED KEYBOARD' at the end of this chapter.

The eight KS lines are sequentially driven by a 3-bit to 8-bit decoder in the C&T; the decoder inputs are the three significant bits (LSB) of the C&T's 56-bit counter. Thus, each KS line is driven once each eight bits of the system 5(word (i.e., 7 times each word). When a key is down, the pulses on the KS line corresponding to that key are couple the associated KD line, then input to a data selector in the C&T.

The data selector uses the three most significant bits of the 56-bit counter to sequentially select each KD line; each lir selected once each word time. When the KD line being selected is pulsed by the decoder, via the associated KS line, data selector transfers the input signal to its output. This signal is then used to load the keycode-buffer register with six outputs of the 56-bit counter; 16 states of the counter are not used. The output of the data selector is also use set status-bit 0, the key-down status bit, in the C&T. Status-bit 0 must be reset — that is, the key must be release before subsequent keys are accepted.

The keycode-buffer register is loaded with the same octal keycode once each word-time until the key is released. keycode in the buffer register is, however, not loaded into the address register until the C&T receives a ROM instruc to do so; the instruction for that operation is contained in the 'key-down preparation routine' instructions (descr next).

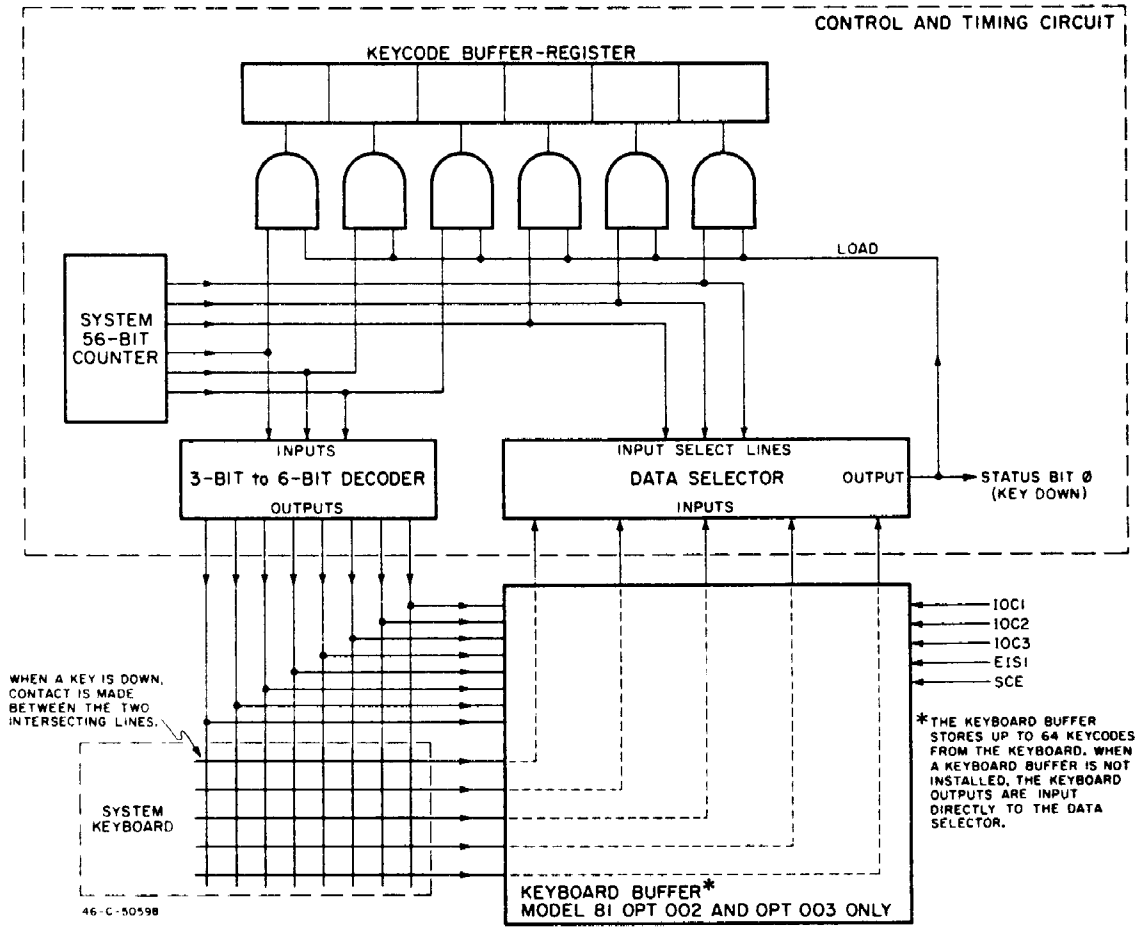


Figure 3-1. The Keyboard Scanner

KEY-DOWN PREPARATION ROUTINE

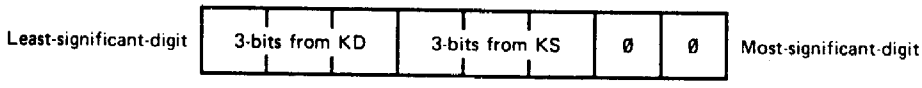
When a keyboard key, other than DECIMAL or PRINT OFF, is pressed, a keycode corresponding to that key is generated (see 'Generating Keycodes') and status bit 0 is set. The ROM instructions in the display-wait loop continually test status bit 0 to determine if a key has been pressed. When status bit 0 is set, the system exits the wait loop and enters the key-down preparation routine. The primary functions of this routine are:

- to provide a software-controlled delay to ensure the key entry was not due to keybounce.
- to blank the display.
- to prepare the A&R, C&T, and the I/O processor to perform any instruction required to service the key which is down.
- to test a status-bit which is set by the SHIFT key. If that bit is set, an instruction is issued to activate a particular ROM. If the bit is reset, another instruction activates a different ROM. The ROM activated by this process contains the first instruction for servicing the keycode in the keycode-buffer register. (ROM selection is described later in this chapter.)

Upon completion of the preparation routine -- which may require up to 60 word times -- the calculator system is ready to service the keycode in the user-defined display mode of operation.

SERVICING THE KEYBOARD INPUTS

The final instruction in the preparation routine loads the keycode from the C&T's buffer register into the address register. Two bits are added to the six-bit keycode by hardware in the C&T to make the eight-bit instruction address (Ia). Both bits are zeros and are placed in the two most significant bit positions. The eight- bit address, in the address register, is in the form:



The C&T outputs the address (Ia) from the address register to the ROMs during bit-times 19 through 26 of the ensuing word (i.e., the first word after the completion of the preparation routine). This address is stored in the address register of all ROMs in the system. Each ROM decodes the address and, at bit-time 44, the instruction specified by the address is loaded, in parallel, into each ROM's instruction register. Only the active ROM -- that is, the ROM which was selected during the preparation routine -- can, at this time, output the instruction (Is) from the instruction register.

A SUMMARY OF THE PRECEDING INFORMATION

Before continuing, let's briefly summarize the operations which have previously taken place.

- Initially, the calculator was OFF. When the unit was switched ON, the system began synchronizing and PWO was generated to preset the system and to delay subsequent operations until the printer was ready.
- Next, a routine was entered that set up the correct display and printed CLEAR (unless the PRINT OFF key was down).
- The calculator then entered a wait loop. During this time, the display was on and a continual test for a key-down condition was taking place.
- When a key was pressed, the calculator exitted the wait loop and began a keydown preparation routine during which the system was prepared to accept the 6-bit keycode stored in the C&T. The last instruction in the routine activated the correct ROM and loaded the keycode into the C&T's address register; while loading the keycode into the address register, two zeros were added to complete the 8-bit address.
- Finally, after completion of the preparation routine, the keycode was loaded into each ROM's address (Ia) register and, at bit-time 44, the instruction in the specified address was loaded into each ROM's ten-bit instruction register.

Until this time, the operations performed by the calculator have been reasonably well defined. From this time on, however, the instructions define the operations performed by the calculator; each instruction differs from each other instruction, depending upon the requirements of the problem being solved.

CHAPTER 3
MODELS 46 AND 81 THEORY OF OPERATION

THE ROM INSTRUCTIONS

A Word About the First Keycode-Instruction

Let's discuss the instruction, just loaded into the instruction register, for a moment.

Since only 5 key-down and 8 key-select lines are used, only 40 (8X5) instructions can be accessed by keycodes the keyboard. All of those instructions are clustered within one ROM (one ROM is active for shifted keys, an for unshifted keys). All keycodes, however, require more than a single instruction to perform the required operat Therefore, each keycode eventually addresses a ROM-select or branch instruction to actually access the routin service that key. Some of those routines may contain additional branch or jump-subroutine instructions to con servicing the key.

The Instruction

Each ROM contains 256 (2^8) instructions (Is), each of which is accessed by a different instruction address (Ia). and only one instruction is output, bit-serially, during bit-times 45 through 54 of each word. Those instructions:

- are decoded by the issuing (active) ROM and, if the operation is arithmetic, 3-bits of Is determine whi the 6 possible WS signals is output to the A&R during the ensuing word-time. (Two types of WS si originate in the C&T during arithmetic operations).
- are decoded by the inactive ROMs to provide an arrangement whereby control can be switched from one to another. Only one ROM in the system is active (i.e., outputting instructions) at one time. The addre the ROM-select instruction is incremented in the C&T, then used as the selected ROM's instruction ad (Ia).
- are decoded by the C&T, thereby providing control of the C&T operations and also providing branch subroutine instruction addresses for the system. (The return address of subroutine operations is the increme address of the subroutine instruction. It is stored in the C&T until it is required for the return.)

  Other instructions are decoded by the C&T word-select outputs. This occurs only during certain arithr operations performed by the A&R circuit. The C&T word-select signals either specify a single digit operatio an operation on all digits less than a specified digit number; WS from the C&T can never specify operation the center portion of a word.
- control of the A&R. Data is placed in the A&R registers either by arithmetic operations or by exchanging between registers. BCD data can be input or output to the A&R by additional instructions.

  The BCD data in each of the seven A&R registers can be exchanged or transferred using other instructions arithmetic operations in the calculator are accomplished in the A&R by arithmetic instructions. T instructions, and only these instructions, require a WS input signal during the ensuing word-time.
- toggle the display information to the display circuits. Yet another instruction must be used to disable information to the display.
- control the I/O processor which, in turn, controls the printer and the 'Busy' light.

THE I/O PROCESSOR CIRCUIT

When a printout is necessary, instructions are used to load the row (or sector) hexadecimal number of the de character into selected digit positions in two 56-bit registers; each digit position corresponds to one column on print-drum. (One of the two 56-bit registers is located in the A&R circuit.) When the ROM-generated hexadec number in each digit-position corresponds to the hexadecimal print-drum row number, the hammer in corresponding column is activated.

The I/O processor always 'listens' to the instructions on the Is bus. Some instructions, however, are ignored by processor while others instruct the processor to disable instructions to the A&R and C&T circuits.

When the system is busy performing an operation, two processor outputs, SCE and IOC3 are used to switch the Light on (SBL).

Finally, the status of the DECIMAL and PRINT OFF keys are tested and the results recorded in the A&R and by the processor. The processor receives an instruction to test one of those keys, then outputs an enable signal wh if the key is down, forces the FLG' line to a logical 1. The resulting logical 1 FLG signal then sets status-bit 1 the C&T, thereby causing a ROM instruction to be issued that performs the appropriate operation. (The PRINT key, when pressed, also removes power to the printer.)

THE DISPLAY CIRCUITS

The System Clock

One of the functions of the anode driver circuit is to provide the two-phase clock pulses shown in Figure 3-2. With the exception of two externally-connected timing components, the anode driver contains all of the circuits necessary to perform this function. Systems which do not contain the anode driver utilize discreet components for the clock circuit; these components are located on the Father Board (A4). The two-phase clock frequency is 170 KHz.

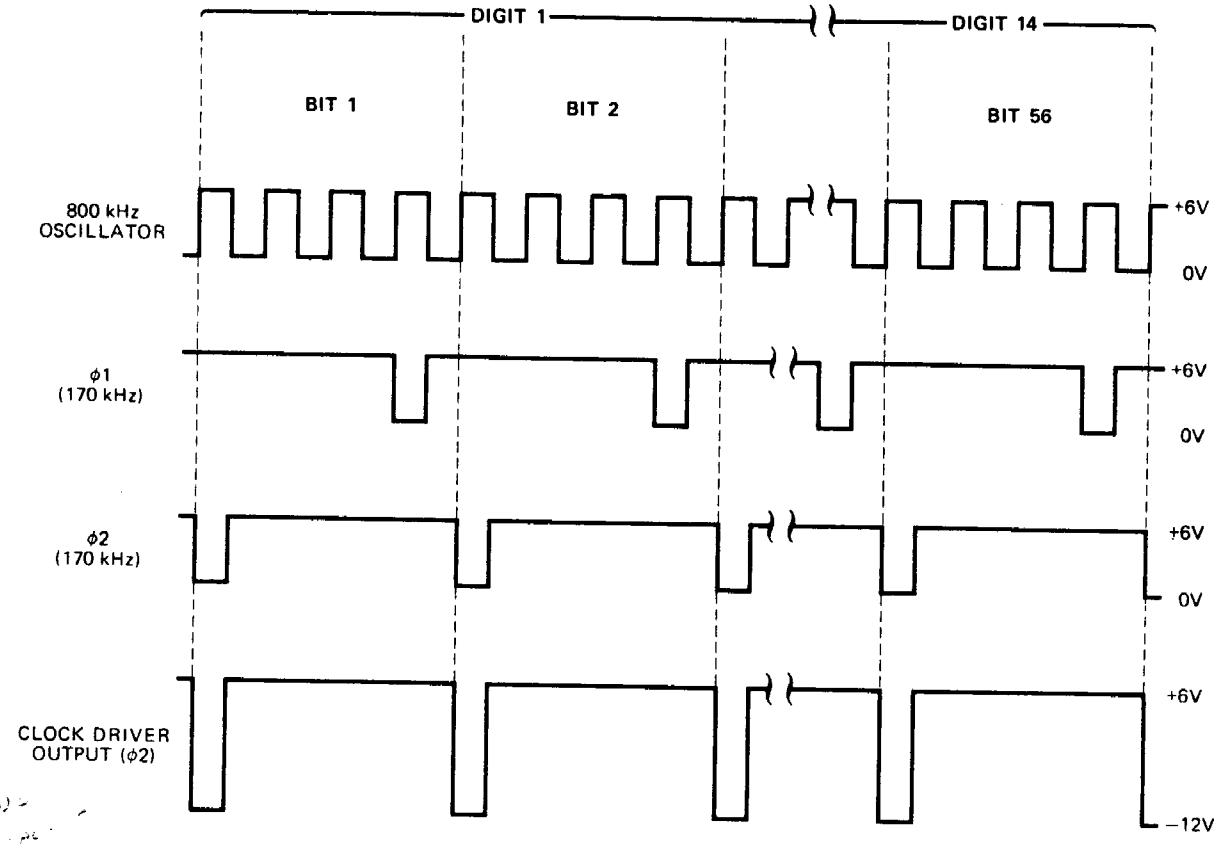


Figure 3-2. System Two-phase Clock Signals

The Anode and Cathode Drivers

The multiplexed Data A through Data E information, which is output by the A&R, is input to the anode driver. The anode driver demultiplexes the information and drives the anode of the appropriate display LEDs; each LED is one segment of a digit (see Figure 3-3). The anode driver provides drive for the same segments in each of the 15 display digit positions. The cathode driver, however, selects a single digit position for displaying the information.

When the anode driver has completed the display of a digit (i.e., after four system bit-times), it outputs a shift-clock pulse to the cathode driver. The cathode driver then enables the next digit (to the left) for displaying the ensuing A&R Data A through Data E outputs. Two consecutive shift-clock signals are output during any digit which is followed by a decimal point; the decimal-point data is output by the A&R at the same time as the preceding digit-data. This results in a 15-digit display with only 14 digits in the system-word. Digits which are blank are treated the same as other display digits, except when the anode driver decodes the A&R circuit outputs, no LED anodes are driven.

The START signal from the A&R circuit resets the cathode driver's digit counter, thereby setting the cathode driver to digit-position one.

The 'Busy Light' is switched on or off by the I/O processor circuit using instructions from one of the ROMs.

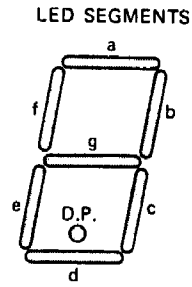
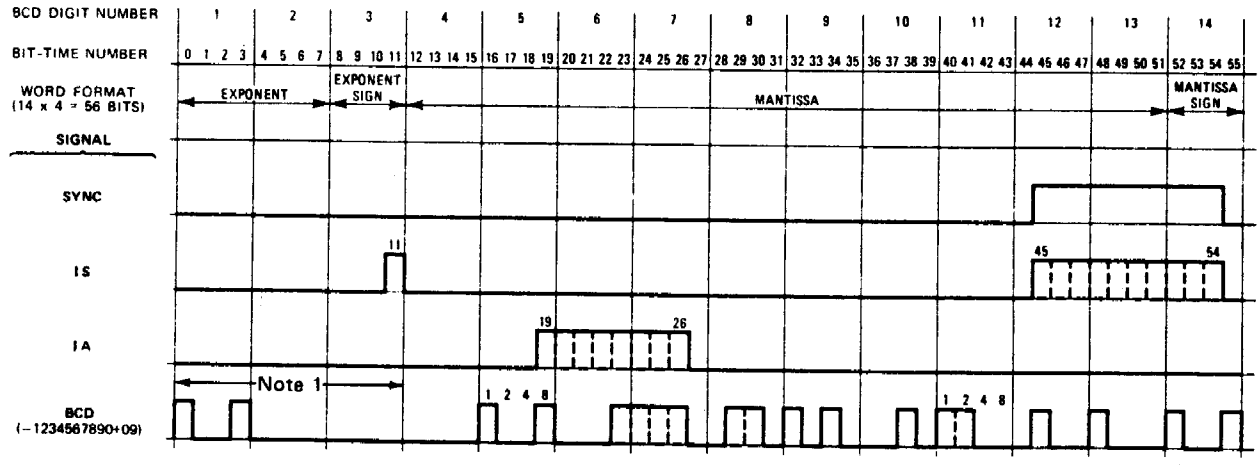


Figure 3-3. The Segments of Each Display Digit

THE A&R BCD OUTPUTS

The only method of 'looking' at information in the system is to use an oscilloscope, synchronized to either STA (bit 0), or the trailing edge of SYNC (i.e., bit 54), to monitor the BCD line on the A&R. Since the BCD data in A&R is recirculated once each word-time when the calculator is not busy, that data can be seen on the BCD out Figure 3-4 shows an example of data on the BCD line when the display is:

Note again that negative exponents are handled by the A&R in the ten's-complement notation.



NOTE 1: When a negative exponent occurs, the system handles the exponent in the ten's-complement notation (see Figure 2-1 in Chapter 2).

Figure 3-4. Looking at the BCD Information

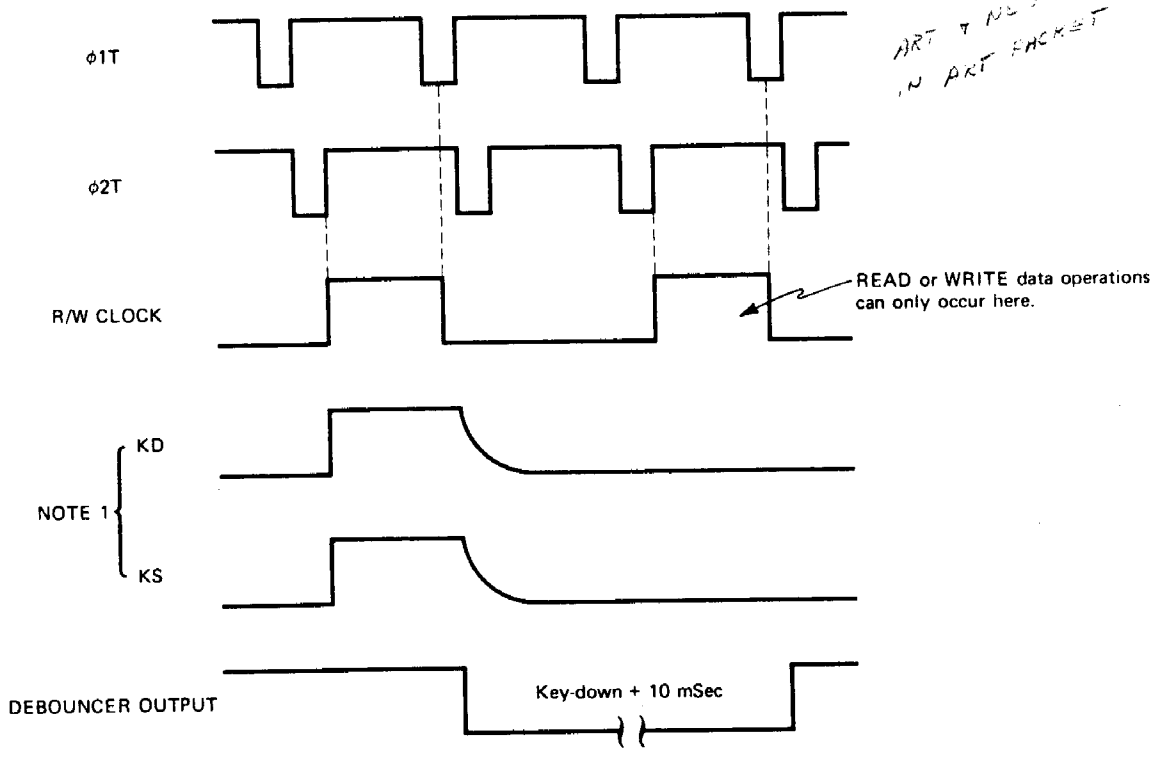
THE MODEL 81 BUFFERED KEYBOARD

The buffered keyboard circuits, located on both the Opt 3 Display and the Opt 2 Father Boards, interrupt the KD signals between the keyboard and the C&T and, at the same time, monitor the C&T's KS outputs (see Figure 3-1).

When a key is down, a 10 msec one-shot is triggered to protect against keybounce. Then, the keyboard's KD signals, together with encoded KS signals from the C&T, are stored in one address of a 9X64-bit, random-access memory (RAM). Up to 64 encoded keycodes can be stored in the buffer.

The data in the buffer is output only when two conditions are met. First, the calculator must *not* be busy processing any previous inputs, as indicated by the states of the IOC1, IOC2, IOC3, EIS1, and SCE data. Second, the C&T's KS outputs, when encoded by the buffer circuits, must be identical to the KS data stored in the RAM. When those conditions are met the calculator is ready to accept the KD data from the buffer and the KS data for the keycode (i.e., the system bit-time) is correct. The KD information first input to the buffer is then output to the C&T. This process continues, with the buffer sequentially outputting KD information on a first in first out basis, until the RAM is empty.

To implement the use of the keyboard buffer, R/W Clock, R/W Control, Key-down Detector, Debouncer, KS Encoder, and KS Comparitor circuits are used. All of these circuits, together with the RAM, are contained on either the Father Board or Display Board, whichever is installed. Figure 3-5 is a timing diagram of the buffer circuits.



NOTE 1: The actual KD & KS signals seen depend upon whether a MOSTEK or AMI C & T is being used. In either case, the signals are NOT precisely as represented here.

Figure 3-5. The Keyboard Buffer Timing

–NOTES–

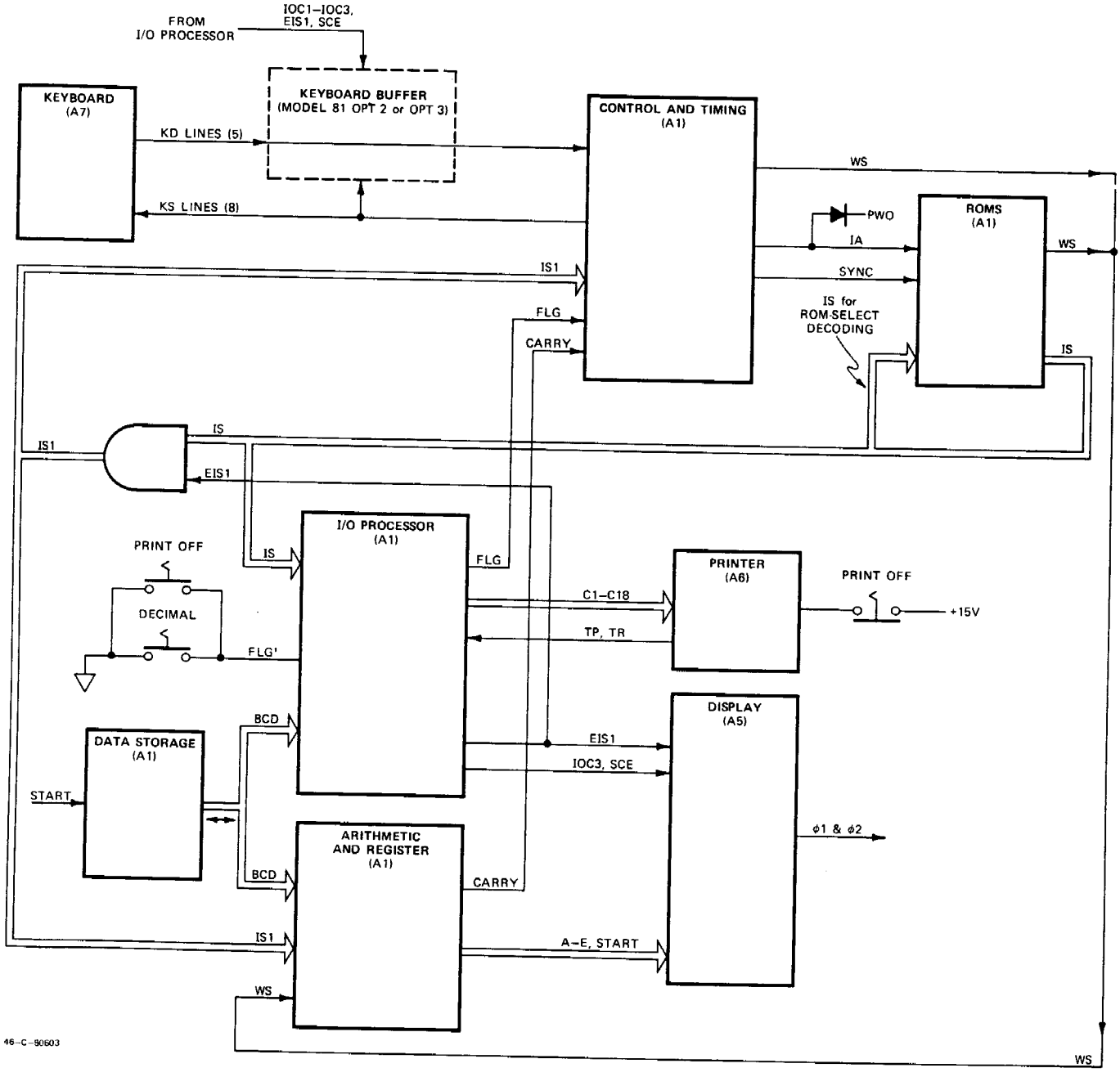


Figure 3-6. Models 46 and 81 Block Diagram

Table 4-0. Chapter 4 Quick Reference

SUBJECT	DESCRIPTION	REFERENCE PAGE
SYSTEM POWER-UP	Power supplies Generating PWO The power-up routine - a series of instructions that prepare the calculator for user-initiated operations.	4-5 4-5 4-5
DISPLAY-WAIT LOOP	A routine the calculator enters, whenever calculations are not being performed, during which the keyboard is tested for a key-down and the results of the previous operation are displayed.	4-5
GENERATING KEYCODES	Keyboard operation with the C&T when a key is pressed.	4-6
KEYDOWN PREPARATION ROUTINE	A sequence of ROM instructions to prepare the calculator for the acceptance of a keycode.	4-7
SERVICING KEYBOARD INPUTS	The instruction address (Ia) corresponding to the key which is down is generated in the C&T, then input to the ROMs.	4-7
THE ROM INSTRUCTIONS	The instructions (Is) output by the ROMs control the A&R, C&T, and I/O processor operations. The instructions are also input to the other ROMs so that system control can be switched back-and-forth between ROMs.	4-8
THE I/O PROCESSOR	The processor provides printer control, as well as control of the Model 5 Options.	4-8
THE DISPLAY CIRCUITS	The anode & cathode drivers decode the time-shared A&R outputs to provide the correct display. The anode driver also provides the system clock signals.	4-9
THE A&R BCD OUTPUTS	The A&R's BCD port is the only method of looking at data in the calculator.	4-11
MODEL 5 OPTIONS	The MODEL 5 Options input or output data to the system via the I/O processor.	4-11

CHAPTER 4
9805A THEORY OF OPERATION

INTRODUCTION

The information contained in this chapter describes the 9805A Calculator 'system' operation rather than the operation of each individual circuit. Information contained in Chapter 2 briefly describes the individual circuits; you should have a thorough understanding of that information before continuing with this chapter. The Models 46 and 81 Theory of Operation is contained in Chapter 3.

If you are already familiar with the information in Chapter 3 only those sections which are preceded by a ■ symbol need be read. Those sections contain information, usually shown in italics, which differs from the information in Chapter 3.

Figure 4-5 is a block diagram of the 9805A calculator system and shows the signals used in the system, their originating device, and destination. That information will be useful during the remainder of the chapter.

■LOGIC DESCRIPTION

The logic in the 9805A system requires that both MOS and bipolar logic levels be used; bipolar logic levels are 0V or +5V, whereas MOS-circuit logic levels are 0V or +6V. The clock driver outputs are +6V and -12V.

Both negative- and positive-true logic is used in the system. Negative-true logic signals are shown as the signal name or mnemonic with a bar across the top of the characters; these signals are a logical 1 at 0V levels. Positive-true logic signals do not have a bar across the top of the characters; *these signals are either +5V or +6V, depending on the type of logic circuits in use,* when true.

Table 4-1 lists the mnemonics and the associated signal names which are used in the 9805A system.

Table 4-1. The 9805A System Signal Mnemonics

MNEMONIC	NAME	FUNCTION
AUTO·	Automatic Decimal	AUTO· key down
$\overline{A}$	Not A	disable Is and WS from the mainframe ROMs to the A&R and C&T
ADV	Advance	paper advance signal to the printer (C19·C20)
$\overline{B}$	Not B	disable Ia to ROM group B
BCD	Binary-coded-decimal	BCD input/output line to A&R from all data storage circuits and the I/O processor
BDE	Binary Data Enable	enable signal for the BCD data from the system data storage circuits
$\overline{C}$	Not C	disable Ia to ROM group C
C1 thru C20	Data C1 thru Data C20	I/O processor data outputs to both the plotter I/O and printer electromagnets via the drivers. C1 through C8 are inputs from PROM
Col 1 thru Col 18	Column 1 thru Column 18	printer electromagnet-driver outputs to enable hammers

Continued

Table 4-1. The 9805A System Signal Mnemonics (Cont'd)

MNEMONIC	NAME	FUNCTION
CRY	Carry	carry information to the C&T from the A&R
Data A thru Data E	Data A thru Data E	encoded display information from A&R to display circuits
DBL	Disable	see $\overline{A}$
EIS1	Enable Instruction Set 1	signal from I/O processor used to enable instruction from the ROMs to the A&R and C&T
EXT	External Data	keycodes being input from the I/O processor to the C&T. These keycodes originate in the PROM
FBS	Function Block Select	signal generated on mother board which indicates that a Stat block key is down. Used to force the processor FLG' low
FLG'	Flag Prime	this signal is an input to the I/O processor when a keyboard key is pressed which affects all subsequent operations (e.g., PRINT OFF). FBS, the function-block select signal, also generates a FLG' input signal
GIOE	Group I/O Enable	I/O processor decoded output which enables the plotter interface
Ia	Instruction Address	an eight-bit input to the ROMs which contains the ROM-address select information
IOC1-3	I/O Codes, bits 1 thru 3	Coded I/O control information
Is	Instruction	ROM pre-programmed outputs
IsB	Instruction Set Buffered	Is signals which are buffered
Is1	Instruction Set 1	instructions which are input to the processor, C&T, and A&R
Is2	Instruction Set 2	instructions which are input only to the processor

Continued

Table 4-1. The 9805A System Signal Mnemonics (Cont'd)

MNEMONIC	NAME	FUNCTION
KD	Key-down	input line to C&T on which a signal is returned when a key is down
KS	Key-select	output of C&T to the keyboard
MPWO	MOS Power-on	MOS power-on-preset signal; MPWO is 0V at turn-on
PWO	Power-on	bipolar logic signal used to preset the logic when power is switched ON
Φ1	Phase 1	first phase of the 2-phase clock signal (170 KHz)
Φ2	Phase 2	second phase of the 2-phase clock signal
READ	Read	I/O processor decoded output to PROM which enables the PROM keycode outputs
RED	Red Ribbon	red ribbon select signal which enables printer solenoid; generated by the combination of C19 with C20
RESET	Reset	print-drum row 0 indicator, generates the TR signal
RGC	ROM Group Clear	clears any previously selected ROM group enable signals
SBL	Set Busy Light	Busy-light ON signal
SCE	Select-Code Enable	strobe pulse used to enable I/O control data (IOC1-IOC3)
SRA	Select ROM Group A	I/O processor output used to reset the $\overline{A}$ signal
SRB	Select ROM Group B	processor output signal which generates SRB_1 when a keyblock is installed

Continued

Table 4-1. The 9805A System Signal Mnemonics (Cont'd)

MNEMONIC	NAME	FUNCTION
SRC	Select ROM Group C	processor output signal which generates SRC_1 when the data storage assembly is installed
SRB_1	ROM Group B Present	signal which resets $\overline{B}$ when keyblock is installed
SRC_1	ROM Group C Present	signal which resets $\overline{C}$ when data storage assembly is installed
SRT	Start	word-time bit-0 indicator from A&R
SRTB	Start, Buffered	buffered SRT signal
SYNB	SYNC B	buffered word synchronization signal
TP/TL	Printer Timing	print-drum row timing indicator, used to generate the TP signal
TP	Printer timing/ time clocked	printer timing pulse which is phase locked to system used to increment row counter in processor
TR	Timing Reset	print-drum row 0 indicator, used to reset the processor row counter to 0
WS	Word Select	signal from either a ROM or the C&T used to enable the portion of a word on which the A&R is to operate
WSB	Word Select Buffered	buffered WS signal output
YINTF	Interrogate Flag	decoded processor output, used to determine if the plotter interface is ready

SYSTEM POWER-UP

■*Of the five power supplies (+5V, +6V +10V, +15V, and -12V) the +5V supply powers-up first.* Thus, the system clock is operating before the MOS/LSI logic. The +10V supply generates both the +7.5 and +3.75V supplies which are used by the display circuits. The +15V supply is used only by the printer. The +6V and -12V supplies provide power for the MOS circuits.

■Generating PWO (Power-ON)

When the C&T receives power, the two-phase system clock inputs from the Father Board or, if installed, the Display Board cause the circuit to begin sequencing and, subsequently, the first *SYNB signal* is generated. (Note that before the SYNB signal is generated, the C&T may attempt to output an Ia; this address is all zeros due to the address register having been cleared when power was removed.) The SYNB signal clocks *flip-flop U23A*, which generates the signal PWO. *MPWO, the MOS logic-level equivalent of PWO,* is generated by the PWO signal. While PWO is 0 volts, the SYNB signal, together with Φ1 and Φ2, are synchronizing the system.

The PWO and MPWO signals are used to:

- set the bipolar logic to a predetermined state before system operation begins.
- delay any system operations for at least 500 msec to allow time for the print-drum to obtain its normal operating speed.
- preset the ROMs; only ROM 0 of Group A is activated and can output instructions when MPWO is released.
- preset the I/O processor to Enable Instruction-Set One (EIS1), thereby ensuring the instruction outputs of the ROMs are input to the A&R and C&T.
- hold the C&T's Ia (address) outputs at logical 0; the C&T attempts to output incremented addresses each word time, but the Ia line is held at a logical 0 by the MPWO signal.

Before PWO is released, the system is fully synchronized and the print-drum is rotating at its normal operating speed. Thus, when PWO is reset by the first SYNB signal after the 'D' input of *U23A* is high, the system can begin processing data.

The Power-up Routine

Since address zero is present on the Ia line and ROM 0 of Group A is selected, the instruction in address 0 of Group A, ROM 0 is the first instruction executed by the system. Together with the ensuing instructions, it preconditions the system for subsequent, user-initiated operations. The preconditioning, or power-up, routine determines the display format, the information in the display (zeros), and also causes CLEAR to be printed. The final instruction in the routine branches the system to a set of instructions which are used as a 'display-wait loop'.

■While the power-up routine is being executed, the calculator ignores any key which is down. The power-up instructions do, however, interrogate the status of the mode keys (i.e., *AUTO·* and PRINT OFF).

THE DISPLAY-WAIT LOOP

When the power-up instructions have been completed, or any other time the system is idle, the system begins executing a set of ROM instructions, called the display-wait loop, during which the system continually searches for a key-down condition. Until a key-down occurs, information in the A&R circuit is continuously recirculated and displayed while the remainder of the system is idle. When any key, other than AUTO· or PRINT OFF is pressed, a status bit in the C&T is set and the octal equivalent-code for that key is loaded into the C&T's buffer register. Then, the wait loop instructions are exitted and a set of 'key-down preparation routine' instructions is accessed.

The AUTO· and PRINT OFF keys do not affect the wait loop. These keys are tested each time a data entry or printing operation is begun.

GENERATING KEYCODES

■The keyboards are electronically constructed as a 5X7 matrix of switches which, when a key is pressed, connect on the seven key-select lines (KS) to one of the five key-down lines (KD) (see Figure 4-1).

> **NOTE**
>
> *The Model 5 does not use key-select line KS-0.*

The seven KS lines are sequentially driven by a 3-bit to 8-bit decoder in the C&T; the decoder inputs are the tl least-significant bits of the C&T's 56-bit counter. Thus, each KS line is driven once each eight bits of the system 56 word (i.e., 7 times each word). When a key is down, the pulses on the KS line corresponding to that key are couple the associated KD line and input to a data selector in the C&T.

The data selector uses the three most significant bits of the 56-bit counter to sequentially select each KD line; each lir selected once each word time. When the KD line being selected is pulsed by the decoder, via the associated KS line, data selector transfers the input signal to its output. The output signal is then used to load the keycode-buffer regi with the six outputs of the 56-bit counter; 21 states of the counter are not used. The output of the data selector is used to set status-bit 0, the keydown status bit, in the C&T.

The keycode-buffer register is loaded with the same octal keycode once each word-time until the key is released. keycode in the buffer register is, however, not loaded into the address register until the C&T receives a ROM instruc to do so; the instruction for that operation is contained in the 'key-down preparation routine' instructions.

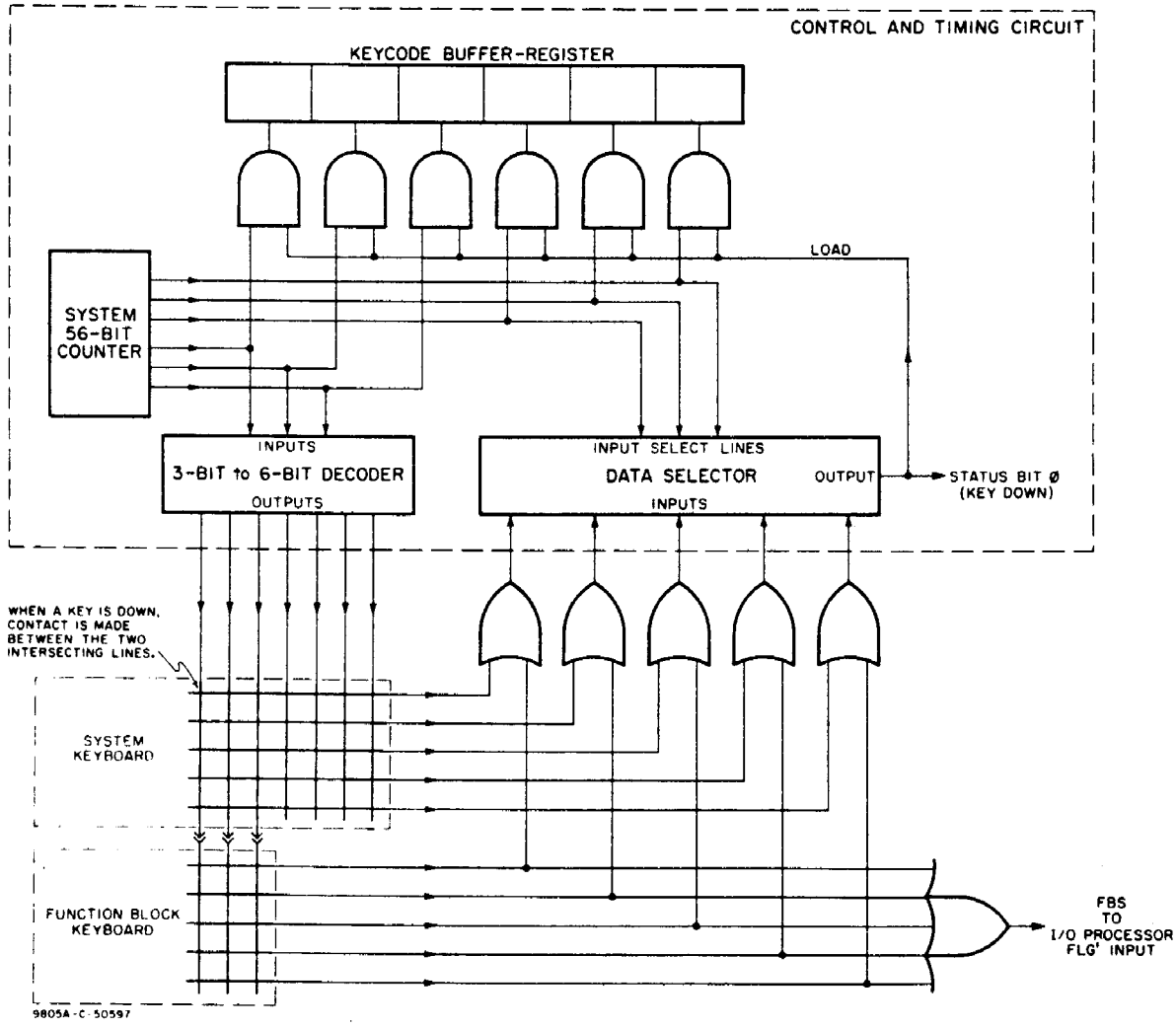


Figure 4-1. The Keyboard Scanner

KEY-DOWN PREPARATION ROUTINE

When a keyboard key, other than one of the mode keys, is pressed, a keycode corresponding to that key is generated (see 'Generating Keycodes') and status-bit 0 is set; if status-bit 0 is already set, the key is ignored. The ROM instructions in the display-wait loop continually test status-bit 0 to determine if a key has been pressed. When status-bit 0 is set, the system exits the wait loop and enters the key-down preparation routine. The system ignores subsequent key-down conditions until the original key which was down is released. The primary functions of this routine are:

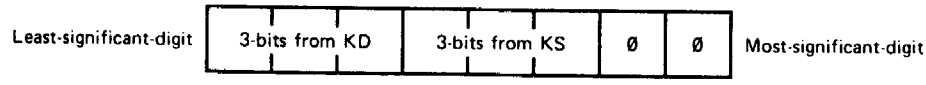
- to provide a software-controlled delay to ensure the key entry was not due to keybounce.
- to blank the display.
- to prepare the A&R, C&T, and the I/O processor to perform any instruction required to service the key which is down.
- to test a status-bit which is set by the SHIFT key. If that bit is set, an instruction is issued to activate a particular ROM. If the bit is reset, another instruction activates a different ROM. The ROM activated by this process contains the first instruction for servicing the keycode in the keycode-buffer register (ROM selection is described later in this chapter).

■Upon completion of the preparation routine, *which may require up to 20 word times*, the calculator system is ready to service the keycode in the user-defined display modes of operation.

SERVICING THE KEYBOARD INPUTS

■The final instruction in the preparation routine loads the keycode from the C&T's buffer register into the address register. Two bits are added to the six-bit keycode by hardware in the C&T to make the eight-bit instruction address (Ia). Both bits are zeros, and are placed in the two most-significant-bit positions. *(External keycode entries may not have zeros in the two MSB positions. Those keycodes are described later in this chapter.)*

The eight-bit address, in the address register, is in the form:



Beginning at bit-time 56 of the last word in the preparation routine (*i.e., approximately 18 words after the key was pressed*), the address is clocked, bit-serially, to the ROMs on the Ia bus. The address is received by the ROMs during bit-times 19 through 26 of the ensuing word (i.e., the first word after the completion of the preparation routine). This address is stored in the address register of each ROM in the system. Each ROM decodes the address and, at bit-time 44, the instruction specified by the address is loaded, in parallel, into each ROM's instruction register. Only the active ROM (the ROM which was selected during the preparation routine) can, at this time, output the 10-bit instruction from the instruction register.

A SUMMARY OF THE PRECEDING INFORMATION

Before continuing, let's briefly summarize the operations which have previously taken place.

- Initially, the calculator was OFF. When the unit was switched ON, the system began synchronizing and PWO was generated to preset the system and to delay subsequent operations until the printer was ready.
- Next, a routine was entered that set up the correct display and printed CLEAR.
- The calculator then entered a wait loop. During this time, the display was on and a continual test for a key-down condition was taking place.
- When a key was pressed, the calculator exitted the wait loop and began a keydown preparation routine during which the system was prepared to accept the 6-bit keycode stored in the C&T. The last instruction in the routine activated the correct ROM and loaded the keycode into the C&T's address register; while loading the keycode into the address register, two zeros were added to complete the 8-bit address.
- Finally, after completion of the preparation routine, the keycode was loaded into each ROM's address register and, at bit-time 44, the instruction in the specified address was loaded into each ROM's ten-bit instruction register.

Until this time, the operations performed by the calculator have been reasonably well defined. From this time on, however, the instructions define the operations performed by the calculator; each instruction differs from each other instruction, depending upon the requirements of the problem being solved.

THE ROM INSTRUCTIONS

A Word About the First Keycode-Instruction

Let's discuss the instruction, just loaded into the instruction register, for a moment.

■*Since only 5 key-down and 7 key-select lines are used, only 35 (5X7) instructions can be accessed by keycodes from keyboard.* All of those instructions are clustered within a single ROM (one ROM is active for shifted keys, another F is active for unshifted keys). All keycodes, however, require more than a single instruction to perform the requ operations. Therefore, each keycode eventually addresses a ROM-select or branch instruction which actually access routines to service that key. Some of those routines may contain additional branch or jump-subroutine instruction continue servicing the key.

The Instruction

Each ROM contains 256 (2^8) instructions (Is), each of which is accessed by a different instruction address (Ia). One only one instruction is output, bit-serially, during bit-times 45 through 54 of each word. Those instructions:

- are decoded by the issuing (active) ROM and, if the operation is arithmetic, 3-bits of Is determine which of six possible WS signals is output to the A&R during the ensuing word-time. (Two types of WS signals originat the C&T during arithmetic operations.)
- are decoded by the inactive ROMs to provide an arrangement whereby control can be switched from one RON another; only one ROM in the system is active (i.e., outputting instructions) at one time. The address of ROM-select instruction is incremented in the C&T, then used as the selected ROM's instruction address (Ia).
- are decoded by the C&T, thereby providing control of the C&T operations and also providing branch subroutine instruction addresses for the system. (The return address of subroutine operations is the increme address of the subroutine instruction, and is stored in the C&T until it is required for the return.)

  Other instructions are decoded by the C&T for the two types of C&T word-select outputs. This occurs during certain arithmetic operations performed by the A&R circuit. The C&T word-select signals either speci single digit operation, or an operation on all digits less than a specified digit number; WS from the C&T can n specify operations on the center portion of a word.
- control the A&R. Data is placed in the A&R registers either by arithmetic operations or by exchanging between registers. BCD data can be input or output in the A&R by additional instructions.

  The BCD data in each of the seven A&R registers can be exchanged or transferred using other instructions. arithmetic operations in the calculator are accomplished in the A&R by arithmetic instructions. These instructi and only these instructions, require a WS input signal during the ensuing word-time.
- toggle the display information to the display circuits by another instruction. Yet another instruction must be to disable the information to the display.
- control the I/O processor circuit, which in turn controls the printer and *the external ROM groups (e.g., the plo interface).*

■THE PROCESSOR CIRCUIT

When a printout is necessary, instructions are used to load the row (or sector) hexadecimal number of the des character into digit positions in two 56-bit registers; each digit position corresponds to one column on the print-dr (one of the two 56-bit registers is located in the A&R circuit.) When the ROM-generated hexadecimal number in e digit-position corresponds to the hexadecimal print-drum row number, the hammer in the corresponding colum activated.

The I/O processor always 'listens' to the instructions on the Is bus. Some instructions, however, are ignored by processor while others instruct the processor to disable instructions to the A&R and C&T circuits (EIS1).

The I/O processor provides control of the optional Model 5 ROM circuits – the plotter interface, data storage circ statistics keyblock, and the statistics PROM. When instructions require the use of one of those assemblies, the proce outputs signals, which, when decoded by an external decoder, select the appropriate ROM group (SRA, SRB, or SRC) disabling instructions to the other two groups. Also, instructions are available to interrogate the plotter FLAG sig (YINTF), enable the interface (GIOE), or read information from the PROM (READ). Data is transferred from th circuits to the A&R on the BCD line or the C&T on the EXT line.

Finally, the status of the keyboard mode keys, the *AUTO·* and PRINTER OFF, is tested and the results recorded in the A&R and C&T by the processor. The processor receives an instruction to test one of those keys, then outputs an enable signal which, if the key is down, forces the FLG' line to a logical 1. The logical 1 FLG' signal then causes the processor to set status-bit 11 in the C&T (via the FLG line), thereby causing a ROM instruction to be issued that performs the appropriate operation.

■*The approach described above is also used for keyblock keys. In this case, however, instructions to the C&T and A&R circuits from the keyblock ROMs are enabled and the main system ROM instructions are disabled.*

THE DISPLAY CIRCUITS

The System Clock

One of the functions of the anode driver circuit is to provide the two-phase clock pulses shown in Figure 4-2. With the exception of two externally-connected timing components, the anode driver contains all of the circuits necessary to perform this function. Systems which do not contain the display option utilize discrete components for the clock circuit; these components are located on the Father Board (A4). The two-phase clock frequency is 170KHz.

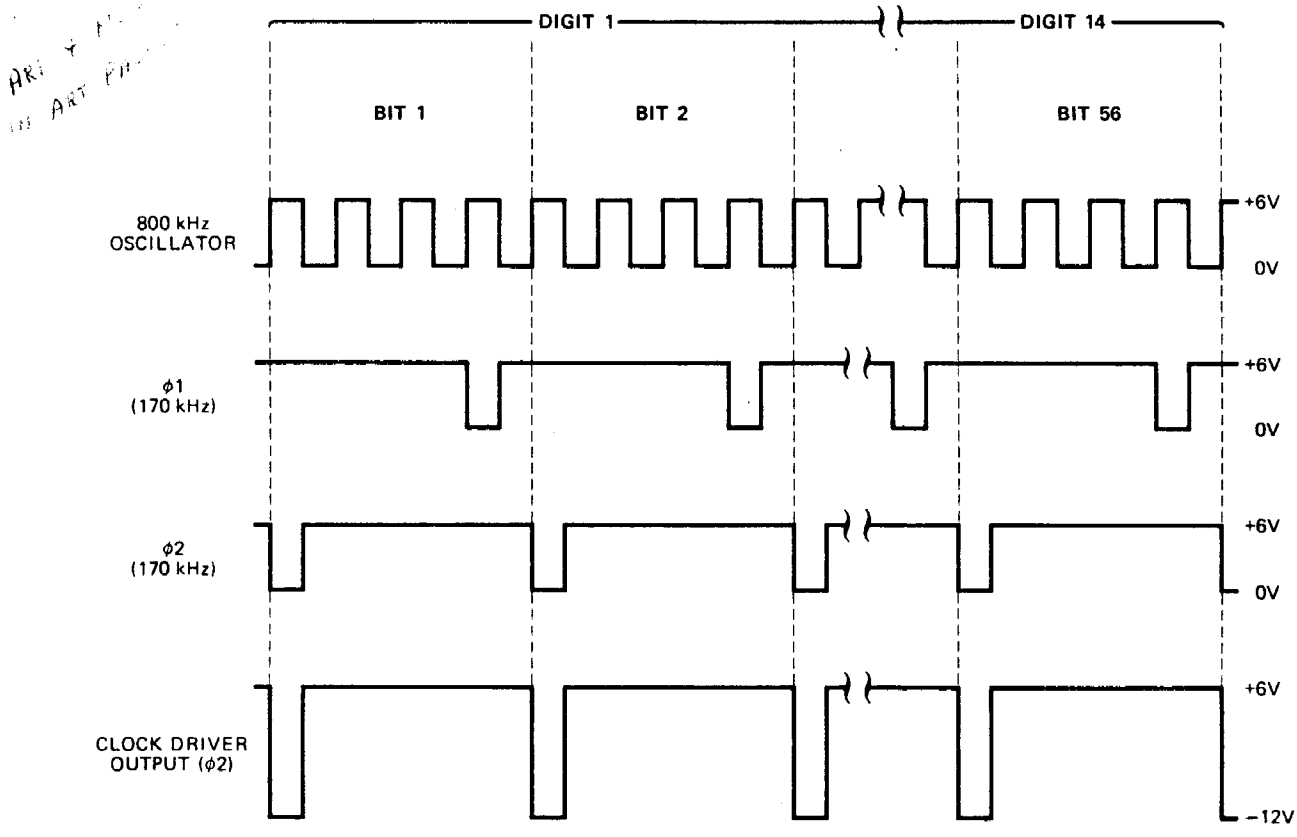


Figure 4-2. System Two-phase Clock Signals

The Anode and Cathode Drivers

The multiplexed Data A through Data E information, which is output by the A&R, is input to the anode driver. anode driver demultiplexes the information and drives the anode of the appropriate display LEDs; each LED is segment of a digit (see Figure 4-3). The anode driver provides drive for the same segments in each of the 15 positions. The cathode driver, however, selects a single digit position for displaying the information.

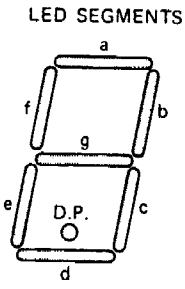
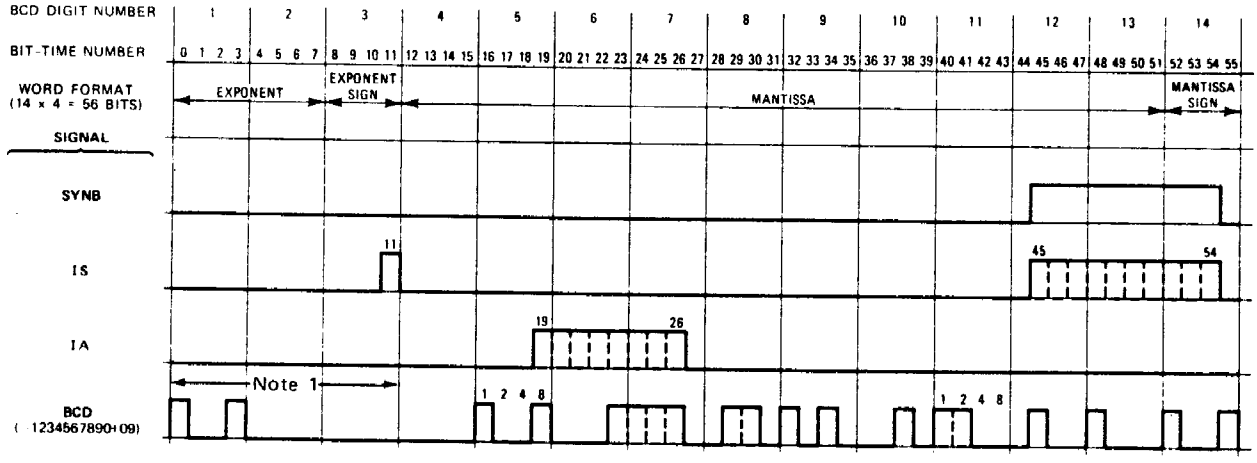


Figure 4-3. The Segments of Each Display Digit

When the anode driver has completed the display of a digit (i.e., after four system bit-times), it outputs a shift-clock p to the cathode driver. The cathode driver then enables the next digit (to the right) for displaying the A&R's ensuing I A through Data E outputs. Two consecutive shift-clock signals are output during any digit which is followed by a dec point; the decimal-point data is output by the A&R at the same time as the preceding digit-data. Digits which are b are treated the same as other display digits except that when the anode driver decodes the A&R circuit outputs, no l anodes are driven.

The START signal from the A&R circuit resets the cathode driver's digit counter, thereby setting the cathode drive digit-position one.

The 'Busy Light' is switched on or off by the I/O processor circuit using instructions from one of the ROMs.



Note 1: When a negative exponent occurs, the system handles the exponent in the Ten's-complement notation (see Figure 2-1 in Chapter 2).

Figure 4-4. Looking at the BCD Information

■THE A&R'S BCD DATA

The only method of 'looking' at information in the system is to use an oscilloscope, synchronized to either START (bit 0) or the trailing edge of SYNB (i.e., bit 54), to monitor the BCD line of the A&R. Since the BCD data in the A&R is recirculated once each word-time when the calculator is not busy, that data can be seen on the BCD output. Figure 4-4 shows an example of data on the BCD line when the display is:

BCD data-transfers with the A&R are controlled by the BDE signal which, in turn, controls a bi-directional amplifier on the Father Board.

Note that negative exponents are handled by the A&R in the ten's-complement notation.

■THE MODEL 5 OPTIONS

When a Model 5 Statistics Keyblock key is pressed, control of the system is transferred to the keyblock ROMs by a 'Select ROM Group B' (SRB) signal from the I/O processor. The keyblock ROM instructions are then serviced by the mainframe data-processing circuits – the C&T, A&R, and I/O processor – in the same way as mainframe ROM instructions are serviced.

When a keyblock key is pressed which requires that either the plotter interface or the data storage circuits be used, control of the system is transferred to the appropriate circuit's ROMs by a Select ROM Group C (SRC) or, for plotter control, a GIOE signal from the I/O processor. These ROMs also use the mainframe data-processing circuits to service the required instructions. Control of the data being input or output by the optional circuits is accomplished by the I/O processor, which is under control of the associated circuit's ROMs.

The processor outputs the signals GIOE and YINTF to enable the plotter interface if the plotter is not busy. The data storage circuits use the BCD line to receive the address of the data being input or output. Then, during a subsequent word time, these circuits input or output the BCD data on the BCD line (see 'The A&R's BCD Data').

The Statistics PROM circuit contains eight-bit keycodes which are input, bit-parallel to the processor on data lines C1 through C8. The processor outputs the keycodes, bit serial, on the EXT line where they are input to, and then processed by, the C&T. The C&T is being controlled by instructions from the keyblock ROMs. Unlike the keyboard keycodes, the PROM keycodes must be 8-bit codes; so the two zeros in the most significant bit positions are not added by the C&T circuit.

–NOTES–

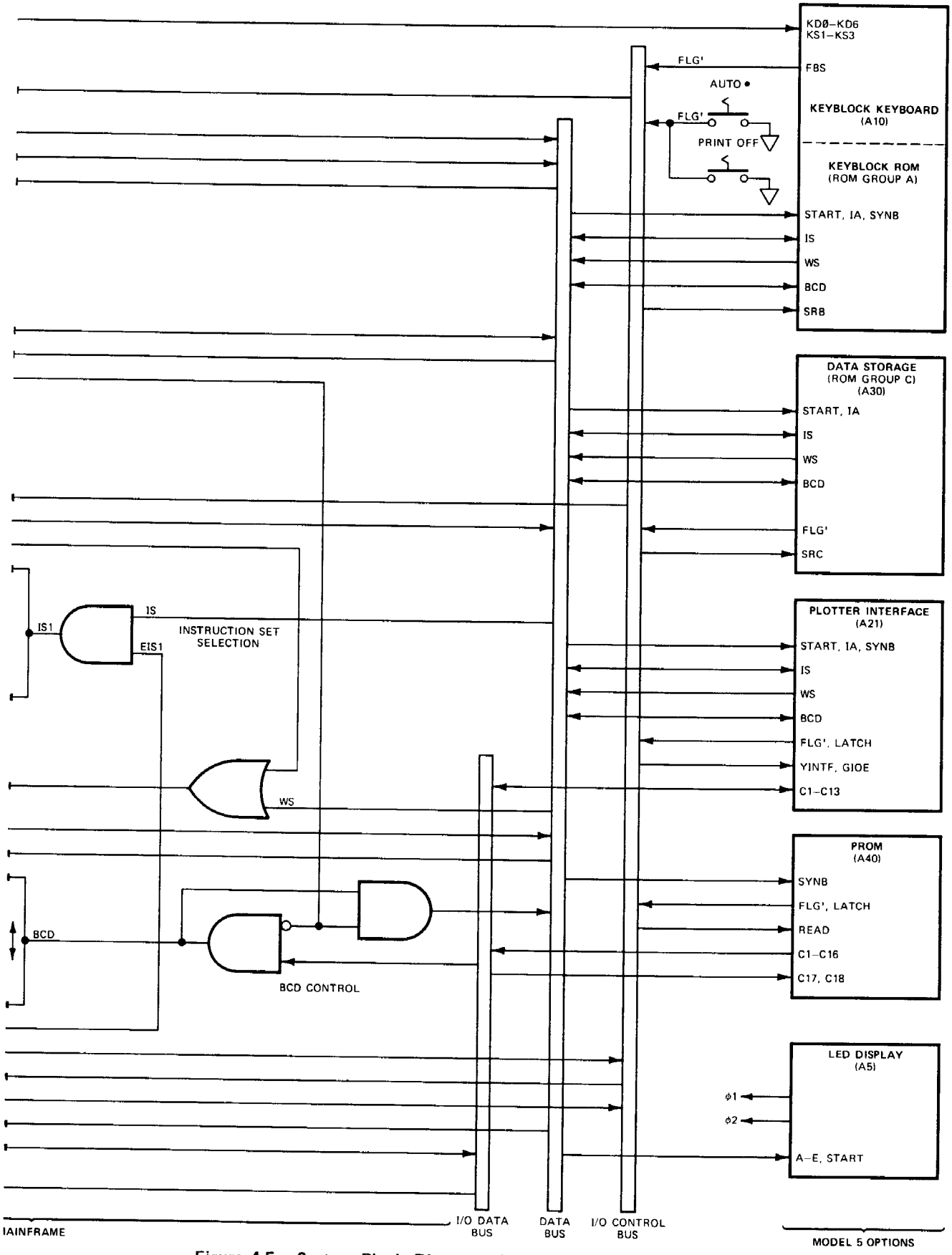


Figure 4-5. System Block Diagram with Signal Interconnections

Table 5-1. Test Equipment Recommended for ROM Tests

INSTRUMENT TYPE	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
Oscilloscope	Measure pulse @ 1 μsec MAX amplitude -12V	180C/1801A 1820C
ROM Tester	N/A	ET 7083
9821A Calculator	423 data storage-registers	9821A, Opt.001
Service Cassette	N/A	00081-90032
Multi-Function Meter	Volts, current & ohm	3469B
Scope Probes	10:1 ≥10 Meg and ≤10 pf input (2 ea.)	10004B
RECOMMENDED SERVICE TOOLS		
8710-0899	Small Pozidrive Phillips Screwdriver	
8710-0004	Small Longnose Pliers	
8710-0012	Small Diagonal Cutters	
8730-0009	Slot Drive Screwdriver	
8690-0015	Soldering Aid	
8700-0003	Exacto Knife	
8700-0006	Replacement Blades, 5 Blades/Package	
8710-0007	Fine Point Tweezer	
8690-0089	Soldering & Desoldering Kit	
Replacement parts for soldering and desoldering kit	8690-0091 Heat Cartridge 30 watt 8690-0092 Tini-Tip 1/16" 8690-0093 Tini-Tip 1/8" 8690-0095 Antiseize 1/4 oz. Tube	
CHEMICAL		
8500-0232	T.F. Freon	
8500-0210	Quick-Freeze	
6010-0144	Bottle of Flux Remover	
6040-0297	Silicone Grease	

Table 5-2. The ROM-Test Software

FILE NO.	FILE SIZE	CONTENTS
0	250	Executive (user instructions)
1	75	Special Program 'RT'
2	150	ROM-Test Supervisor
3	75	Pass/fail Control Program
4	75	Checksum Lister Control Program
5	75	Model 46 data (R43)
6	75	Model 46 data (for 1818-0087 ROMs)[R43]
7	150	Model 81 data (R138)
8	50	Model 5 Motherboard ROM-data (R31)
9	50	Model 5 Keyblock ROM-data (R31)
10	50	Model 5 Interface ROM-data (R31)
11	25	Model 5 Data Storage ROM-data (R10)
12	25	12-digit lister program
13	50	Tape lister-program
14	50	spare
15	50	spare
16	100	spare
17	100	spare

CHAPTER 5
TROUBLESHOOTING ROMS

INTRODUCTION

The information in this chapter will assist you in repairing Model 5, Model 46, or Model 81 Calculators which contain defective ROMs. The test procedures provided in this chapter must be successfully completed before the repair procedures in Chapter 6 are begun.

Recommended Test Equipment

Table 5-1 lists the equipment necessary to test the ROMs in each of the calculators. If the recommended test equipment is not available, any instrument which has specifications equal to, or better than, the recommended equipment may be used.

THE ROM-TEST SYSTEM

Complete operating and service information for the ROM-Test System is provided in the 'ET 7083 ROM Tester Operating and Service Manual' (09805-90010).

The ROM-Test System consists of an ET 7083 ROM Tester, a 9821A (Opt 001), and the programs and data from the service cassette (see Table 5-2). This system provides a means of testing each ROM in the preprogrammed calculators without removing the ROM from the circuit board.

ROM-Test Software

The software (i.e., the data from the service cassette) is used by the 9821A Calculator to control the ROM tests (see Table 5-2). The three files used during each test contain the following information:

- The ROM Test Binary Program performs each test by providing the correct signals to the ET 7083 ROM Tester and interpretting and storing the test results.
- Either the pass/fail or list checksums program may be used. These programs 'call' the binary program and output the test results for the technician's use. The pass/fail program prints only "FAILED IS AND WS" or whichever checksum was incorrect, together with the associated ROM number of those ROMs which fail their test. If all ROMs pass their test, PASS is displayed. The checksum lister program lists the Is and WS checksums, together with the associated ROM number, of all ROMs on the circuit board being tested.
- The third file used during each test contains data which is stored in the 9821A data registers. This data selects the ROM to be tested on the circuit board, so different data must be used to test the various ROM boards.

System Operation

When the software is properly loaded, the correct system connections have been made, and RUN PROGRAM is then pressed, the pass/fail or checksum lister program calls the binary program (special program "RT"). This transfers control of the tests to the binary program. The binary program tests the ROMs and records the results of the tests in 9821A data registers. The control program then outputs the results for the operator.

The ET 7083 ROM Tester

The ROM Tester interfaces the 9821A to the ROMs being tested and also provides the timing signals required for the ROMs to operate correctly. When Model 5 ROMs are being tested, dc power is provided for the ROMs; dc power for Models 46 and 81 ROMs must be provided either by the device-under-test (DUT) power supplies or from an external source; the ET 7074 power supply box can be used for this purpose.

ROM TEST PROCEDURE

Before switching the ET 7083 ON or applying power to the ROMs, verify that the ROM-Test System is correctly installed and the appropriate software is loaded into the 9821A. If any doubt exists about the installation procedures, consult the ET 7083 ROM Tester Operating and Service Manual.

CAUTION

DAMAGE MAY RESULT IF THE MODEL 46 OR MODEL 81 16-PIN ROM-CLIP IS IMPROPERLY CONNECTED. BEFORE APPLYING POWER TO THE ROMS ALWAYS VERIFY THAT THE PINS ON THE CLIP ARE ALIGNED WITH THOSE ON THE ROM. THEN VERIFY THAT THE PINS ON THE CLIP ARE NOT SHORTED TO THE METALLIC COVERPLATE ON TOP OF THE ROM.

CHAPTER 5
TROUBLESHOOTING ROMS

> **NOTE**
>
> The Models 46 and 81 Calculators have three jumper wires on the mother board which must be removed before the ROM tests are begun. These jumpers are located under the keyboard and are marked 'WS', 'IA', and 'SYNC'.

When both the DUT and the test system have been properly prepared to perform the ROM tests, the ROM tests ca performed by pressing: END, EXECUTE ... RUN PROGRAM. Depending on the control program (i.e., pass/fai checksum lister) being used, the results of the tests are presented either by the 9821A printing the ROM number FAILED IS and/or WS of those ROMs which fail or by the 9821A printing the ROM number and the associ checksums of all ROMs tested. In most situations, the former presentation, obtained by using the pass/fail progran preferable. If, however, you are using the checksum lister program, then the test results for each ROM must com exactly with the printouts shown in Table 5-4.

Interpreting the Test Results

If all ROM tests result in failure indications, verify that the test system is installed correctly and the correct softwa being used. If a Model 46 or a Model 81 is being tested, verify that the jumpers on the mother board are removed. If test system is properly installed, ensure that the power supply, clock (both Φ1 and Φ2), and sync inputs to the ROMs within the limits specified in the ROM tester manual. If all of the above checks are satisfactory, verify proper sys operation by performing the ROM tests on ROMs which are known to be operating correctly. (Any circuit board contains ROMs and operates correctly may be used for this purpose.) If the system appears to be operating correctly, or more of the ROMs originally being tested are defective. All ROM tests, except the test on ROM 0, require that at one other ROM be operating correctly before the tests can be successfully run. Thus, if a ROM, which is used to s the ROM to be tested, is defective, neither ROM can be tested satisfactorily. ROM 0, for example, is used during testing of all other ROMs and, if defective, may cause all ROM tests to result in a failure indication. Table 5-3 shows ROMs which must be operating correctly before the indicated ROM can be tested. Correlating the information in table with the test results should indicate which ROM (or ROMs) is defective.

ROMs in which the inputs or outputs have become shorted to ground or to one of the power supplies will prevent ROM tests from being properly performed; only 0's or 1's will be output by the ET 7083 as the checksums. Those t of failures must be found by removing ROMs until the shorted ROM is isolated. Then, replace the defective ROM rerun the ROM tests.

> **CAUTION**
>
> ALL MOS CIRCUITS ON THE CIRCUIT BOARD MAY BE DAMAGED IF THE +6V POWER SUPPLY IS SHORTED TO GROUND – EITHER ON THE CIRCUIT BOARD OR INSIDE AN INTEGRATED CIRCUIT. IF THIS TYPE OF FAILURE OCCURS, DO NOT APPLY AC POWER UNTIL THE SHORT HAS BEEN REMOVED.

The ROMs must be satisfactorily tested before the board tests in Chapter 6 are performed.

Table 5-5 shows the functions assigned to each of the ROMs in the preprogrammed calculators.

> **IMPORTANT NOTE**
>
> When replacing ROMs, always verify that the new ROM and defective ROM are marked with the same part numbers.

Before returning the calculator to the customer, perform the appropriate calculator test sequence in Chapter 6.

Table 5-3. ROM Test Sequence

ROM P/N	ROM Being Tested	ROM-Select Sequence	
Model 46 ROM Tests			
1818-0058	A0	PWO	(ROM 0)
	A1	0 to 1	(ROM 1)
	A2	0 to 1 to 2	(ROM 2)
	A3	0 to 3	(ROM 3)
1818-0087*	B0	0 to 3 to 5	(ROM 5)
	B1	0 to 3 to 6	(ROM 6)
	B2	0 to 4 to 7	(ROM 7)
	B3	0 to 4 to 8	(ROM 8)
1818-0060	B4	0 to 4	(ROM 4)
Model 81 ROM Tests			
1818-0068	A0	PWO	(ROM 0)
	A1	0 to 1	(ROM 1)
	A2	0 to 1 to 2	(ROM 2)
	A3	0 to 1 to 3	(ROM 3)
1818-0069	A4	0 to 1 to 4	(ROM 4)
	A5	0 to 1 to 5	(ROM 5)
	A6	0 to 1 to 2 to 6	(ROM 6)
	A7	0 to 7	(ROM 7)
1818-0067	B0	0 to 8	(ROM 8)
	B1	0 to 9	(ROM 9)
	B2	0 to 1 to 10	(ROM 10)
	B3	0 to 1 to 11	(ROM 11)
1818-0070	B4	0 to 1 to 12	(ROM 12)
	B5	0 to 8 to 13	(ROM 13)
	B6	0 to 8 to 15 to 14	(ROM 14)
	B7	0 to 8 to 15	(ROM 15)
1818-0071	C0	0 to 16	(ROM 16)
	C1	0 to 17	(ROM 17)
	C2	0 to 16 to 18	(ROM 18)
	C3	0 to 16 to 19	(ROM 19)
1818-0072	C4	0 to 4 to 20	(ROM 20)
	C5	0 to 16 to 23 to 21	(ROM 21)
	C6	0 to 18 to 15 to 22	(ROM 22)
	C7	0 to 16 to 23	(ROM 23)
9805A Mother Board ROMs			
1818-0041	0	MPWO	
1818-0042	1	0 to 1	
1818-0043	2	0 to 2	
1818-0044	3	0 to 3	
1818-0045	4	0 to 4	
1818-0046	5	0 to 3 to 5	
1818-0047	6	0 to 6	
1818-0048	7	0 to 7	

*ROM P/N 1818-0087 supersedes ROM P/N 1818-0059.

Continued

Table 5-3. ROM-Select Sequence (Cont'd)

ROM P/N	ROM Being Tested	ROM-Select Sequence
Stat Keyblock Assembly ROMs		
1818-0049	0	MPWO
	1	0 to 1
	2	0 to 2
	3	0 to 3
1818-0050	4	0 to 4
	5	0 to 5
	6	0 to 6
	7	0 to 7
Plotter Inferface ROMs		
1818-0052	0	MPWO
	1	0 to 3 to 1
	2	0 to 3 to 2
	3	0 to 3
1818-0053	4	0 to 4
	5	0 to 5
	6	0 to 3 to 6
	7	0 to 7
Data Storage ROMs		
1818-0038	0	MPWO
1818-0039	1	0 to 1
1818-0040	2	0 to 2

Table 5-4. Correct ROM Checksums for ROM Tests

9805A MOTHERBOARD ROM CHECKSUMS				MODEL 46 ROM CHECKSUMS		
0	ROM No.	4		0	4	
143332	IS Checksum	152076		163266	145022	14307
20123	WS Checksum	57775		60045	100017	7777
1		5		1		
127005		14063		6107		15525
20024		177651		17746		10005
			QUAD-ROM		QUAD-ROM	
2		6		2		
143704		124355		5740		17524
60021		157755		177651		16000
3		7		3		
155760		173730		160164		14232
140021		60043		60051		60041

Table 5-4. Correct ROM Checksums for ROM Tests (Cont'd)

MODEL 81 ROM CHECKSUMS

	ROM GROUP A	ROM GROUP B	ROM GROUP C
QUAD-ROM	0 (ROM No.) 137256 (IS Checksum) 160047 (WS Checksum)	8 141420 17764	16 22353 120044
	1 1277 114	9 177351 120015	17 27576 20015
	2 6634 120107	10 60631 20033	18 111073 140025
	3 174465 117624	11 71307 77740	19 21707 1
QUAD-ROM	4 176177 157743	12 171661 77776	20 53774 117776
	5 27661 20047	13 120350 177716	21 137445 140023
	6 134744 57512	14 24232 60006	22 12033 37740
	7 166325 40061	15 36527 40022	23 35711 57757

Continued

Table 5-4. Correct ROM Checksums for ROM Tests (Cont'd)

9805A ROM GROUP B		9805A ROM GROUP C	
STATISTICS KEYBLOCK ROM CHECKSUMS		PLOTTER INTERFACE ROM CHECKSUMS	DATA STORAGE ROM CHECKSUMS
	0 ROM No.	0	0
	152646 IS Checksum	171412	61751
	160001 WS Checksum	100022	67
	1	1	1
QUAD-ROM	172154	143274	127234
	37774	17771	140010
	2	2	2
	10505	152663	104436
	160012	100056	157765
	3	3	
	141152	105415	
	40005	77757	
	4	4	
	22417	132244	
	100017	57705	
	5	5	
QUAD-ROM	2633	130704	
	140004	77755	
	6	6	
	16643	166746	
	20033	17677	
	7	7	
	170426	151274	
	17775	137772	

Table 5-5. ROM Assignments

ROM	ASSIGNMENT
Model 46	
A0	1. Addition and subtraction routines 2. Mode conversion for trig. functions 3. Power ON routines
A1	1. Trigonmetric routines
A2	1. Logarithms, exponentials, multplication, and division routines
A3	1. Factorial routine 2. Print routine 3. To POLAR routine 4. Constant storage
B0	1. Display wait loop 2. Start of shifted functions routines
B1	1. PRINT key routine 2. LIST key routine 3. Data adjustment routine for display or printing
B2	1. Start of routines for unshifted keys
B3	1. Preparation for print (cont'd from B1) 2. Overflow check 3. Data fetch from storage registers
B4	1. $\Sigma\pm$ key routine 2. Standard deviation routine 3. Data entry routine 4. To POLAR routine
Model 81	
A0	1. Power On 2. Paper advance 3. Digit entry
A1	1. Supervisor, accepting keycodes 2. Display routine 3. Total, subtotal, CLEAR X<>Y, R↓, SAVE, CHANGE SIGN routines 4. Routine start for + x ÷ –
A2	1. Accepting keycodes in shift mode 2. Multiply, divide by constant 3. %, Δ% routines 4. Part of the add, subtract routine
A3	1. + – x ÷ routines 2. X→Y, Ln, X routines 3. Normalization routine
A4	1. Σ+, Σ- routines 2. Mean and standard deviation routines 3. Load data storage address 0, 1, 2, 3

Continued

Table 5-5. ROM Assignments (Cont'd)

ROM	ASSIGNMENT
Model 81 (Cont'd)	
A5	1. Cash flow 2. Accumulated interest for mortgage (Σ+ and extended 6 function) 3. RND ( ) key routine
A6	1. Day, date routine
A7	1. 'Print' routine 2. Data adjustment routine for display and print 3. Overflow, underflow check 4. ROM group A RETURN supervisor
B0	1. Supervisor for N, I, PMT, PV, FV key routine start 2. DAY, TL data storage supervisor and routine start
B1	1. Supervisor for N, I, PMT, PV, FV STORE, RECALL, problem setting and printout 2. % of total routine (extended function 9)
B2	1. Accrued interest routine 2. Discounted note routine 3. Bond price and yield to maturity routine start
B3	1. N, PMT, PV, FV computation 2. I computation given N, PV, FV 3. Problem set up for other I computations including APR 4. Routine start for BOND price
B4	1. Set mode 2. Print mode
B5	1. 2 dimension trend line routine 2. RND ( ) routine start 3. ADJUST routine (used in EXT 2, 3, 4, 6)
B6	1. Output for N, I, PMT, PV, FV, DAY, DATE 2. Output for mean and standard deviation 3. Sum of years digit depreciation start 4. Diminishing balance routine printout routine
B7	1. ROM group B RETURN supervisor 2. TL output 3. Yield to maturity routine start 4. Subroutines that include data storage, address loading, print messages, etc.
C0	1. STORE and RECALL from data storage routine 2. Print data storage content routine 3. Part of data adjustment routine 4. Effective rate of interest per period (extended function 0)
C1	1. Discounted rate of return (extended function 1) 2. % of total routine end

Table 5-5. ROM Assignments (Cont'd)

ROM	ASSIGNMENT
C2	1. Yield to maturity computation
C3	1. I computation given N, PMT, PV (FV), N, I 2. APR computation
C4	1. Extended function supervisor 2. Coupon equivalent yield (extended function 8) 3. Bond price computation start
C5	1. Diminishing balance depreciation routine start (EXT 3) 2. Rule of 78 prepayment routine (EXT 5) 3. APR output 4. Coupon equivalent yield output 5. Yield to maturity and bond price output
C6	1. DAY, DATE, day of week routine end 2. Discounted rate of return output 3. Yield to maturity routine end
C7	1. Sum of years digits, declining balance and diminishing balance depreciation routine body 2. ROM group C RETURN supervisor 3. Various subroutine access points
Model 5 Mother Board	
0	1. Power ON 2. Acceptance of unshifted keycodes (and all PROM keycodes)
1	1. Digit entry 2. RND ( ) key routine 3. Basic 'print' routine
2	1. Display generation 2. RECALL and STORE routines 3. Overflow routine 4. Basic wait for 'key down' loop
3	1. Parenthesis routines 2. Check for illegal operations (resulting in NOTEs)
4	1. If, set, and clear flags tests 2. Addition/Subtraction routines
5	1. Logarithm and exponential routines 2. Multiplication and division routines
6	1. Acceptance of shifted keycodes 2. Label search 3. 'Jump to absolute' routine 4. 'Go to' subroutine
7	1. 'Print' preparation routines

Table 6-1. Recommended Test Equipment

INSTRUMENT TYPE	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
Board Tester	N/A	ET 7074
9821A Calculator	423 Data Storage Registers	-hp-9821A Opt. 001
Test Cassette	N/A	00081-90032
Oscilloscope	Measure pulse @ 1 μsec MAX amplitude −12V	180C/1801A 1820C
Multi-Function Meter	Volts, current & ohm	3469B
Scope Probes	10:1≥10 Meg and ≤10 pf input (2 ea.)	10004B
Logic Probe	TTL logic probe	-hp- 10525A

RECOMMENDED SERVICE TOOLS

8710-0899	Small Pozidrive Phillips Screwdriver
8710-0004	Small Longnose Pliers
8710-0012	Small Diagonal Cutters
8730-0009	Slot Drive Screwdriver
8690-0015	Soldering Aid
8700-0003	Exacto Knife
8700-0006	Replacement Blades, 5 Blades/Package
8710-0007	Fine Point Tweezer
8690-0089	Soldering & Desoldering Kit
Replacement parts for soldering and desoldering kit	8690-0091 Heat Cartridge 30 watt 8690-0092 Tini-Tip 1/16" 8690-0093 Tini-Tip 1/8" 8690-0095 Antiseize 1/4 oz. Tube

CHEMICAL

8500-0232	T.F. Freon
8500-0210	Quick-Freeze
6010-0144	Bottle of Flux Remover
6040-0297	Silicone Grease

CHAPTER 6
TROUBLESHOOTING CIRCUIT BOARDS

INTRODUCTION

The information contained in this chapter will assist you in repairing the preprogrammed calculator circuit boards. All ROMs on the board being tested must have been satisfactorily tested (see Chapter 5).

Before testing any board and after making any required repairs, perform the appropriate key test procedure.

Chapter Organization

This chapter is organized into two sections: The first section contains information describing the repair of circuit boards using an ET 7074 Board Tester. The second section provides information for repairing the various circuit boards where an ET 7074 Board Tester is not available. Additional information is provided at the end of the chapter which describes general troubleshooting hints.

Recommended Test Equipment

Table 6-1 lists the test equipment required to troubleshoot the circuit boards. If the recommended test equipment is not available, any instrument which meets or exceeds the required specifications may be used.

REPLACING DEFECTIVE PARTS

Damaged Circuit Boards

When one of the MOS/LSI circuits is being replaced, particular care must be taken to avoid damaging the circuit board. If a circuit board is inadvertently damaged by excessive heat, or should a trace or solder pad peel off the circuit board, appropriate repairs (or circuit board replacement) must be accomplished before the unit is returned to the customer.

Replacing Display Units

There are six *different* luminous-intensity categories of LED units; the LEDs on each display board are matched at the factory. Therefore, when replacing a LED unit, always ensure that the alpha code on the back of the replacement unit matches the code on the defective unit. Separate part numbers are available for each intensity (see Chapter 7). If a replacement unit of the same intensity is not available, another intensity (i.e., alpha-code) may be used ONLY WHEN AN OBVIOUS MISMATCH DOES NOT RESULT. Before soldering the replacement unit in place, be sure that it is correctly aligned with the existing units.

Replacing A&Rs or C&Ts

At the time of this printing, either MOSTEK or AMI manufactured A&R or C&T units may be used as replacement parts for any calculator. If incompatabilities are found, you will receive information describing those incapabilities via CPD Inter-Office Service Memos (IOSM).

THE BOARD-TEST SYSTEM

The board test system consists of an ET 7074 Board Tester, a 9821A (Opt. 001) Calculator, a duplicate of the board being tested (i.e., a standard), and the software listed in Table 6-2. Information describing the system installation procedures is provided in the 'ET 7074 Board-Test System Operating and Service Manual'.

System Operation

Tests on the circuit boards are performed under control of the 9821A. The test system first attempts to synchronize the device-under-test (DUT) with the standard unit. Then, if the two boards synchronize, the tester utilizes commands from the 9821A to perform identical operations in the DUT and standard unit while, at the same time, comparing the DUT's inputs and outputs to those of the standard unit. If any of the inputs or outputs fail to compare, the test is stopped and information which describes signals in error and when the error occurred is sent to the 9821A. The 9821A then lists the error information, after which the tester is instructed to retest the circuit board. If the DUT fails the retest, the error information is again printed. Otherwise, 'RETEST' is printed. If, at any time, the tester sends the 9821A non-valid error information, 'MALFUNCTION' is printed to inform you that the test-system malfunctioned.

The 9821A Software

When properly used, the 9821A software (see Table 6-2) controls the tests being performed by the system and outputs the test results to the operator. The following explanations describe the software used for the tests.

Table 6-2. Board-Test Software

FILE NO.	FILE SIZE	CONTENTS
18	100	Special Program 'BDT'
19	150	Board-Test Supervisor
20	200	Models 46 & 81 Control Program
21	50	Model 46 Commands (R41)
22	50	Model 81 Commands (R35)
23	250	Model 81 Keyboard Buffer Control Program
24	100	Model 81 Keyboard Buffer Commands (R59)
25	225	Model 9805A Control Program
26	50	9805A Motherboard/Fatherboard Commands (R21)
27	50	Plotter Interface Commands (R15)
28	50	Data Storage Ass'y Commands (R14)
29	50	Single-Step Control Program
30	75	Keycode-Looping Control Program
31	75	Command Lister Program
32	75	Command Loader Program
33	75	Spare File
34	75	Spare File
35	250	Spare File
36	250	Spare File
37	75	Spare File
38	75	Spare File
39	75	Spare File
40	75	Spare File

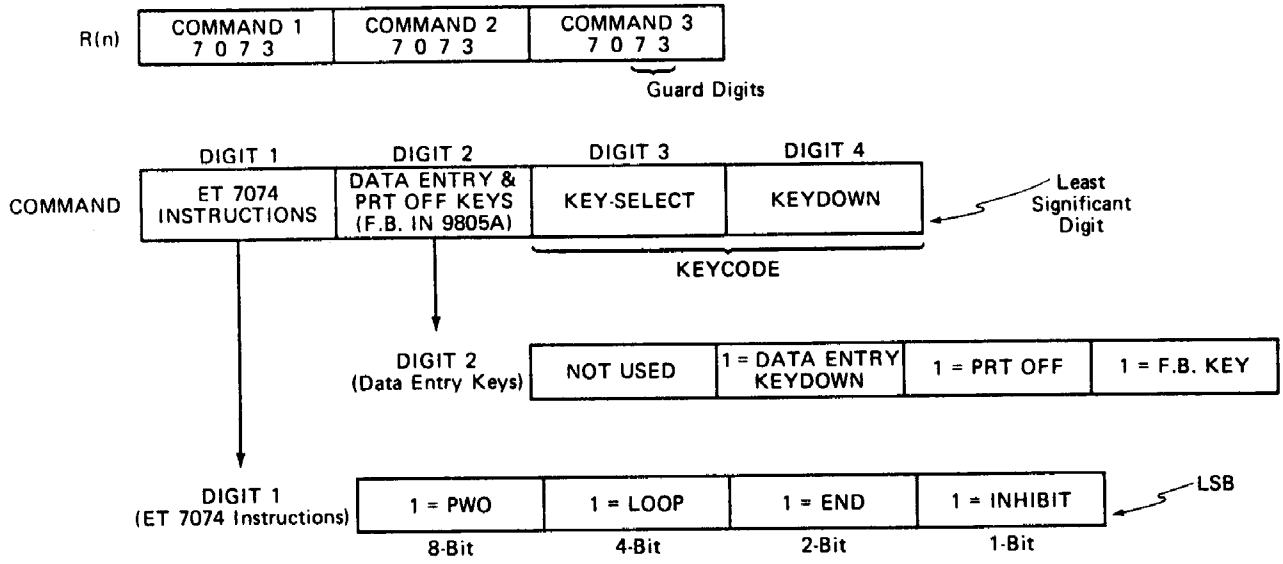
The Binary program, special program 'BDT', controls the information input to, and output from, the 9821A. After be 'called' by the control program, the binary program uses the commands in the 9821A data registers to specify operations performed by both the DUT and the standard unit. The test results are received by the binary program a stored in designated 9821A data registers where they can be recalled, then printed, by the control program.

The control program 'calls' special program BDT and, when the test is complete, recalls the test results from appropriate data registers and prints the error messages on the printer. The program then returns control of the tests the binary program so the board can be retested and the results of the retest printed.

If the binary program receives a non-valid error code from the tester, the control program prints 'MALFUNCTION'.

The commands stored in the 9821A data registers are unique to each type of circuit board. Each command consists four BCD digits (see Figure 6-1). Because three commands (i.e., 12 BCD digits) are stored in each register, use of the t guard-digits is required. Thus, a program is required to list or load the entire 12-digit command-set in each register (Figure 6-2). Each command in the data registers are in three parts:

- The most significant digit (MSD) specifies the function of the command. A BCD 6 is 'send keycode' and an 8 o instructs the tester to issue a PWO signal. A 7 or 1 instructs the tester to 'inhibit the keycode'; the keycode is se but comparisons of the DUT and standard unit signals are not performed. This allows initialization of the boa before tests are begun. A BCD 4 instructs the tester to 'loop on the keycode' (use of a BCD 4 is described later this chapter). A BCD 2 indicates the test is complete.
- The next BCD digit specifies the data-entry format (e.g., AUTO DECIMAL on the Model 5 and Model 81) a PRINT OFF modes of operation. The most-significant-bit (MSB) position of this digit is not currently used and t LSB position is only used to specify that the keycode is for the 9805A Stat Block.
- The final portion of each command is the two least significant digits. These digits specify the keycode which issued by the command.



Inhibit always inhibits the keycode.
If 4-bit and 2-bit are set, the instruction is 'send keycode'.

For Example:

A command 7073 indicates a keycode 73 which is inhibited.
A command 6023 indicates a keycode 23 which is sent to boards.
A command 6524 indicates a keycode 24 from the function block to be sent with AUTO DECIMAL key down.
A command 6226 indicates a keycode 26 sent with PRT OFF down.
A command 2000 indicates the end of test.

Figure 6-1. The Test-system Command Format

```
0:
FXD 0;10→B;15→A⊢
1:
IF B=10;0→B;PRT
"REGISTER",A⊢
2:
PRT (RA+1E14-1.0
00000000005E14)1E
-4⊢
3:
RA-(RA+1E15-1E15
)→X;IF X≤-1;PRT
X+10000;GTO 5⊢
4:
SPC 3;PRT "FINAL
 REGISTER",A;
SPC 14;GTO 6⊢
5:
B+1→B;A+1→A;SPC
1;GTO 1⊢
6:
END ⊢
Σ23000
```

NOTE

This program prints all 12 digits in each data register. The commands are numbered left-to-right in each register.

Figure 6-2. 9821A Data Register 12-digit Command Listing Program

ET 7074 TEST PROCEDURE

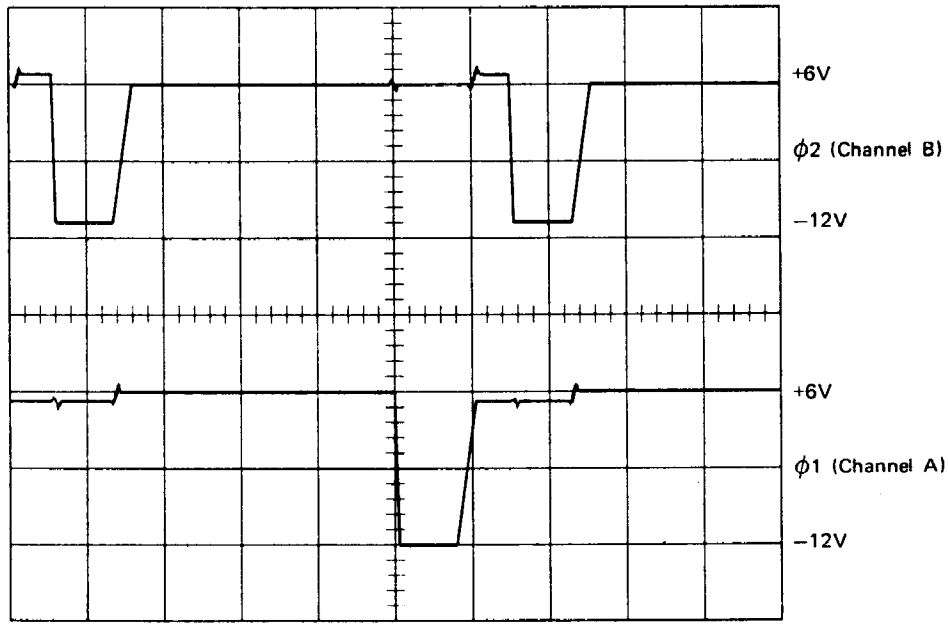
> **NOTE**
>
> The Board-Test System may not provide understandable test results if either the board being tested or the standard unit contains any defective ROMs.

Before beginning this test procedure, perform the procedure in Chapter 5. Then, verify proper power supply and clo operation. The power supply specifications are given in Table 6-3, while the method of testing the clocks is shown Figure 6-3.

Table 6-3. Power Supply Specifications

NOMINAL VOLTAGE	46/81 LIMITS	9805A LIMITS
+5V (9805A)	N/A	+4.75 +5.25
+6V	+5.5V to +6.5V	+5.6V to +6.6V
+15V	+14V to +16.5V	+14.1 to +16.2
-12V	-11V to -13V	-11.2 to -13.2*

* The ET 7074 tests on the 9805A -12V supply are dependent on the +6V supply output.



180C SETTINGS	
1801A Vertical Amp	**1810C Time Base Unit**
INPUT: Channel A (Φ1); DC Channel B (Φ2); DC	TIME/DIV: 1 μsec (CAL)
VOLTS/DIV: (A&B) .5 (with 10:1 input probe & CAL adjusted to .9 V/CM	SWITCH POSITIONS: All buttons should be out (blue) except the AUTO/NORM and ac/dc switches which should be in (black).
DISPLAY: ALT B (A&B) + UP	

Figure 6-3. Scope Settings and Waveforms for Clock Tests

If testing the power supplies and clock inputs to the board indicates any failures, those failures must be corrected before continuing subsequent tests.

Verify that the C&T and A&R circuits in the standard unit are from the same manufacturer (i.e., either MOSTEK or AMI circuits) as the corresponding circuits in the DUT. The two manufacturers build these circuits somewhat differently, resulting in slightly different operation. Thus, if a circuit is tested by comparing it with a similar circuit from a different manufacturer, incorrect test results will occur.

NOTE

If, after performing tests using the ET 7074, you are not sure what is causing your particular failure, you may wish to perform the test procedures at the end of this chapter.

IMPORTANT NOTE

The C&T in both the standard unit and the DUT must be from the same manufacturer – either MOSTEK or AMI. This also applies to the A&R in both units.

Now install the board being tested into the test system and load the correct programs into the 9821A. Information describing the installation procedures is provided in the 'Board-Test System Operating and Service Manual'.

After the system is properly installed and the appropriate software is loaded into the 9821A, the board tests may be run by pressing END, EXECUTE...RUN PROGRAM. If you are not sure what software to use, load, then run the program in File 0.

Interpreting the Test Results

If 'PASS' is displayed by the 9821A, the board is operating correctly. If, on the other hand, 'MALFUNCTION' is printed at any time, the 'test system' is *not* operating correctly. In the latter case, the test should be rerun. If MALFUNCTION is again printed, the test system is defective and must be repaired before further tests can be performed.

It should be noted that the test system's checks of the DUT's circuit boards are so thorough and accurate that failures are sometimes found in calculators that *appear* to be operating correctly.

NOTE

If the 9821A displays 'NOTE 25', special program 'BDT' is not stored in memory; either the incorrect program was stored in memory or none of the special programs exists in memory.

If the DUT fails the test, the 9821A will first list all information describing when the failure occurred; this information includes the last command and keycode issued and the precise word-and-bit-times during which the first incorrect signal was detected. The important facts in this printout are:

- If the command number is 0, then the DUT never fully synchronized with the standard unit. This may be due to power supply, clock, PWO, or SYNC failures, whichever is indicated in the incorrect signal listing.
- If the failure is in any command other than 0, the failure occurred *after* the two boards were synchronized. The information in this printout is particularly useful in duplicating the failure using the DUT's keyboard. Duplication of the failure is accomplished by using Table 6-5 to find the command (hence, the keycode) which was being processed when the failure occurred. The key(s) corresponding to that keycode should then be pressed to duplicate the failure. If you wish to continually repeat those keycodes, the keycode looping program from File 30 may be used in place of the control program. When 'COMMAND' is displayed, enter any 4-digit (from Table 6-5) command you wish to test. *The last command must be 4000*, which automatically starts the test. More than one command may be entered.

```
0:
15→A;0→B→R15⊢
1:
ENT "COMMAND ?",
C;RA=1E4+C→RA⊢
2:
IF C=4000;GTO 5⊢
3:
B+1→B;IF B=3;A+1
→A;0→B→RA⊢
4:
GTO 1⊢
5:
*CSP "BDT",4,R15
,R0⊢
6:
IF FLG 1;GTO 5⊢
7:
*CSP "BDT",0,R15
,R0;GTO 6⊢
8:
END ⊢
Σ1607
R403
```

Figure 6-4. The Keycode Looping Program

> **NOTE**
>
> This program should be used in place of the control program. Then, when 'COMMAND?' is displayed, enter any 4-digit command from Table 6-5; the last command entered must be 4000.

The next information on the 9821A printout is last addresss, address (i.e., current address), group and ROM. T information indicates which ROM was active, together with the current and preceding address, when the failure occur Remember, there are 4 ROMs in a quad-ROM and no more than 2 quad-ROMs or eight single ROMs in a group.

> **NOTE**
>
> Ignore the ROM Group information when testing 9805A circuit boards.

Either IS1 or IS2 is printed next. IS1 indicates that the C&T, A&R, and processor are all executing the ROM instructi IS2 instructions are received only by the I/O processor.

If the last WS signal issued was from the C&T, 'WS FROM C&T' is printed. If the last WS signal originated in a ROM, printout is given.

If the next printout is 'DSTC' (data storage to C register in the A&R), then a data storage unit, located on the DUT, inputting BCD data to the A&R when the failure occurred. If DSTC is printed and, later in the signal error printou BCD error is printed, the data storage unit is defective.

WORD and BIT, the next information provided, tells you exactly when the error occurred after the last keycode issued. If the bit-time printed is greater than 55, the systems probably were not synchronized.

After the word and bit information is printed, a complete list of signals which were incorrect at the time the first error was detected, is provided. The signal which is printed first is usually the first incorrect signal found by the tester. Table 6-4 provides a few of the more common failures and the associated indications from the printout.

When the first test is complete, the board is retested and the error information is again printed (if the retest is accomplished with no failures, 'RETEST' is printed). It is particularly important to note any differences found during the retest. If a considerable number of differences occur, you should rerun the entire test. Then, compare all of the printouts and determine which signals were consistently incorrect. Those signals are probably the key to isolating the hardware failure.

The ET 7074 Display

The ET 7074 displays three numbers after detecting an error: The two-digit error number corresponds to the lowest-numbered signal which failed the test (see Tables 6-6). The BIT and WORD display information duplicates the information on the printout.

Table 6-4. Common Failures and Associated Error Signals

SIGNAL(S) IN ERROR	POSSIBLE CAUSE
COMMAND 79 Keycode 30 (Model 46)	DUT and standard C&T's dissimilar manufacturer
DSTC with BCD errors	Defective data storage circuit
BCD errors (Models 46 or 81)	Probably defective data storage circuit, but could be A&R or processor
BCD errors (9805A)	Defective A&R or I/O processor
Ia errors	Probably defective C&T
WS errors (Not 'WS from C&T')	Probably defective C&T
Is = 0, with BCD or CRY error	Defective A&R
C1 through C18 errors	Defective I/O processor or associate output circuit
CRY or SRT errors	Often defective A&R
SCE errors	Defective I/O processor
COMMAND 0, WORD 0, SYNC error	Defective C&T
COMMAND 0, WORD 0, clock error	Defective clock driver
COMMAND 0, WORD 0, PWO error	Defective PWO circuit or defective C&T (SYNC)
COMMAND 0, WORD 0, IOC1, 2, or 3 error	Defective C&T
Word 0 errors of the first uninhibited command	Defective C&T
All printer hammers chatter	TP or TR inputs to processor incorrect

Table 6-5. Board-Test System Commands

MODEL 46 BOARD TEST COMMANDS						
COMMAND NO.		COMMAND	KEY	COMMAND NO.	COMMAND	KEY
R(15)	1	7064	7	41	6063	8
	2	6063	8	42	6062	9
	3	6062	9	43	6073	CHS
R(16)	4	6076	Enter↑	44	6072	EEX
	5	6024	4	45	6064	7
	6	6023	5	46	6006	FIX
7		6022	6	47	6064	7
8		6026	+	48	6022	6
9		6020	Prt	49	6044	0
10		6013	STO	50	6053	SIN
11		6034	1	51	6054	TO POL
12		6032	3	52	6073	CHS
13		6033	2	53	6060	Shift
14		6013	STO	54	6054	REC
15		6033	2	55	6042	$\Sigma+$
16		6012	RCL	56	6014	R↓
17		6036	x	57	6042	$\Sigma+$
18		6034	1	58	6016	$x \rightleftarrows y$
19		6013	STO	59	6060	Shift
20		6066	–	60	6016	!
21		6033	2	61	6060	Shift
22		6060	Shift	62	6014	$\bar{x}$,s
23		6006	SCI	63	6060	Shift
24		6074	7	64	6042	Shift
25		6060	Shift	65	6060	$\bar{x}$,s
26		6056	$\sqrt{x}$	66	6073	RAD
27		6060	Shift	67	6060	Shift
28		6004	y^x	68	6043	π
29		6034	1	69	6060	Shift
30		6044	0	70	6013	DM←
31		6013	STO	71	6060	Shift
32		6032	3	72	6072	GRD
33		6060	Shift	73	6060	Shift
34		6040	Δ%	74	6050	ATN
35		6074	LAST X	75	6052	COS
36		6013	STO	76	6012	RCL
37		6046	÷	77	6024	4
38		6032	3	78	6060	Shift
39		6013	STO	R(41) 79	6030	ALL
40		6024	4	80	8000	(PWO)
				81	2000	(END TEST)

Table 6-5. Board-Test System Commands (Cont'd)

MODEL 81 KEYCODE COMMANDS					
COMMAND NO.	COMMAND	KEY	COMMAND NO.	COMMAND	KEY
R(15) 1	6034	1	32	6434	1
R(15) 2	6033	2	33	6434	1
R(15) 3	6072	STO	34	6462	9
R(16) 4	6444	0	35	6464	7
R(16) 5	6456	i	36	6432	3
R(16) 6	6422	6	37	6472	STO
7	6472	STO	38	6464	7
8	6434	1	39	6476	SAVE
9	6402	PV	40	6450	DAY
10	6464	7	41	6462	9
11	6472	STO	42	6404	N
12	6433	2	43	6472	STO
13	6404	n	44	6463	8
14	6440	FV	45	6424	4
15	6472	STO	46	6423	5
16	6432	3	47	6403	PMT
17	6416	x⇄y	48	6472	STO
18	6472	STO	49	6462	9
19	6424	4	50	6442	EXT
20	6422	6	51	6462	9
21	6473	CHS	52	6430	CLEAR
22	6453	TL	53	6470	RCL
23	6472	STO	54	6403	PMT
24	6423	5	55	6460	Shift
25	6423	5	56	6446	÷
26	6453	TL	57	6403	PMT
27	6472	STO	58	6463	8
28	6422	6	59	6456	i
29	6434	1	60	6460	Shift
30	6443	.	61	6402	BND
31	6433	2	62	2000	END TEST

Table 6-5. Board-Test System Commands (Cont'd)

9805A MAINFRAME COMMANDS FOR ET 7074 TEST SYSTEM					
COMMAND NO.	COMMAND	KEY	COMMAND NO.	COMMAND	KEY
R(15) 1	7073	(inhibit test)	34	6270	Shift
R(15) 2	7073	(inhibit test)	35	6214	1/x
R(15) 3	7073	(inhibit test)	36	6236	%
R(16) 4	6226	(print OFF)	37	6216	)
R(16) 5	6633	2 (auto decimal)	38	6272	RND
R(16) 6	6243	5	39	6222	.
7	6240	+	40	6270	Shift
8	6226	(	41	6240	e^x
9	6253	8	42	6270	Shift
10	6250	–	43	6213	LN_x
11	6226	(	44	6250	–
12	6244	4	45	6243	5
13	6242	6	46	6270	Shift
14	6266	Cancel Entry	47	6226	CHS
15	6234	1	48	6216	)
16	6222	.	49	6213	X
17	6243	5	50	6254	7
18	6226	(	51	6233	2
19	6234	1	52	6270	Shift
20	6233	2	53	6250	x/12
21	6252	9	54	6216	)
22	6212	÷	55	6212	÷
23	6226	(	56	6243	5
24	6234	1	57	6242	6
25	6223	0	58	6216	)
26	6214	↑	59	6020	=(Print ON)
27	6244	4	60	6256	STO (Print OFF)
28	6232	3	61	6273	CLEAR
29	6216	)	62	6246	RECALL
30	6270	Shift	63	6276	PRINT
31	6212	LGx	64	9000	PWO
32	6240	+	65	2000	END
33	6632	3			

Table 6-5. Board-Test System Commands (Cont'd)

PLOTTER COMMANDS			
COMMAND	KEYCODE	KEY	EXPLANATION
1	6073	CLEAR	
2	6034	1	
3	6043	5	
4	6056	Store	
5	6023	0	Commands 2-10
6	6070	Shift	Set up graph limits
7	6076	Print	of $X_{max} = 15$, $X_{min} = 0$
8	6034	1	
9	6034	1	
10	6063	Last Entry	
11	6034	1	
12	6023	0	
13	6056	Store	
14	6023	0	Commands 11-19
15	6070	Shift	Set up graph limits
16	6076	Print	of $Y_{max} = 10$, $Y_{min} = 0$
17	6034	1	
18	6033	2	
19	6063	Last Entry	
20	6034	1	
21	6056	Store	
22	6034	1	Commands 20-29
23	6023	0	Raise the plotter pen
24	6070	Shift	and move it to (1, 10)
25	6076	Print	then lower the pen.
26	6034	1	Move pen to coordinate
27	6012	÷	Lower pen
28	6022	.	
29	6063	Last Entry	
30	6023	0	
31	6070	Shift	
32	6076	Print	Commands 30-35 Plot
33	6034	1	a line from previous
34	6040	+	coordinates to (1, 0)
35	6063	Last Entry	
36	6034	1	
37	6044	4	
38	6056	Store	
39	6034	1	
40	6023	0	Commands 36-46
41	6070	Shift	Raises plotter pen
42	6076	Print	and moves it to (14, 10)
43	6034	1	and then lowers the pen
44	6012	÷	
45	6022	.	
46	6063	Last Entry	
47	9000	PWO	
48	2000	END	

Table 6-5. Board-Test System Commands (Cont'd)

30 DATA REGISTER KEYCODES			
COMMAND	KEYCODE	KEY	EXPLANATION
1	6072	RND	
2	6022	.	SET Precision
3	6070	Shift	
4	6064	St. Prgm	
5	6023	0	
6	6020	=	Clear all Data Registers
7	6034	1	
8	6033	2	
9	6032	3	
10	6044	4	
11	6043	5	Number to be stored
12	6042	6	
13	6054	7	
14	6053	8	
15	6052	9	
16	6070	Shift	
17	6056	Store	
18	6023	0	
19	6020	=	Store number in 0
20	6070	Shift	
21	6056	Store	
22	6034	1	
23	6023	0	
24	6020	=	Store number in 10
25	6070	Shift	
26	6056	Store	
27	6033	2	
28	6023	0	
29	6020	=	Store number in 20
30	6070	Shift	
31	6046	Recall	
32	6023	0	
33	6020	=	Recall number from 0
34	6070	Shift	
35	6046	Recall	
36	6034	1	
37	6023	0	
38	6020	=	Recall number from 10
39	6070	Shift	
40	6046	Recall	
41	6033	2	
42	6023	0	
43	6020	=	Recall number from 20
44	9000	PWO	
45	2000	END	

Table 6-6. Board-Test System Signal Error Codes

MODEL 46 & 81 ERROR CODES			
ERROR CODE	SIGNAL	ERROR CODE	SIGNAL
0	SYNC	46	C7
1	SRT	47	C8
2	IA	48	C9
3	IS	49	C10
4		50	C11
5		51	C12
6		52	C13
7		53	C14
8	WS	54	C15
9		55	C16
10	CRY	56	C17
11		57	C18
12	A	58	RED
13	B	59	ADV
14	C	60	TP
15	D	61	TR
16	E	62	
17	FLG	63	
18	ENABLE	64	
19		65	
20	BCD	66	PWO
21		75	
22		76	
23		77	
24	SBL	78	
25		79	
26		80	KS0
27		81	KS1
28	SCE	82	KS2
29		83	KS3
30		84	KS4
31		85	KS5
32		86	KS6
33	FLG'	87	KS7
34	EIS1	88	KD0
35	IOC2	89	KD2
36		90	KD3
37	IOC3	91	KD4
38		92	KD6
39	IOC1	93	
40	C1	94	POWER
41	C2	95	CLOCKS
42	C3	96	
43	C4	97	8000 WORDS
44	C5	98	POWER
45	C6	99	PWO

Table 6-6. Board-Test System Signal Error-Codes (Cont'd)

9805A ERROR CODES					
ERROR CODE	SIGNAL	ERROR CODE	SIGNAL	ERROR CODE	SIGNAL
00	SYN	33	FLG'	66	PWO
01	STRB	34	EIS1	67	
02	IA	35	GIOE	68	
03	IS	36	LATCH	69	
04	ISB	37	YINTF	70	
05	IS1	38	READ	71	
06	IA(MOS)	39	WRITE	72	
07	IS(MOS)	40	C1	73	
08	WS	41	C2	74	
09	WSB	42	C3	75	FKD0
10	CRY	43	C4	76	FKD2
11	WS(MOS)	44	C5	77	FKD3
12	DATA A	45	C6	78	KKD4
13	DATA B	46	C7	79	FKD6
14	DATA C	47	C8	80	FS0
15	DATA D	48	C9	81	FS1
16	DATA E	49	C10	82	KS2
17	FLG	50	C11	83	KS3
18	EXT	51	C12	84	KS4
19	MPNO	52	C13	85	KS5
20	BCD	53	C14	86	KS6
21	BCDY	54	C15	87	KS7
22	BDE	55	C16	88	KD0
23	BLE	56	C17	89	KD2
24	BSYLT	57	C18	90	KD3
25	FBS	58	RED	91	KD4
26	SRA	59	ADV	92	KD6
27	SRB	60	TP	93	
28	SRC	61	TR	94	POWER SUPPLY
29	A	62	TG8	95	CLOCKS
30	B	63	TG9	96	
31	C	64	START(MOS)	97	8000 WORDS
32	RGC	65	X	98	POWER SUPPLY
				99	PWO

MODEL 46 AND MODEL 81 CHECKOUT PROCEDURES

Initial Checks

Before an attempt is made to repair the calculator, make the following quick checks to ensure that a failure has actually occurred:

1. Verify the customers complaint and ensure that the complaint is not caused by a user error.
2. If the calculator is completely inoperative, check the line fuse; replace it if necessary. If the line fuse blows again, the primary power circuit or a power supply is shorted and must be repaired before subsequent tests can be run.

Model 46 Display Checkout

> **NOTE**
>
> Model 46 units with serial numbers less than 200 may not display 0.00 when switched on. This symptom may be corrected by pressing [CLEAR]. The repair of this problem is not included under warranty.

The following key sequence will check the Model 46 display for missing segments.

PRESS: [8] [.] [8] [8] [8] [8] [8] [8] [8] [8] [8] [CHS] [EEX] [CHS] [8] [8]

DISPLAY: `-8.8888888888-88`

> **NOTE**
>
> This test does not check all of the decimal-point segments.

Model 46 Printer Checkout

The following key sequence will check the Model 46 printer operation.

PRESS: [CLEAR] [1] [2] [3] [4] [5] [6] [7] [8] [9] [0] [CHS] [PRINT] [CHS] [e^x] [PRINT]

CORRECT PRINTOUT:

```
CLEAR
-1.234567890+09  ◊

                  ΣS
                  e^x
 9.999999999+99  ◊
```

The keyboard and basic Model 46 operation may be checked by performing the Key Sequence Test (Table 6-8).

CHAPTER 6
TROUBLESHOOTING CIRCUIT BOARDS

Model 81 Printer and Display Checkout

The following sequence will check the Model 81 display for missing segments and the printer operation. The DECIM/ key must be down.

KEY	PRINTER	DISPLAY
CLR	CLEAR	0. 00
SHIFT		0. 00
9		0. 000000000 00
–	.000000000+00 -	0. 000000000 00
1		1. -09
2		1. 2 -08
3		1. 23 -07
.		1. 23 02
4		1. 234 02
5		1. 2345 02
6		1. 23456 02
7		1. 234567 02
8		1. 2345678 02
9		1. 23456789 02
SAVE	1.234567890+02	1. 234567890 02
y^x	M N O T E 1	9999999999 99 ← Flashing
CHS	S	-9. 9999999999 99
◇	-9.999999999+99◇	-9. 9999999999 99

Red

*NOTE – SIGN ON EXPONENT

NOTE

This test does not check all of the display decimal-point segments.

Table 6-7. Model 81 Key Sequence Test

KEY	PRINTER	DISPLAY
CLEAR	CLEAR	0. 00
1		1.
.		1.
0		1. 0
1		1. 01
1		1. 011
9		1. 0119
8		1. 01198
0		1. 011980
SAVE	1.011980	1. 01
3		3.
6		36.
5		365.
SHIFT		365.
DAT	365.00 D A T E 3 12.311980	12. 31

KEY	PRINTER	DISPLAY
CLEAR	CLEAR	0. 00
9		9.
n	9.00 - N	9. 00
9		9.
PMT	9.00 -PT	9. 00
1		1.
0		10.
0		100.
FV	100.00 - F	100. 00
i	I N T 5.19	5. 19

Table 6-7. Model 81 Key Sequence Test (Cont'd)

KEY	PRINTER	DISPLAY
CLEAR	CLEAR	0.00
6		6.
SAVE	6.00 ↑	6.00
X	×	36.00
	36.00 ◇	
9		9.
÷	9.00 ÷	4.00
	4.00 ◇	
STO		4.00
3	→3	4.00
5		5.
Σ+	5.00 Σ+	5.00
RCL		5.00
3	↑	4.00
	4.00 →3	
Σ+	4.00 Σ+	9.00
x̄	.44	0.22
	N 9.00	
	x̄ .22	
x≷y	.44 ≷	0.44
y^x	M↑	0.52
	.52 ◇	
SHIFT		0.52
$\sqrt{x}$	√	0.72
	.72 ◇	
CHS	S ≷ -	0.72
*	- .72 *	0.00

Red

KEY	PRINTER	DISPLAY
CLEAR	CLEAR	0.00
9		9.
n	9.00 → N	9.00
6		6.
i	6.00 → I	6.00
1		1.
0		10.
0		100.
PV	100.00 →P	100.00
SHIFT		100.00
INT	I N T	0.15
	.15	

KEY	PRINTER	DISPLAY
CLEAR	CLEAR	0.00
1		1.
SAVE	1.00 ↑	1.00
5		5.
i	5.00 → I	5.00
5		5.
PMT	5.00 →PT	5.00
SHIFT		5.00
.BND	P R I C E	100.00
	TO MAT	
	100.00	

KEY	PRINTER	DISPLAY
CLEAR	CLEAR	0.00
1		1.
STO		1.
TL	1.00 →3*	1.00
1		1.
TL	1.00 T	1.00
5		5.
STO		5.
TL	5.00 →3*	5.00
3		3.
TL	3.00 T	2.00
SHIFT		2.00
CAL (TL)	T L	0.50
	FACTR	
	1.00	
	S .50	
	y .50	

KEY	PRINTER	DISPLAY
CLEAR	CLEAR	0.00
1		1.
STO		1.
1	1.00 →1	1.00
2		2.
STO		2.
2	2.00 →2	2.00
4		4.
i	4.00 → I	4.00
3		3.
PMT	3.00 →PT	3.00
5		5.
0		50.
PV		50.00
Σ+	50.00 →P	3.96
	Σ+	
	P V	
	47.96	
	I N T	
	3.96	

Table 6-8. Model 46 Key Sequence Test

SEQ NO.	KEY	PRINTER	DISPLAY
1	CLEAR	CLEAR	0.00
2	FIX		
3	8		0.00000000
4	1		1.
5	0		10.
6	ENTER	10.00000000 ↑	10.00000000
7	CLX		0.00000000
8	LAST X	← 0 10.00000000	10.00000000
9	E EX		1. 00
10	2		1. 02
11	PRINT	1.0000000000+02 ◇	1.00000000 02
12	CHS	≠S	−1.00000000 02
13	PRINT	1.0000000000+02 ◇	−1.00000000 02
14	3		3.
15	STO		
16	1	3.00000000 → 1	3.00000000
17	5		5.
18	STO		
19	2	5.00000000 → 2	5.00000000
20	8		8.
21	STO		
22	4	8.0000000000 → 4	8.00000000
23	9		9.
24	STO		
25	8	9.0000000000 → 8	9.00000000
26	LIST	LIST 3.00000000 ← 1 5.00000000 ← 2 0.00000000 ← 3 8.00000000 ← 4 0.00000000 ← 5 0.00000000 ← 6 0.00000000 ← 7 9.00000000 ← 8 0.0000000 ← 9	
27	RCL		
28	8	← 8 9.00000000	9.00000000
29	RCL		
30	4	← 4 8.00000000	8.00000000
31	X	×	72.00000000
32	RCL		
33	1	← 1 3.00000000	3.00000000
34	÷	÷	24.00000000
35	RCL		
36	2	← 2 5.00000000	5.00000000
37	−	−	19.00000000
38	x≠y	≠	9.00000000
39	+	+	28.00000000
40	PRINT	28.00000000 ◇	28.00000000
41	R↓	↓	8.00000000
42	FIX		
43	2		8.00
44	SIN	S	0.14
45	SHIFT		
46	ASN	AS	8.00
47	COS	C	.99

SEQ NO.	KEY	PRINTER	DISPLAY
48	SHIFT		
49	ACS	AC	8.00
50	TAN	T	0.14
51	SHIFT		
52	ATN	AT	8.00
53	TO POL	TO POLAR 45.00 ◇ 11.31 ◇	11.31
54	SHIFT		
55	REC	TO RECT 8.00 ◇ 8.00 ◇	8.00
56	7		7.
57	Σ+	7.00 Σ+	1.00
58	6		6.
59	Σ+	6.00 Σ+	2.00
60	SHIFT		
61	x̄,Δ	# 2.00 ◇ 0.71 σ◇ 6.50 x̄ ◇	6.50
62	SHIFT		
63	CLR	CLEAR	0.00
64	1		1.
65	2		12.
66	1/x	12.00 %	0.08
67	x≠y	≠	0.00
68	SHIFT		
69	y^x	y^x	1.00
70	SHIFT		
71	10^x	e^x	10.00
72	X^2	#	100.00
73	SHIFT		
74	$\sqrt{x}$	r	10.00
75	SHIFT		
76	LOG	lg	1.00
77	ln	ln	0.00
78	e^x	e^x	1.00
79	%	%	0.00
80	SHIFT		
81	Δ%	Δ% NOTE 1	0 0 0 0 0
82	SHIFT		
83	n!	!	1.00
84	SHIFT		
85	RAD	RAD	1.00
86	SHIFT		
87	GRD	GRD	1.00
88	SHIFT		
89	C/I	2.54	2.54
90	SHIFT		
91	π	3.14	3.14
92	SHIFT		
93	DEG	D	3.14
94	SHIFT		
95	DM→	DMS→	3.24
96	SHIFT		
97	DM←	DMS←	3.1416
98	SHIFT		
99	STK	0.00 ←S◇ 1.00 ←S◇ 2.54 ←S◇ 3.14 ←S◇	3.14

9805A CHECKOUT PROCEDURES

Initial Checks

Before an attempt is made to repair the Model 5, a few quick checks should be made to ensure that a failure has actually occurred:

1. Verify the customer's complaint and ensure that the complaint is not due to some type of user error.
2. Check for an improperly installed system.
3. If the calculator is completely inoperative, check and, if necessary, replace the line fuse. If the line fuse blows again, the instrument is defective and must be repaired.
4. Disconnect any installed peripherals and verify that a peripheral is not the source of the trouble.
5. Use the special System Test PROM (-hp- P/N 9805-90031) to check the calculator — see 'Using the System Test PROM' on the following pages.

> **NOTE**
>
> The Power Supply Test Assembly (5060-9199) should be installed in one of the I/O slots (component side to the left) and each of the power supplies tested before performing any of the following procedures. Each power supply output should be within the tolerances given below.

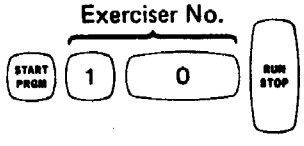
Supply	Tolerance
+5Vdc	+4.75 to +5.25
+6Vdc	+5.6 to +6.6
−12Vdc	−11.2 to −13.2
+15Vdc	+14.1 to +16.2

6. A final test for the 9805A is to test the keyboard keys. This is accomplished by pressing each key, one at a time, and verifying that the correct operation occurs.

Using the System Test PROM

The Model 5 'System Test PROM' is programmed to test either the basic calculator, the data storage registers, the printer, or the plotter I/O card (which includes a cursory test of the 9862A Plotter). To use the PROM, perform the following procedure:

1. Switch the calculator OFF, and install the PROM. Then, remove any installed keyblock and peripheral (other than the plotter) and switch the system ON.
2. PRESS:

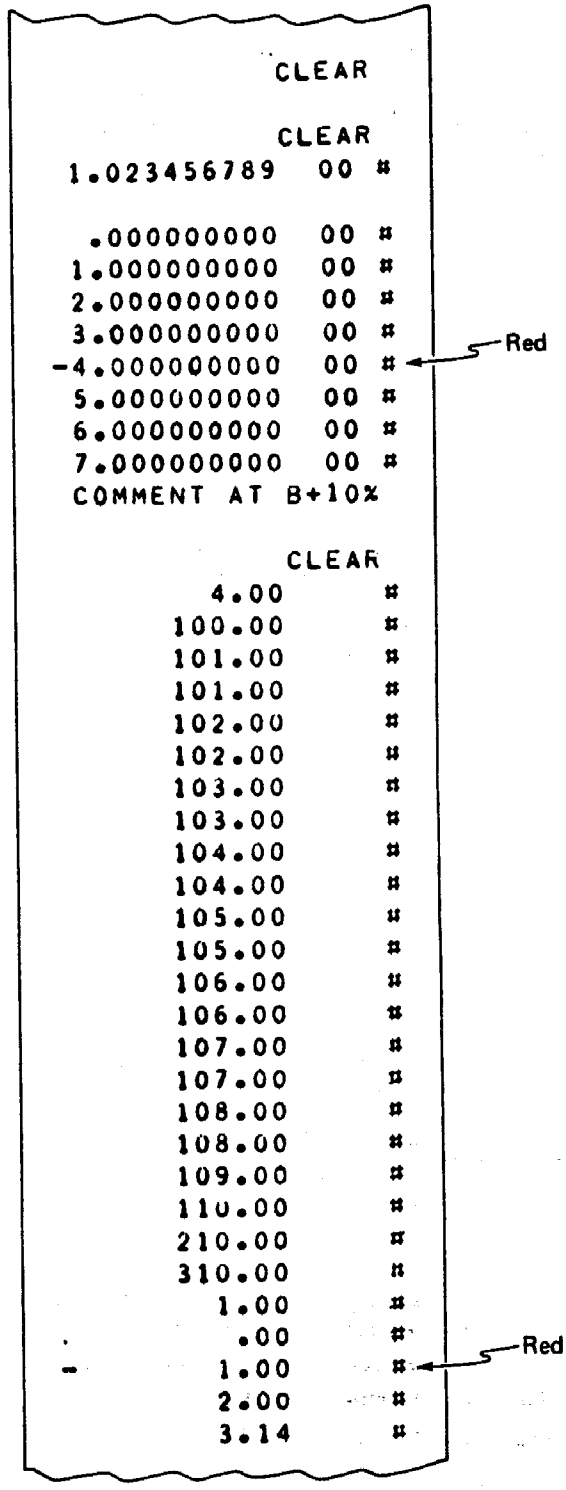


   Exerciser 10 is selected to test the basic machine. This key sequence can be used for other exercisers by replacing the 10 with the appropriate exerciser number (20, 30, or 40).
3. When 3.14 is printed and displayed, exerciser 10 is complete and the resulting printout should be the same as the exerciser 10 listing provided on the following page.
4. If any exerciser fails to run properly, see Table 6-9.
5. Exerciser 20 (Data Storage Register), 30 (Printer), or 40 (Plotter) may be run by performing the instructions given below, then using the key sequence from step 2 (with the appropriate exerciser number) to run the test.

NOTE

Exerciser 10 must be successfully completed before continuing to any other exerciser.

BASIC MACHINE PRINTOUT
Exerciser No. 10



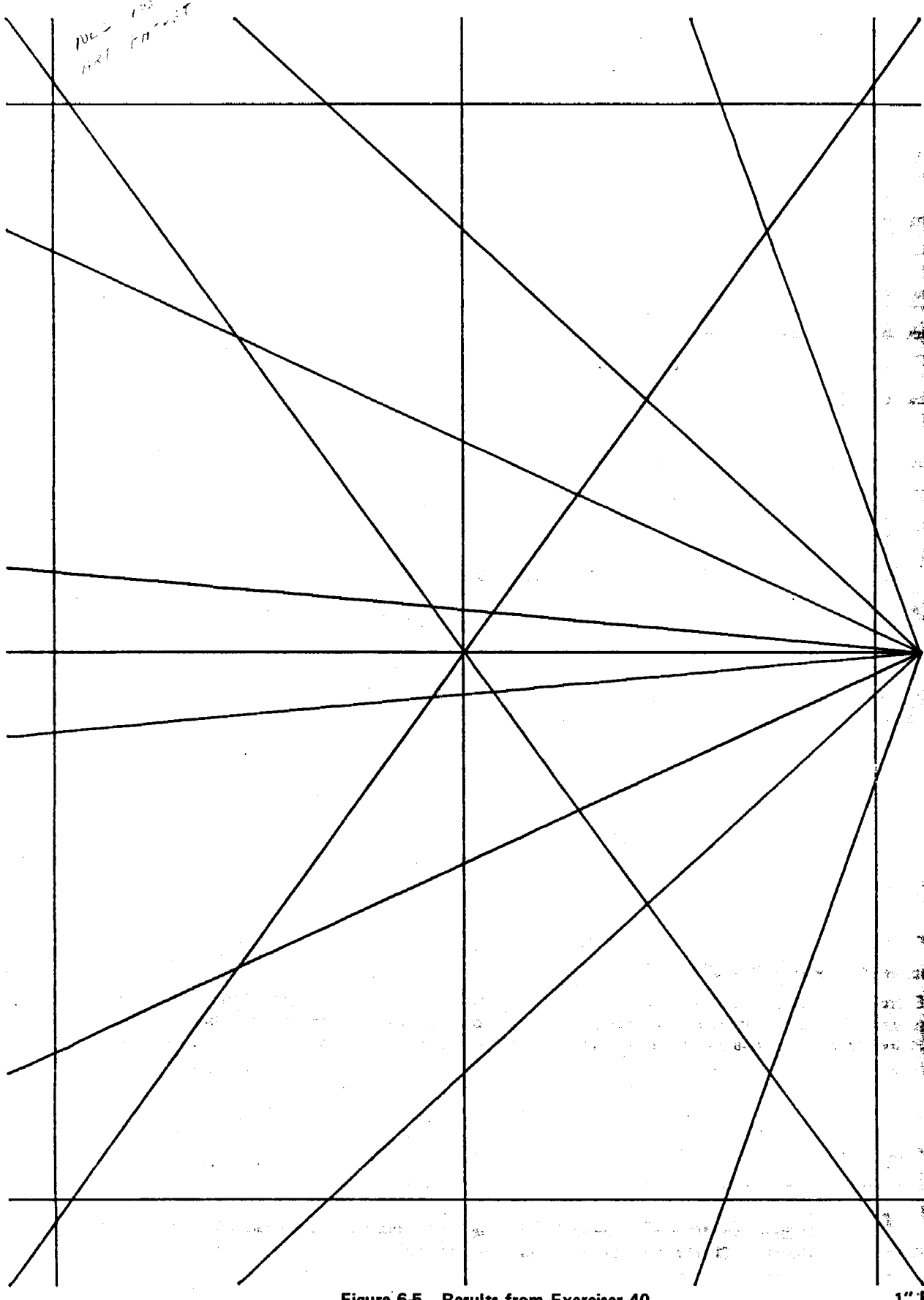
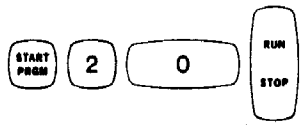


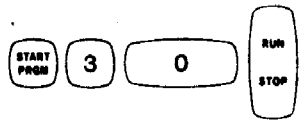
Figure 6-5. Results from Exerciser 40

Instructions for Exerciser No. 20

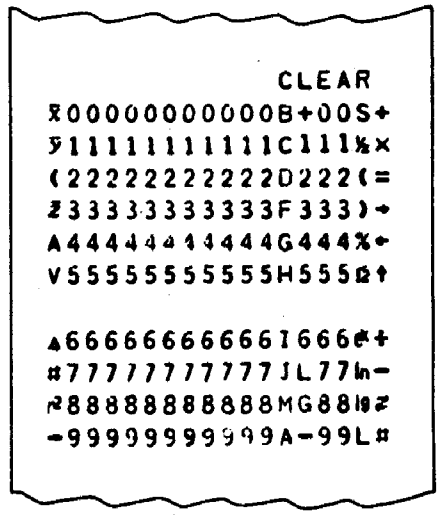
Run Exerciser 10, then PRESS: 

After 'DATACLEAR' is printed, input the number of registers which are installed in the calculator (30) and press RU
Each of the nine checks begins with the printing of DATA= 29 (the number of registers minus 1). Each of the 9 te
should result in a printout of the data in each register, separated into groups of 10 (i.e., 3 groups of 10). Each individ
check is complete when END is printed. The final (9th) printout is one decimal for each data register. The compl
exerciser may take up to 15 minutes.

Instructions for Exerciser No. 30

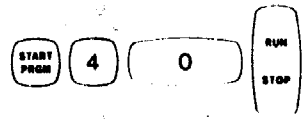
Run Exerciser 10, then PRESS: 

Exerciser 30 should result in the following printout.



Instructions for Exerciser No. 40

Run Exerciser 10 before beginning Exerciser 40. The plotter exerciser completely checks the plotter I/O card, but is o
a cursory check of the plotter. Before beginning the test, place a sheet of paper on the platen and set the two plot
limits 1 inch in from the edges of the paper. Then, run the exerciser by pressing:



NOTE

If Exerciser 40 runs properly, but the customer's plotter routines fail, the 'Statistics Keyblock Checkout Procedure' should be performed.

DATA STORAGE REGISTER PRINTOUT
Exerciser No. 20

```
          CLEAR


        DATACLEAR
        DATA      =

          29.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.

 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.

 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.

          END
```

```
                  DATA      =

                    29.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.

           123456790.
           123456790.
           123456790.
           123456790.
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           123456790.
           123456790.
           123456790.

           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.
           123456790.

                    END
```

```
                  DATA      =

                    29.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.

           123456789.
           123456789.
           123456789.
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           123456789.
           123456789.
           123456789.
           123456789.

           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.
           123456789.

                    END
```

DATA STORAGE REGISTER PRINTOUT
Exercise No. 20
(continued)

```
        DATA     =

          29.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.

   246913578.
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   246913578.
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   246913578.
   246913578.

   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.
   246913578.

           END
```

```
        DATA     =

          29.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.

 123456789.
 123456789.
 123456789.
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 123456789.

 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.
 123456789.

           END
```
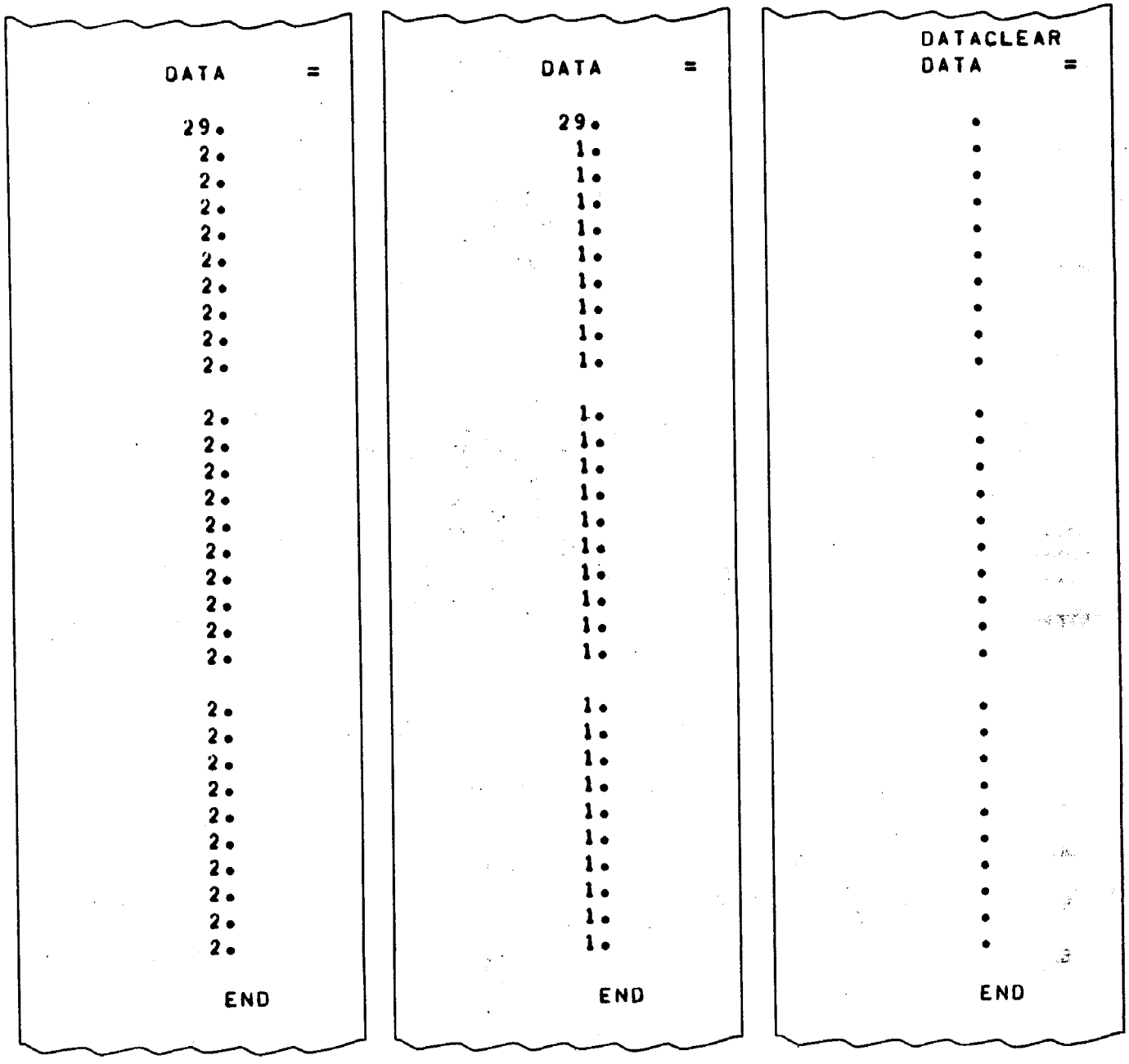

```
        DATA     =

          29.
           1.
           1.
           1.
           1.
           1.
           1.
           1.
           1.
           1.

           1.
           1.
           1.
           1.
           1.
           1.
           1.
           1.
           1.
           1.

           1.
           1.
           1.
           1.
           1.
           1.
           1.
           1.
           1.
           1.

           END
```

DATA STORAGE REGISTER PRINTOUT
Exercise No. 20
(continued)



```
DATA      =

 29.
  2.
  2.
  2.
  2.
  2.
  2.
  2.
  2.
  2.

  2.
  2.
  2.
  2.
  2.
  2.
  2.
  2.
  2.
  2.

  2.
  2.
  2.
  2.
  2.
  2.
  2.
  2.
  2.
  2.

 END
```

```
DATA      =

 29.
  1.
  1.
  1.
  1.
  1.
  1.
  1.
  1.
  1.

  1.
  1.
  1.
  1.
  1.
  1.
  1.
  1.
  1.
  1.

  1.
  1.
  1.
  1.
  1.
  1.
  1.
  1.
  1.
  1.

 END
```

```
DATACLEAR
DATA      =

  .
  .
  .
  .
  .
  .
  .
  .
  .
  .

  .
  .
  .
  .
  .
  .
  .
  .
  .
  .

  .
  .
  .
  .
  .
  .
  .
  .
  .
  .

 END
```

STATISTICS KEYBLOCK CHECKOUT PROCEDURE

NOTE

Exerciser 10 of the 'System Test PROM' must be successfully performed before this procedure is begun.

NOTE

This procedure should be used when you need to determine if a STAT keyblock is defective and a substitute keyblock is not available. If this procedure can successfu lly be performed and the customer's STAT Model 5 doesn't operate correctly, the PROM should be suspect. If this procedure cannot be performed correctly, the keyblock should be suspect. DO NOT SKIP STEPS UNLESS INSTRUCTED TO DO SO.

Setting Up the 9862A Plotter

Place a sheet of 8½" x 11" paper on the plotter platen and press the PAPER HOLD button down. Then, set the plot graph limits approximately 1" in from each of the paper's edges (see arrows on Figure 6-6). Remove any installed PRC

One Variable Checkout Procedure

NOTE

Part of the following procedures require plotter operations. If a plotter is not installed, perform only the specified steps. If any doubt exists as to correct plotter operation, perform Exerciser 40 of the 'System Test PROM'.

Remove any installed PROM, then ensure that the plotter (if installed) and calculator are properly connected and switched ON. Then, press the following keys in the exact sequence given and compare the printout (and plot) with th shown. If an error is made during an entry, return to step 1.

STEP:	PRESS:
1.	CLEAR
2.	RND ( ) 2
3.	VAR 0 1
4.	OFFSET WIDTH
5.	0 DATA ENTRY
6.	1 DATA ENTRY
	(continue to step 14 of this procedure if a plotter is not installed.)
7.	0 STORE
8.	5 AXES 1

PRINTOUT:

```
                CLEAR

V1    .......

                 0F      =
               .00       #

                   C E L=
              1.00       #




               .00       *

              RG1        =
               .00       #
              5.00       #
```

COMMENTS:

STEP:	PRESS:	PRINTOUT:	COMMENTS:
9.	5 AXES 2	RG2 = .00 # 5.00 #	
10.	1 STORE	1.00 →	
11.	AXES 3	T I = 1.00 # 1.00 #	
12.	0 STORE	.00 →	
13.	AXES 4	A I = .00 # .00 #	Plotter plots x and y axes before the Model 5 prints this.
14.	1 DATA ENTRY	1.00 #	
15.	2 DATA ENTRY 2 DATA ENTRY	2.00 # 2.00 #	
16.	3 DATA ENTRY 3 DATA ENTRY 3 DATA ENTRY	3.00 # 3.00 # 3.00 #	
17.	4 DATA ENTRY 4 DATA ENTRY 4 DATA ENTRY 4 DATA ENTRY	4.00 # 4.00 # 4.00 # 4.00 #	
18.	BASIC STAT	N = 10.00 # $\bar{x}$ = 3.00 # Δ1 = 1.05 #	

STEP:	PRESS:	PRINTOUT:	COMMENTS:
19.		HG 1.00 # .00 # .00 # .00 # 2.00 # 1.00 # 1.00 # 10.00 # 3.00 # 2.00 # 2.00 # 20.00 # 4.00 # 3.00 # 3.00 # 30.00 # 5.00 # 4.00 # 4.00 # 40.00 # 6.00 # 5.00 # .00 # .00 # 7.00 # 6.00 # .00 # .00 # 8.00 # 7.00 # .00 # .00 # 9.00 # 8.00 # .00 # .00 # 10.00 # 9.00 # .00 # .00 #	HISTOGRAM PRINTOUT
After 'HISTOGRAM PRINTOUT' is complete, skip STEP 20 if a plotter in not installed.			
20.			
The plot should be identical to the 'FIRST PLOT' shown in Figure 6-6.			

Two Variable Checkout Procedure

This procedure should be performed exactly the same as the single variable procedure. If a plotter is not installed, perform steps 1 and 2, then skip to step 11.

STEP:	PRESS:	PRINTOUT:	COMMENTS:
	CLEAR	CLEAR	
1.	RHO ( ) 2	V2 •••••••	This portion of the procedure requires that a Plotter be installed.
		.00 →	
2.	VAR # 2		
		RG1 =	
3.	0 STORE	.00 #	
		6.00 #	
4.	6 AXES 1		
5.	6 AXES 2	RG2 =	
		.00 #	
		6.00 #	
6.	1 STORE	1.00 →	
7.	1 AXES 3	T I =	
		1.00 #	
		1.00 #	
8.	0 STORE	.00 →	
9.	AXES 4	A I =	Second x and y axes should be plotted over previous axes. New tic marks will be plotted.
		.00 #	
		.00 #	

STEP:	PRESS:	PRINTOUT:	COMMENTS:
10.	CHAR # 2	CT2	
	NOTE: If a plotter is not installed, begin procedure here.	1.00 #	If plotter is not installed, begin proced here.
		1.00 #	2nd 'DATA ENTRY' cause a ◇ charac to be plotted at a specified point i plotter is installed.
11.	1 DATA ENTRY	5.00 #	
		2.00 #	
12.	DATA ENTRY	A =	LINEAR REGRESSION PRINTOUT
13.	5 DATA ENTRY	.75 #	
14.	DATA ENTRY	B =	
		.25 #	
15.	LINEAR	r^2 =	
		1.00 #	
		LE	For any given x(3.5) gives the value o
16.	3 . 5 ŷ EVAL	3.50 #	
		1.63 #	
17.	PLOT		Pressing 'PLOT' causes the linear regr sion to be plotted as shown by 'SECOI PLOT' in Figure 6-6.
18.	CHAR # 3	CT3	
19.	DELETE	D E L	
20.	5 DATA ENTRY	5.00 #	
		5.00 #	The character X plotted before this pri out occurs.
21.	5 DATA ENTRY	4.00 #	
22.	4 DATA ENTRY	2.00 #	The character ⊡ plotted.
23.	2 DATA ENTRY	5.00 #	
		1.00 #	
24.	5 DATA ENTRY	A =	PARABOLIC PRINTOUT
25.	1 DATA ENTRY	* - 3.67 #	
26.	PARA	B =	
		5.75 #	
		C =	
		* - 1.08 #	
		r^2 =	
27.	PLOT	* - .57 #	Parabolic curve plotted as shown THIRD PLOT in Figure 6-6.

* Printout is red

Paired Statistics Checkout Procedure

A plotter is not required to perform any of this procedure.

STEP:	PRESS:	PRINTOUT:	COMMENTS:
	CLEAR	CLEAR	
1.	VAR # 0	2T	
2.	1 DATA ENTRY	DATA 1 1.00 #	
3.	2 DATA ENTRY	2.00 #	
4.	3 DATA ENTRY	3.00 #	
5.	CHANGE SAMPLE	DATA 2 5.00 #	
6.	5 DATA ENTRY	4.00 #	
7.	4 DATA ENTRY	3.00 #	
8.	3 DATA ENTRY	N1 = 3.00 #	
9.	BASIC STAT	$\bar{x}$ = 2.00 #	
		$\Delta 1$ = 1.00 #	BASIC STATISTICS printout.
		N2 = 3.00 #	
		$\bar{y}$ = 4.00 #	
		$\Delta 2$ = 1.00 #	
10.	t	T = * - 2.45 #	Paired t printout
		D = 4.00 #	

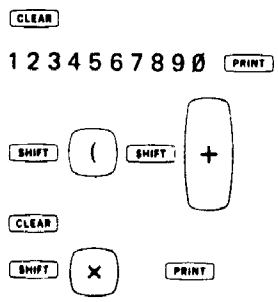
* Printout is red

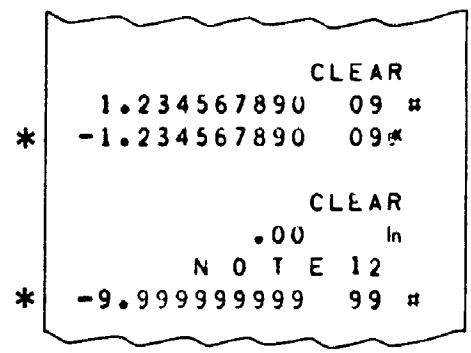
DISPLAY AND PRINTER CHECKOUT PROCEDURE

> **NOTE**
>
> This procedure only checks the printer and not the printer drive circuits on the mother board. If a printer fails this test, the customer and kit printers should be exchanged to determine if the printer or the mother board is defective.

1. Check printer operation by pressing the following keys – in order – and verifying that the resulting printou identical to the one shown below:

   (The [AUTO·] and [PRT OFF] keys must be up.)





* Printout is red

2. If the resulting printout is identical to the above printout, the printer and printer drive circuits are opera correctly. Otherwise, exchange the printer with the kit printer to isolate the defective assembly (see the at NOTE).
3. While performing the tests described in step 1, verify that the segments in the display are operating correctly.

Table 6-9. System Test PROM Symptoms

SYMPTOM	CHECK	PROBABLE CAUSE	ADDITIONAL INFORMATION
Exerciser 10 fails:	1. Remove all peripherals, I/O cards, and optional data storage.	Not in basic machine.	Problem may be caused by an optional assembly
	2. If problem still exists exchange (A40) father or (A41) display board.	A40 or A41 failure.	
	3. Exchange the printer.	Printer failure.	Since the printer is used to output the results of the test, the printer may be the source of the problem.
	4. Replace the mother board.	Mother board failure.	
Exerciser 20 fails:	1. Exchange any installed Data Storage Resisters.	Failure on the optional data storage assemblies.	
Exerciser 30 fails:	1. Exchange the Printer.	Printer failure.	
	2. Exchange the (A40) or (A41) board.		
	3. Replace the mother board.	Mother board failure.	Since Exerciser 10 runs properly, 2 and 3 are not probable failures.
Exerciser 40 fails:	1. Exchange the plotter I/O card.	I/O card failure.	
	2. Check I/O cable and plotter.		11390A Service Kit may be used with customer I/O cable to check the I/O cable and plotter.

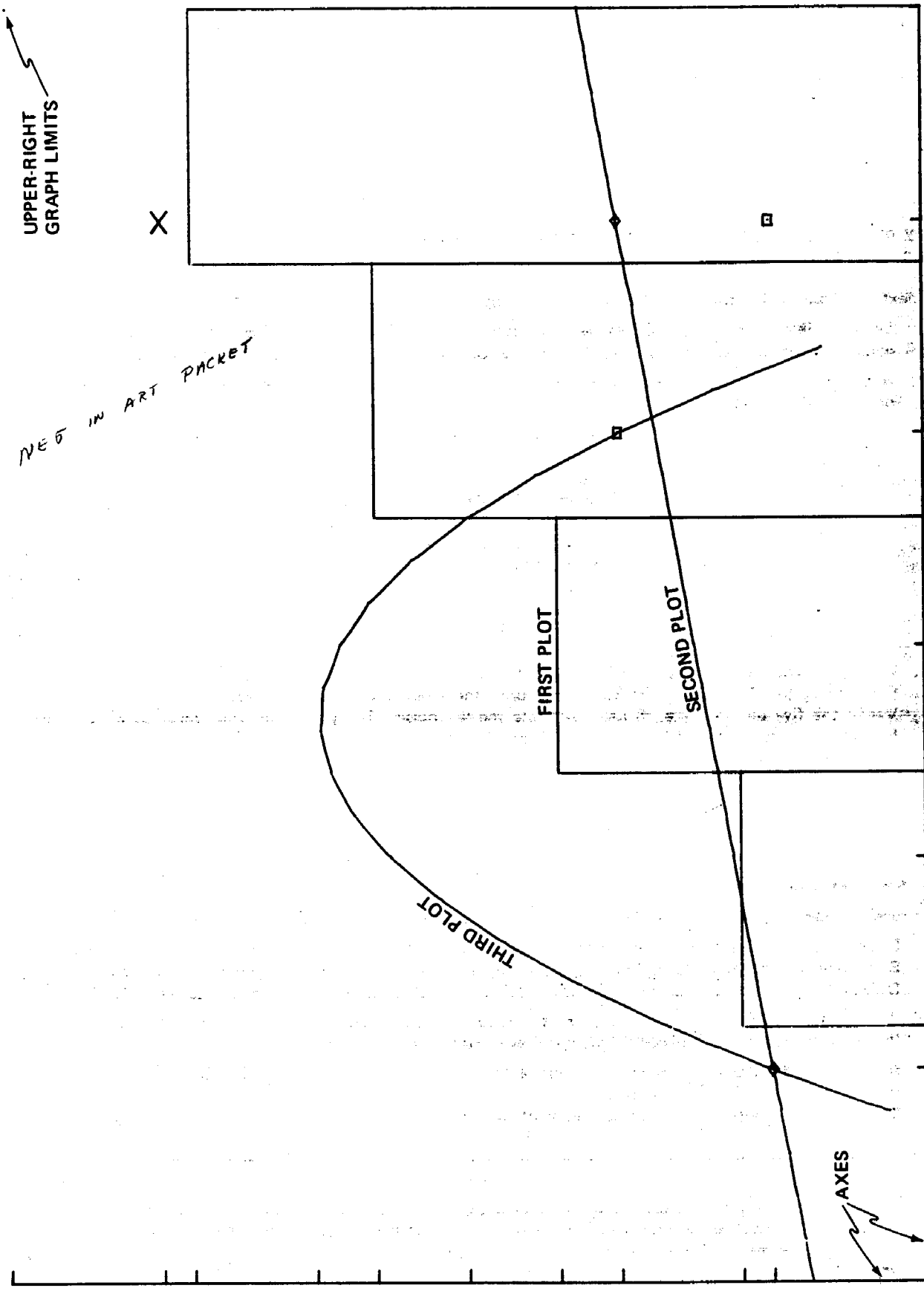


Figure 6-6. Results from STAT Keyblock Checkout Procedure

OSCILLOSCOPE TEST PROCEDURE

Preliminary Tests

Before performing the oscilloscope test procedure, verify that the calculator power supplies are within the specifica given below; a 3469B, or its equivalent, should be used to make these measurements.

Power Supply	Specification
+6V	+5.5V to +6.5V
+15V	+1.4V to +16.5V
-12V	-11V to -13V

If any of the power supplies are not within the specified operating limits, it must be repaired before performing fu tests on the calculator.

The next test ensures that the clock circuits are operating correctly. To perform the test:

1. Set the TIM/DIV and VOLTS/DIV vernier controls to the CAL position. Then, calibrate both 10004A (or equivalent) input probes and the 180C display as described in the associated operating manuals.
2. Next, set the controls on the vertical amplifier and time base units as follows (settings which are not specifie not affect the set-up):

A and B input switches:	DC
A and B VOLTS/DIV:	.5
DISPLAY:	A
A and B POLARITY:	+UP
TIME/DIV:	1μsec
SWEEP MODE:	AUTO
trigger source:	INT
SLOPE:	–
trigger coupling:	ACF
MAGNIFIER:	X1

3. With the calculator switched OFF, connect the channel A input to U12 pin 2 (Φ1). Switch the calculator then adjust the TRIGGER LEVEL control until the scope triggers on the negative-going edge of the Φ1 si Verify the five divisions (i.e., 5 μsec) separate the Φ1 pulses. The pulse amplitude must be at least -9V to Repeat this test on the Φ2 signal at U12 pin 3. Correct any clock circuit failures before proceeding with 'Scope Set-up Procedure' (see Figure 6-3).

Scope Set-up Procedure

This procedure describes the scope settings necessary to adjust your scope to display one 14-digit word of the calcul

1. Switch the calculator OFF. Connect the channel B probe to U12 pin 8 (START) and the channel A probe tc SYNC jumper on the mother board. Make the same scope settings as previously described, except set DISPLAY switch to ALT (B sync) and the TIME/DIV to 20 μsec. Switch the calculator ON.
2. Adjust the TRIGGER LEVEL control so the scope triggers at the beginning of the positive-going START s (bit 0). Adjust the A and B POSITION controls so both signals can be seen.
3. Adjust the HORIZONTAL POSITION control to align the leading edge of the START signal with the left edg the grid. Next, adjust the TIME/DIV VERNIER control until the leading (position-going) edge of the se START signal is aligned with the right edge of the grid.

> **NOTE**
>
> If you align the leading of the SYNC signal with the last grid division (1 cm from the right edge), then the display is bits 0 through 50; each minor division is one bit-time.

Testing the Calculator

> **NOTE**
>
> The preceding tests must have been satisfactorily completed before this procedure is performed.

Figure 6-8 is a troubleshooting tree. To use the tree, switch the calculator in question OFF. Press the DECIMAL switch (Model 81 only) down and ensure that the PRINT OFF key is up. If your calculator does not contain the display option, replace the father board (A4) with a display board (A5). If you are repairing a Option 002 Model 81, replace the father board with *an OPT 001* display board. If a Opt 003 Model 81 is being tested, connect the keyboard cable to the mother board rather than the display board.

Now, switch the calculator ON and note the display and printout. Then proceed with the portion of the troubleshooting tree that most nearly approximates the failure indicated by your calculator. Figure 6-7 shows the 'GROUP I' signals; Table 6-10 explains the 'GROUP II' signals.

When repairs have been completed, perform the key test sequence, for the calculator just repaired, provided earlier in this chapter.

Table 6-10. The GROUP II Signals

Signal	Description for Testing
FLG'	To U13 pin 5; signal is usually +5V — low when the PRINT OFF key is pressed and a printing routine is begun.
FLG	To U13 pin 9; should duplicate the FLG' signal.
CARRY	From U11 pin 6; normally 0V — (approx.) 1 positive pulse each digit when CLEAR is pressed.
IOC1	From U13 pin 20; normally 0V — goes high when nearly any key is pressed.
IOC2	From U13 pin 19; normally 0V - goes high at turn-on.
IOC3	From U13 pin 18; normally +6V — goes low when most keys are pressed.
SCE	From U13 pin 17; normally 0V — goes high when most keys are pressed.
EIS1	From U13 pin 15; normally +6V — goes low when most keys are pressed.
EXT	From U13 pin 3; normally +6V — negative pulse for 1 bit-time when a key is pressed.
PWO	To U13 pin 10 (and other MOS circuits); PWO is always +6V except for 500 msec after the ON/OFF switch is pressed.

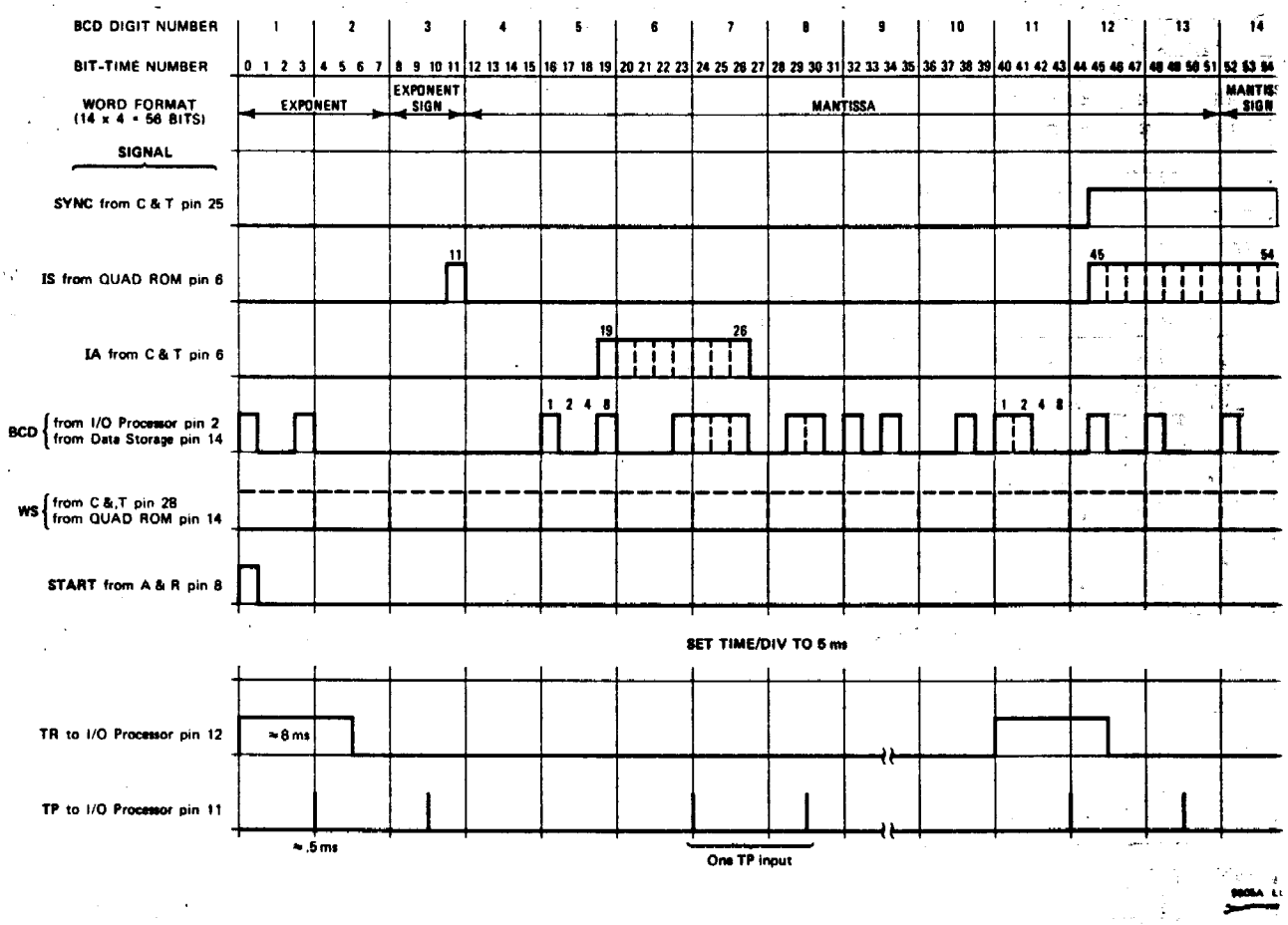
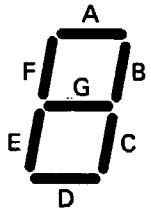


Figure 6-7. The Group I Signals

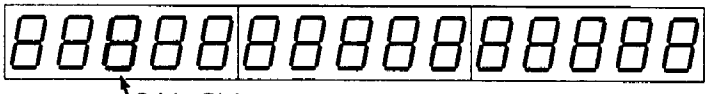
DISPLAY PROBLEMS

Make up of segment.



ART 7 NEO IN ART PACKET

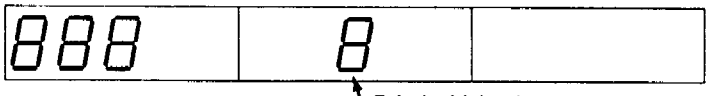
1. Bright digits on display.
   a. Anode driver



2. Digit has a tendency to turn on next digit. A ghost image appears.

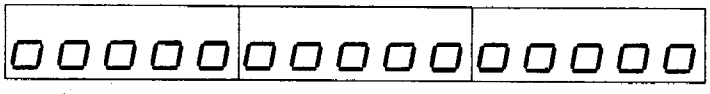
> **NOTE**
>
> If 'G' segment is faintly lighted, it is often caused by the A&R. To correct this problem, change the A&R.

   a. Cathode driver

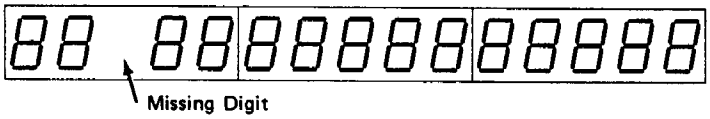


3. Digits missing segments of numbers.
   a. LED

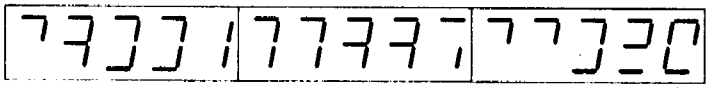
4. All digits missing same segments.
   a. Inductor shorted
   b. Anode driver



5. Single digit missing out of display.
   a. Cathode driver
   b. LED



6. Shorted segment of digit.
   a. LED
   b. Anode driver



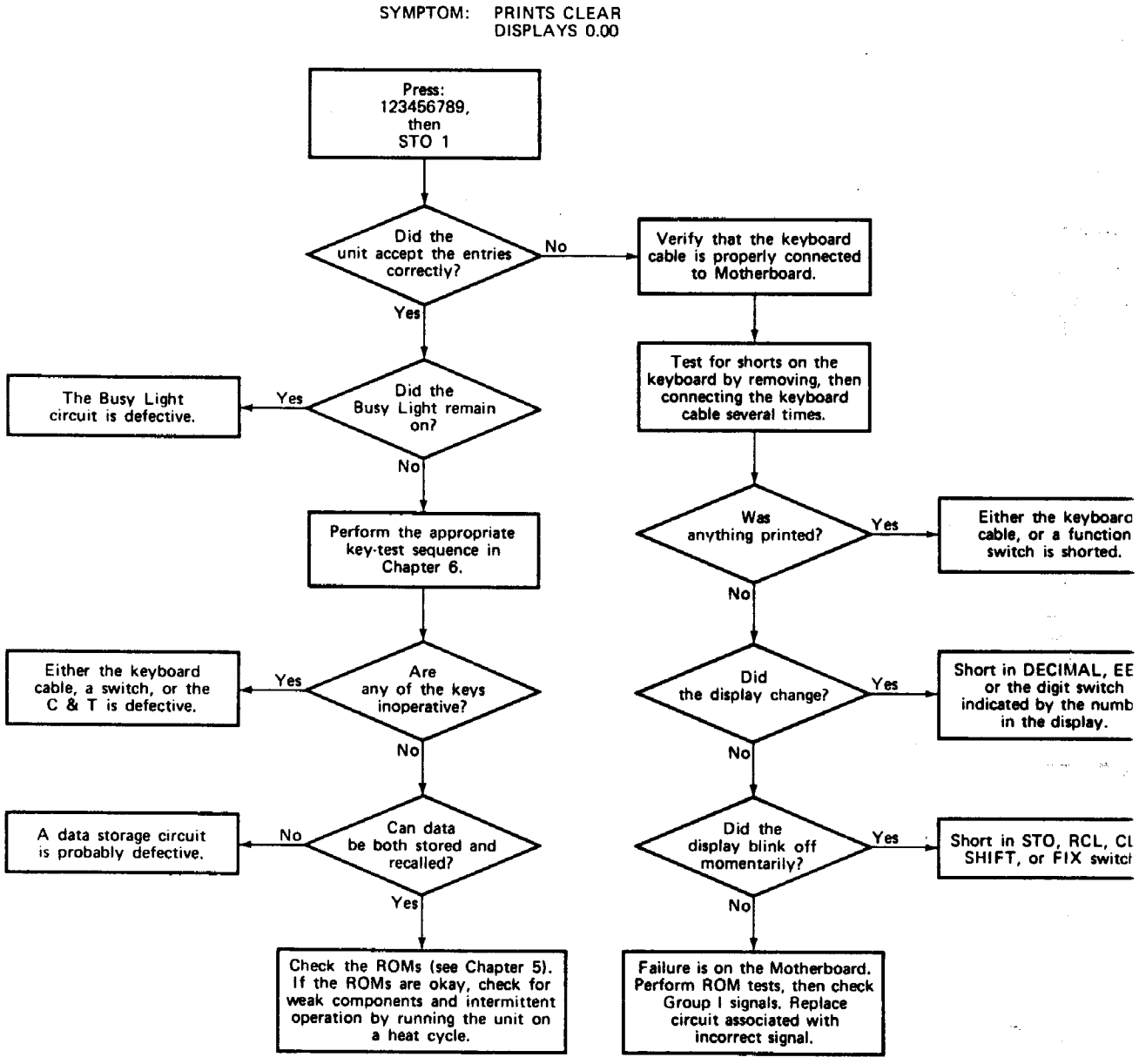
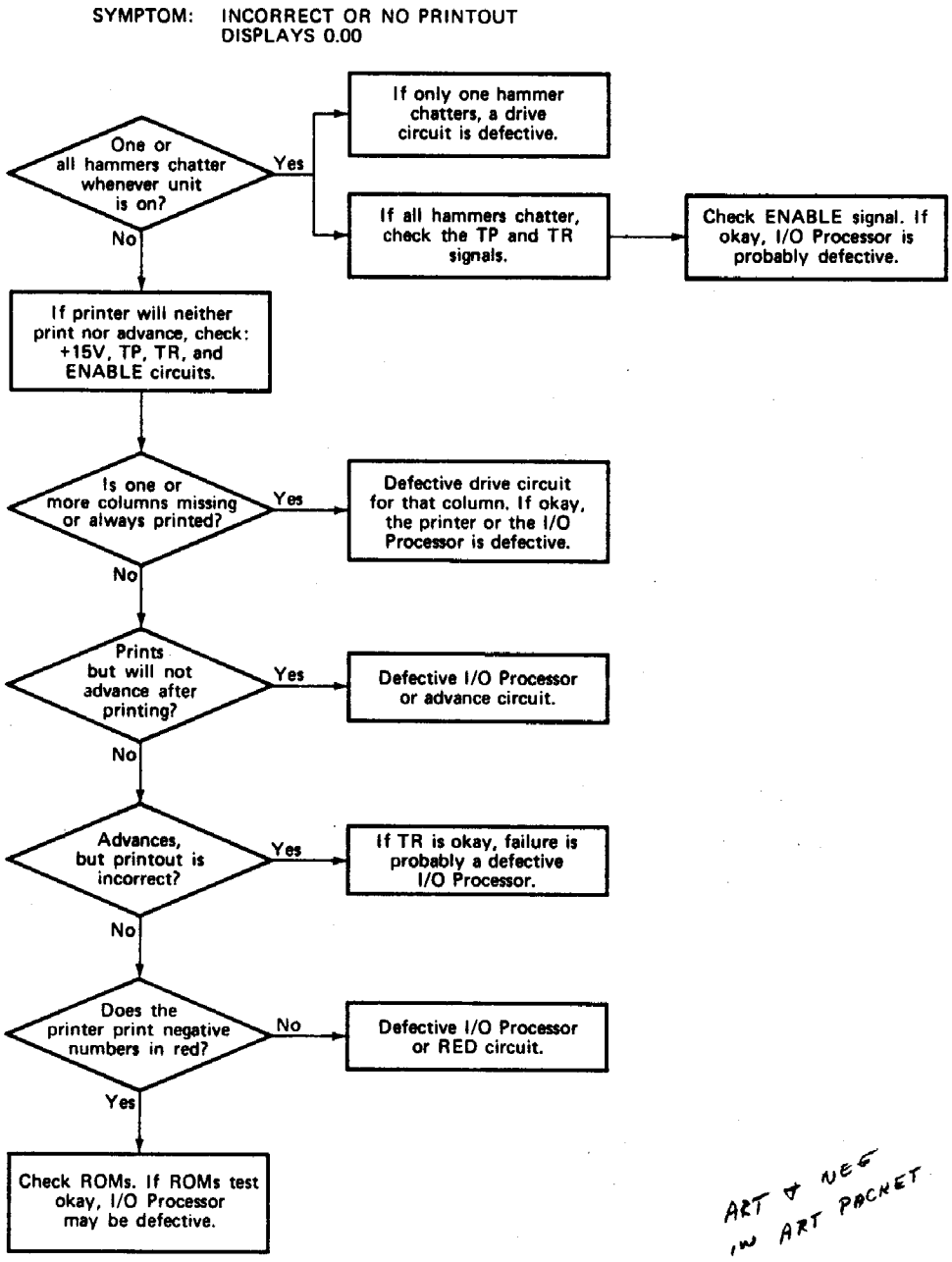
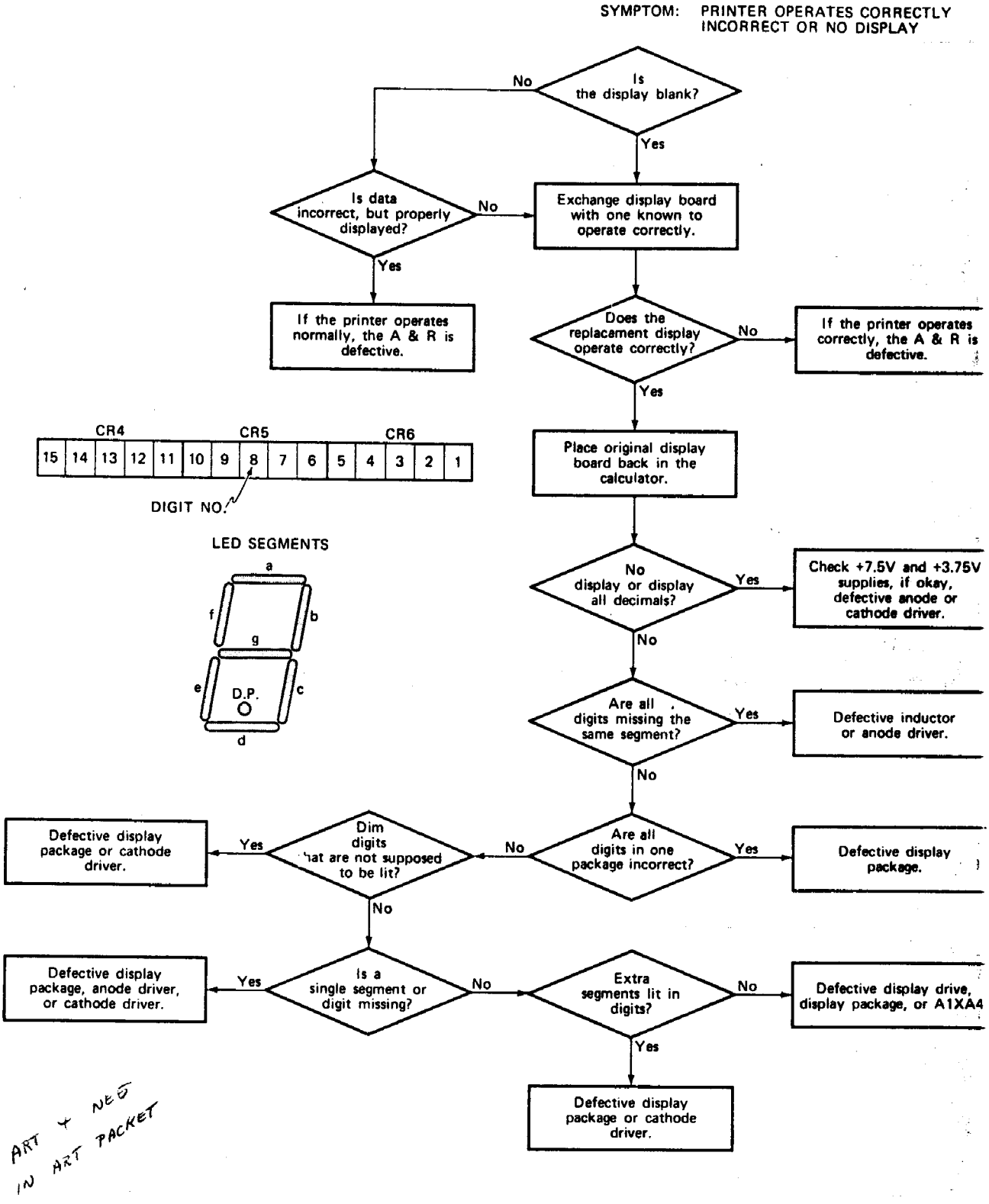


Figure 6-8. Troubleshooting Tree



ART # NEG
IN ART PACKET

Figure 6-8. Troubleshooting Tree (Cont'd)



ART + NEG IN ART PACKET

Figure 6-8. Troubleshooting Tree (Cont'd)

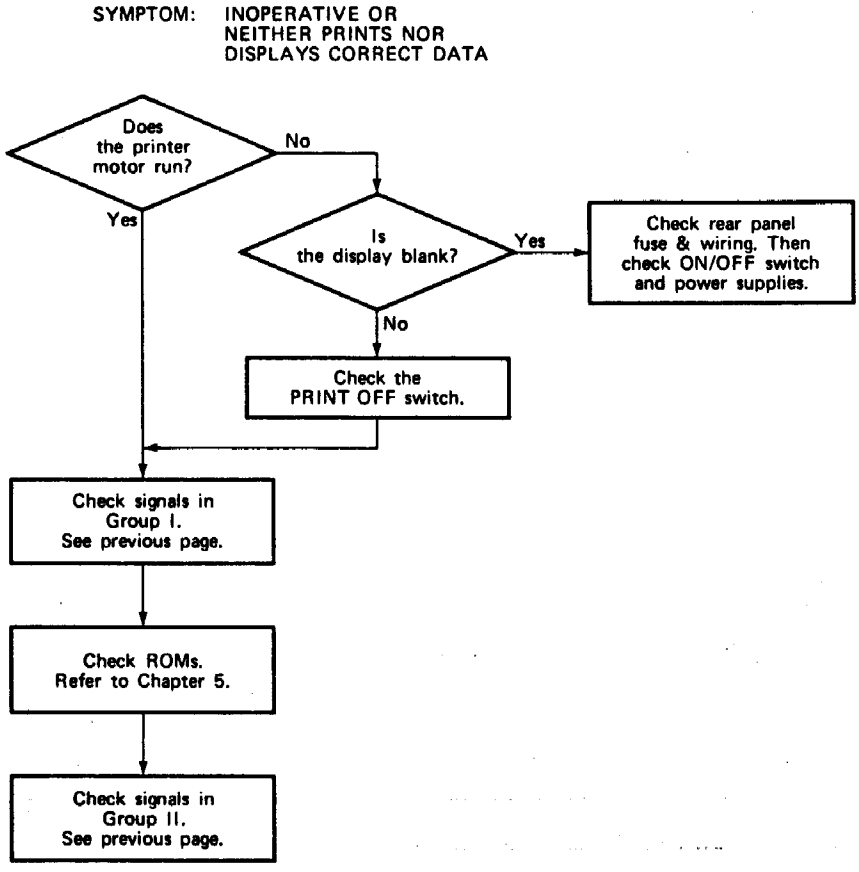


Figure 6-8. Troubleshooting Tree (Cont'd)

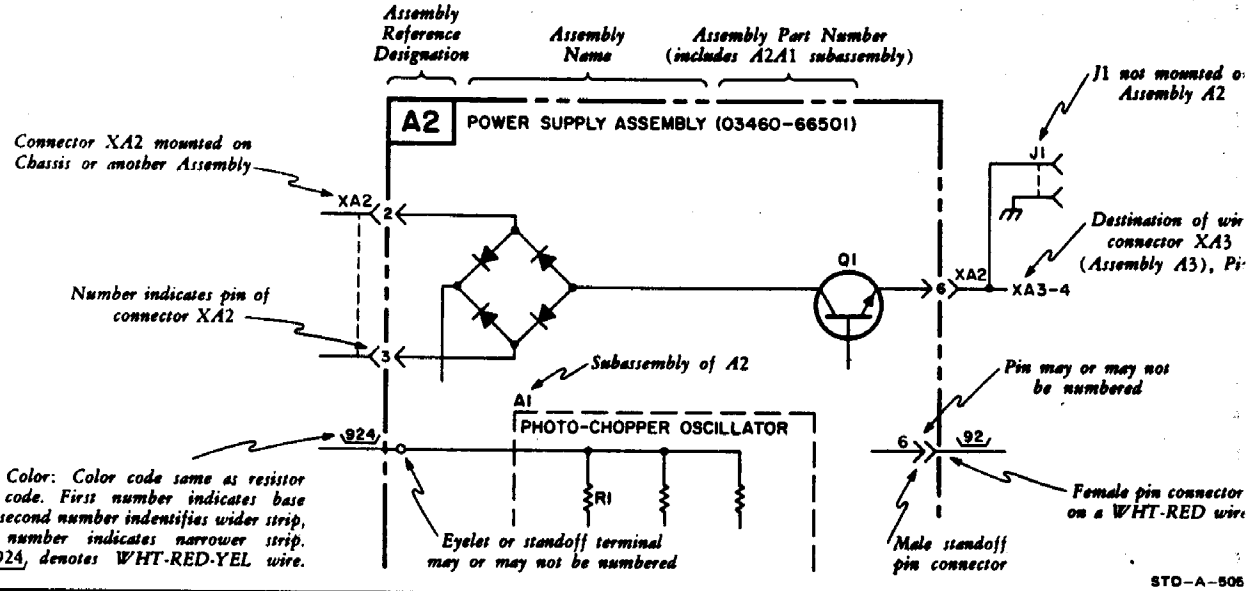
ART # NEG IN ART PACKET

SCHEMATIC NOTES

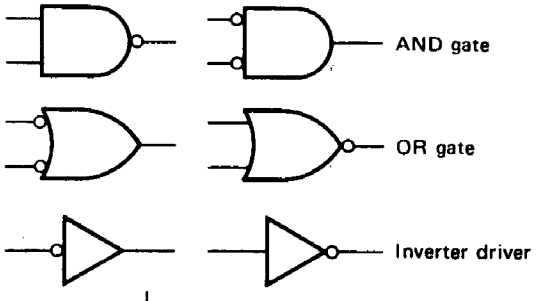
REFERENCE DESIGNATIONS

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH ASSEMBLY OR SUBASSEMBLY DESIGNATION(S) OR BOTH FOR COMPLETE DESIGNATION.

ASSEMBLY	SUBASSEMBLY	COMPONENT	COMPLETE DESIGNATION
A2	NONE	Q1	A2Q1
A2	A1	R1	A2A1R1
NONE	NONE	J1	J1



1. COMPONENT VALUES ARE SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED.
   RESISTANCE IN OHMS, CAPACITANCE IN MICROFARADS, INDUCTANCE IN MICROHENRIES
2. GROUNDS: ⏚ CIRCUIT ▬ CHASSIS ⏚ EARTH
3. ——— - - - ——— DENOTES ASSEMBLY
4. LOGIC SYMBOLS:



Small circle means "low-true" at this input or output.

Input information is transferred to the outputs on the positive edge of the clock pulse. Low inputs to PRESET forces Q high, whereas low inputs to CLR forces Q low; both inputs are independent of CLOCK.

CMOS LATCH (Models 46 & 81): +6V on EN enables the output to follow the input; 0V on EN forces out low.

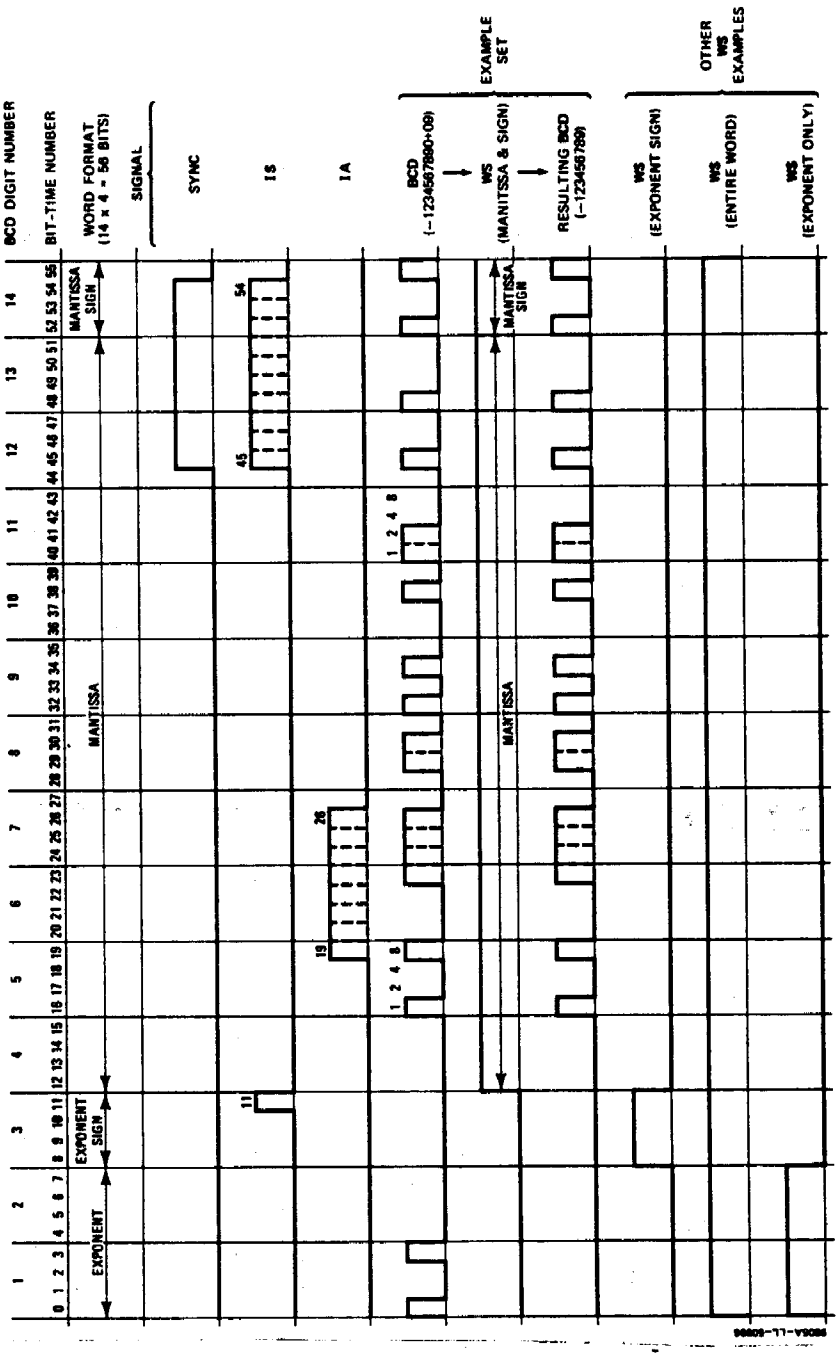


Figure 6-9. System Signals

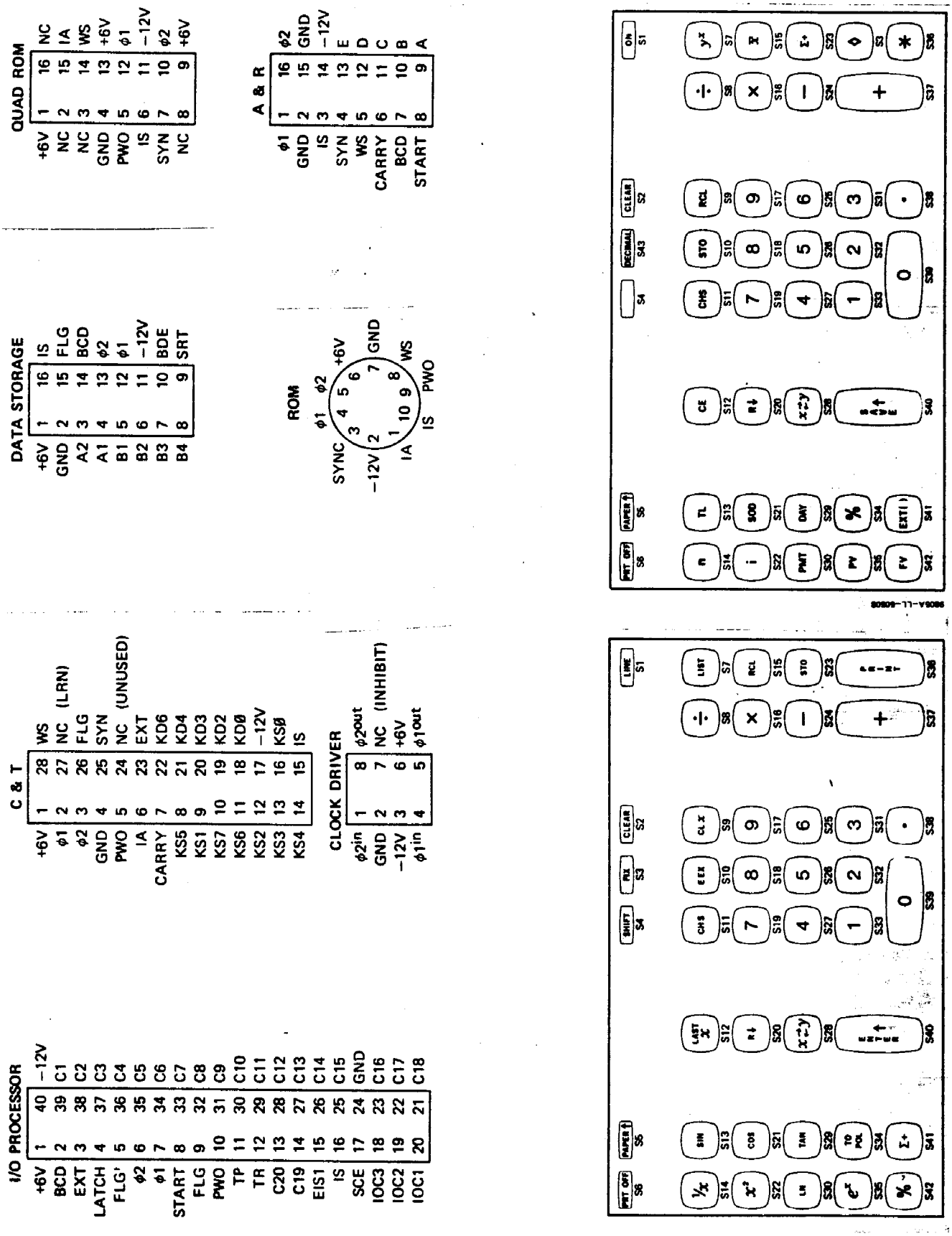
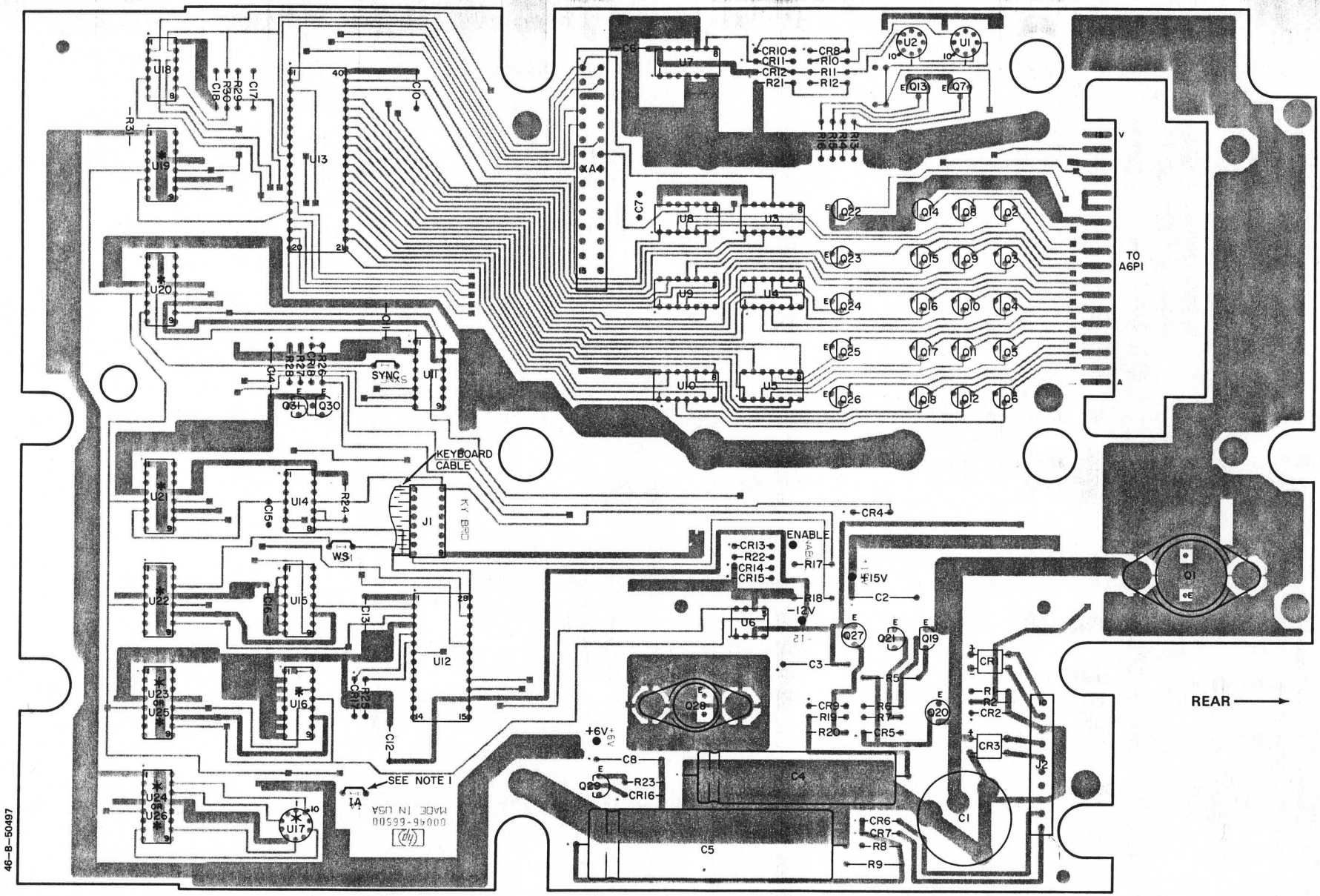


Figure 6-10. Models 46 & 81 Key Reference Designations



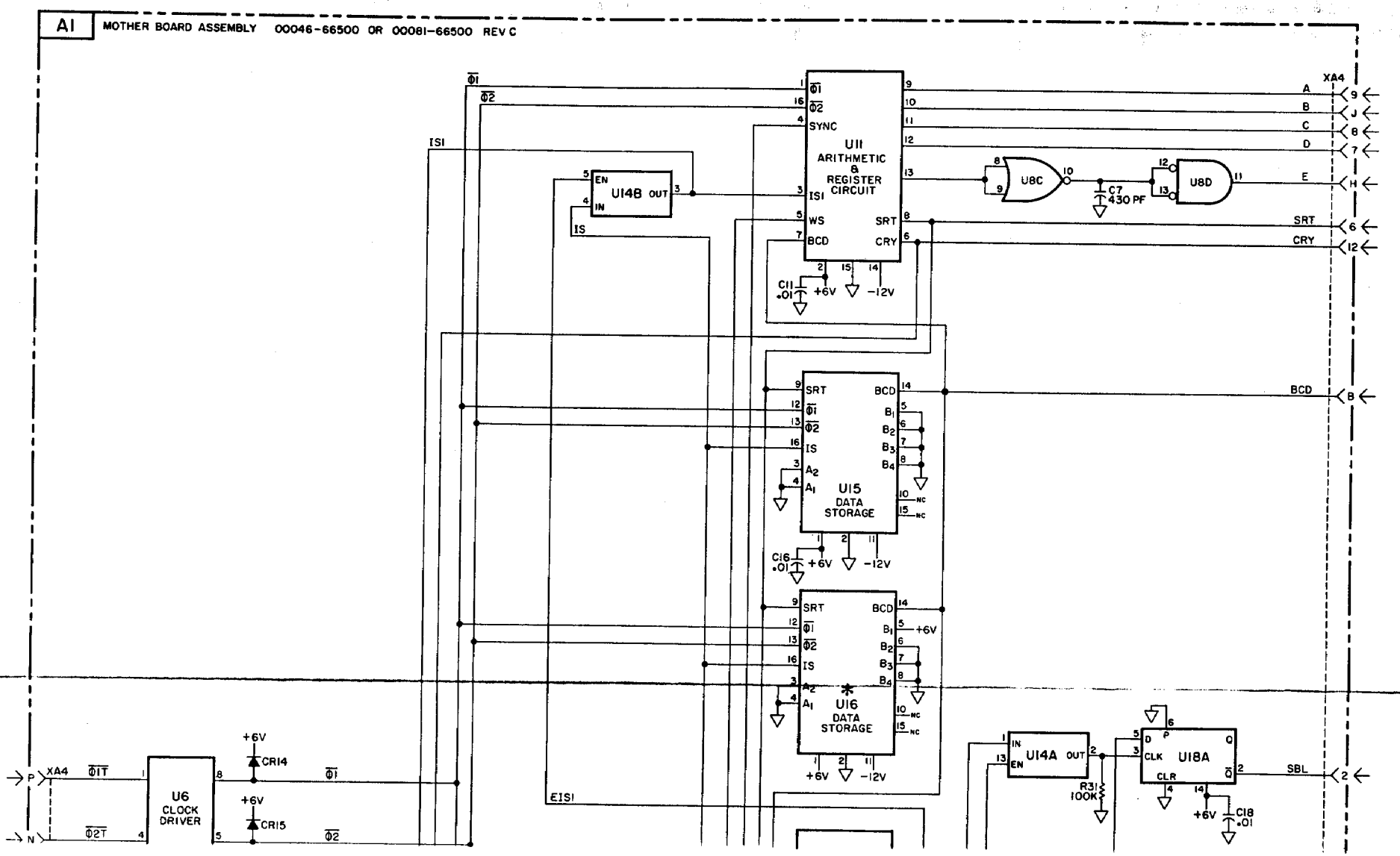
COMPONENT SIDE

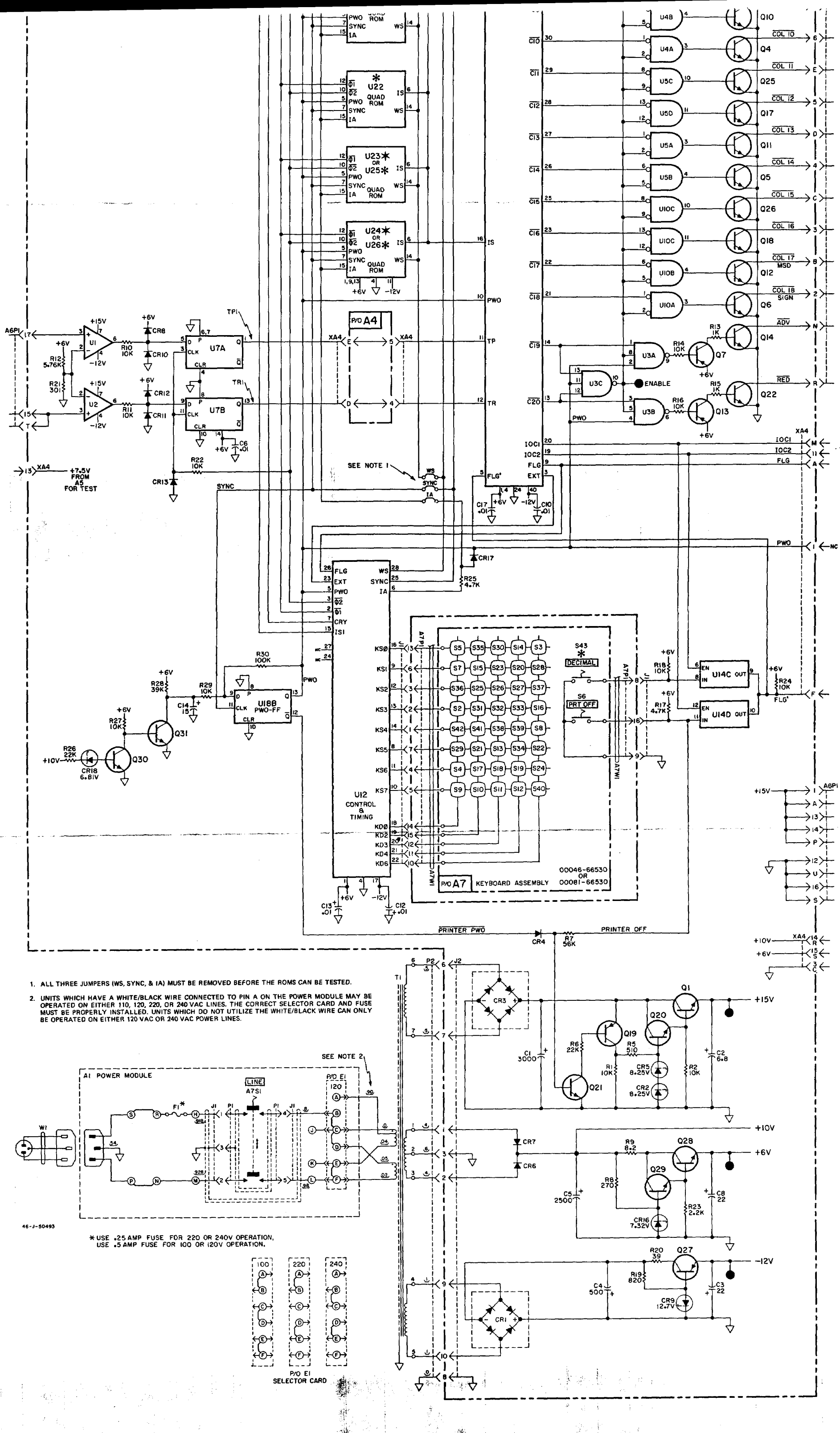
A1

-hp- Part No. 00046–66500 Rev C or 00081–66530 Rev C

NOTES

1. ALL THREE JUMPERS (WS, SYNC, & IA) MUST BE REMOVED BEFORE ANY ROMS CAN BE TESTED.
2. ✱ DENOTES COMPONENT ON MODEL 46 ONLY,
   ✱ DENOTES COMPONENT ON MODEL 81 ONLY.


A1
MOTHER BOARD ASSEMBLY 00046-66500 OR 00081-66500 REV C
U11
ARITHMETIC & REGISTER CIRCUIT
SYNC
ISI
WS
BCD
SRT
CRY
U14B
OUT
IN
EN
C11 .01
+6V
-12V
U8C
U8D
C7 430 PF
XA4
A
B
C
D
E
SRT
CRY
BCD
U15
DATA STORAGE
C16 .01
U16
DATA STORAGE
NC
U14A
R31 100K
U18A
CLK
CLR
SBL
C18 .01
U6
CLOCK DRIVER
CR14
CR15
EISI

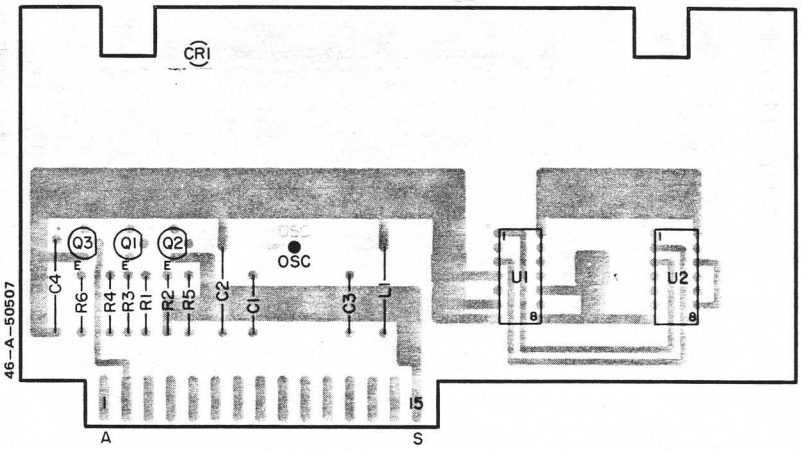


1. ALL THREE JUMPERS (WS, SYNC, & IA) MUST BE REMOVED BEFORE THE ROMS CAN BE TESTED.
2. UNITS WHICH HAVE A WHITE/BLACK WIRE CONNECTED TO PIN A ON THE POWER MODULE MAY BE OPERATED ON EITHER 110, 120, 220, OR 240 VAC LINES. THE CORRECT SELECTOR CARD AND FUSE MUST BE PROPERLY INSTALLED. UNITS WHICH DO NOT UTILIZE THE WHITE/BLACK WIRE CAN ONLY BE OPERATED ON EITHER 120 VAC OR 240 VAC POWER LINES.

46-J-50493

* USE .25 AMP FUSE FOR 220 OR 240V OPERATION, USE .5 AMP FUSE FOR 100 OR 120V OPERATION.

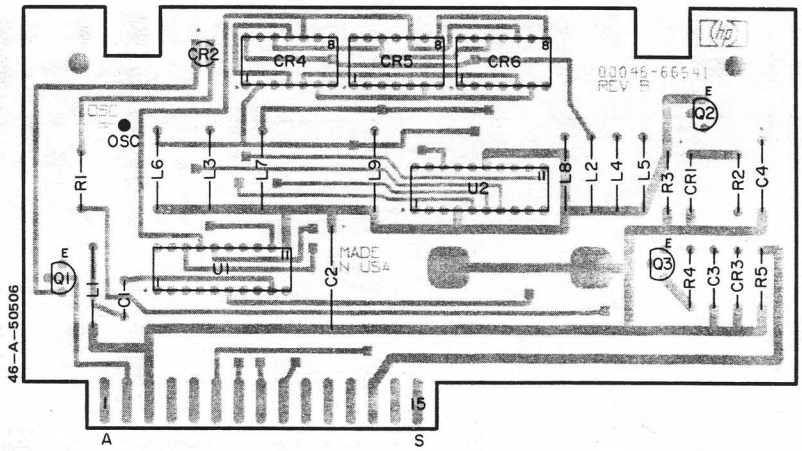
Figure 6-11. Models 46 & 81 Motherboard (A1) Schematic



COMPONENT SIDE

A4

-hp- Part No. 00046–66540 Rev B



COMPONENT SIDE

A5

-hp- Part No. 00046–66541 Rev B

6-47/48

ANODE DRIVER

c	1	20	SG*
b	2	19	SE*
a	3	18	SDP*
d	4	17	SF*
e	5	16	SD*
SHIFT-CLK	6	15	GND
ϕ1	7	14	SB*
ϕ2	8	13	SC*
CAP	9	12	SA*
(TRIM) NC	10	11	+4V

*SEGMENT ENABLE SIGNALS

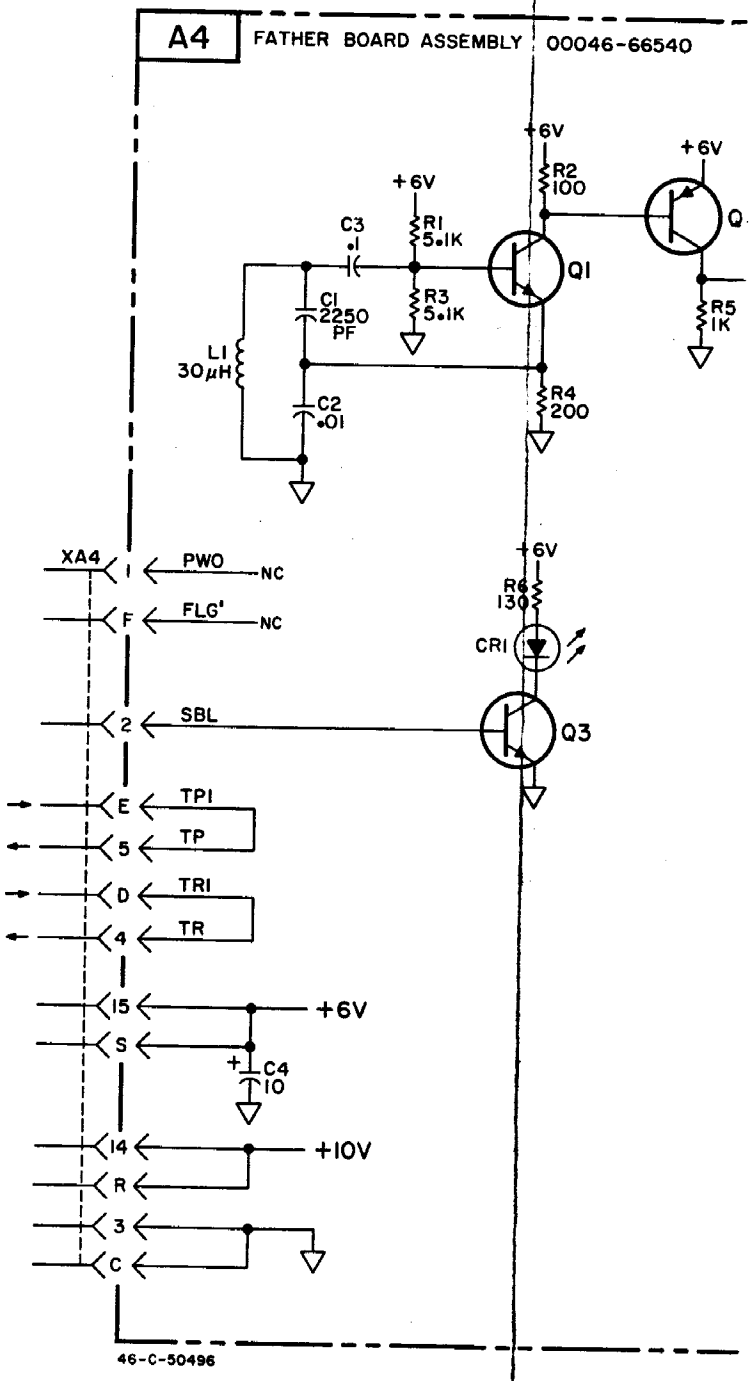
CATHODE DRIVER

9*	1	20	8*
10*	2	19	7*
11*	3	18	6*
+4V	4	17	5*
12*	5	16	4*
13*	6	15	+4V
14*	7	14	3*
START	8	13	2*
CLK	9	12	1*
+7.5V	10	11	15*

*DIGIT ENABLE SIGNALS

LED

DIGIT 5 SELECT	1	14	A
E	2	13	DIGIT 4 SELECT
C	3	12	B
DIGIT 3 SELECT	4	11	DIGIT 3 SELECT
DP	5	10	F
D	6	9	DIGIT 2 SELECT
DIGIT 1 SELECT	7	8	G



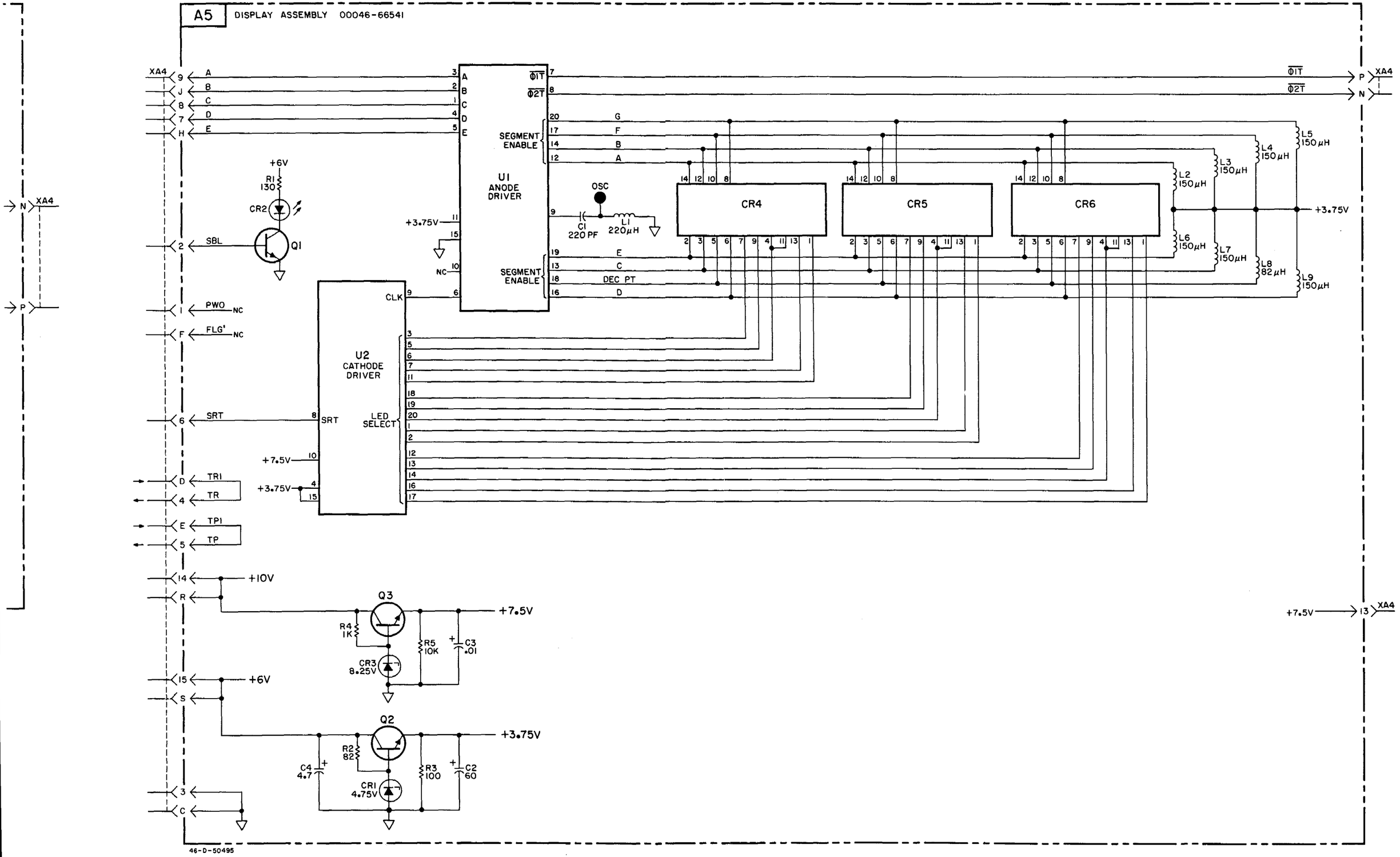
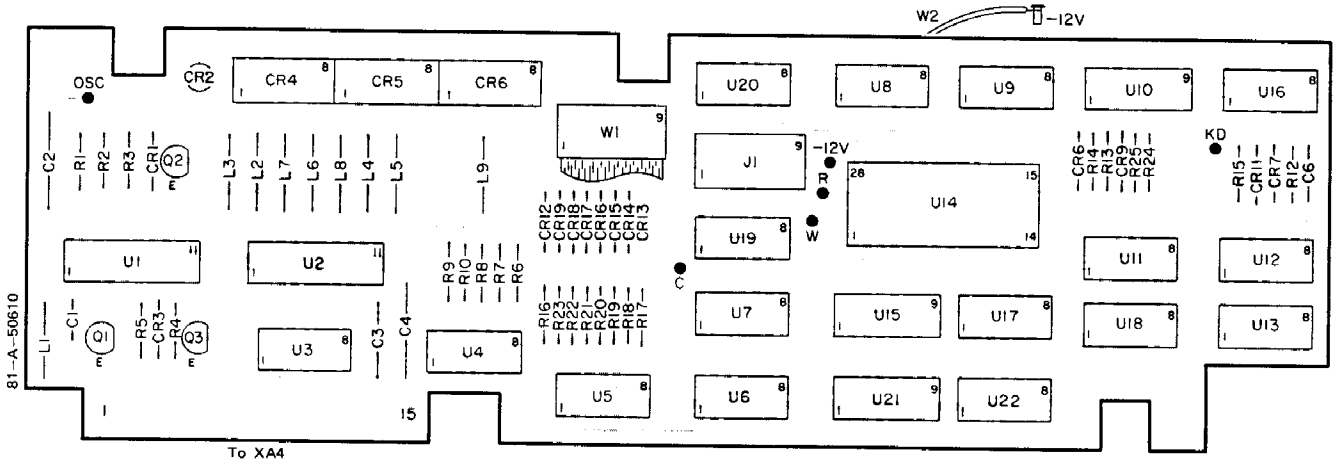


Figure 6-12. Models 46 & 81 Display (A5) & Fatherboard (A4) Schematics



COMPONENT SIDE

A43

-hp- Part No. 00081-66543 Rev A

ANODE DRIVER

c	1	20	SG*
b	2	19	SE*
a	3	18	SDP*
d	4	17	SF*
e	5	16	SD*
SHIFT-CLK	6	15	GND
ϕ1	7	14	SB*
ϕ2	8	13	SC*
CAP	9	12	SA*
(TRIM) NC	10	11	+4V

*SEGMENT ENABLE SIGNALS

CATHODE DRIVER

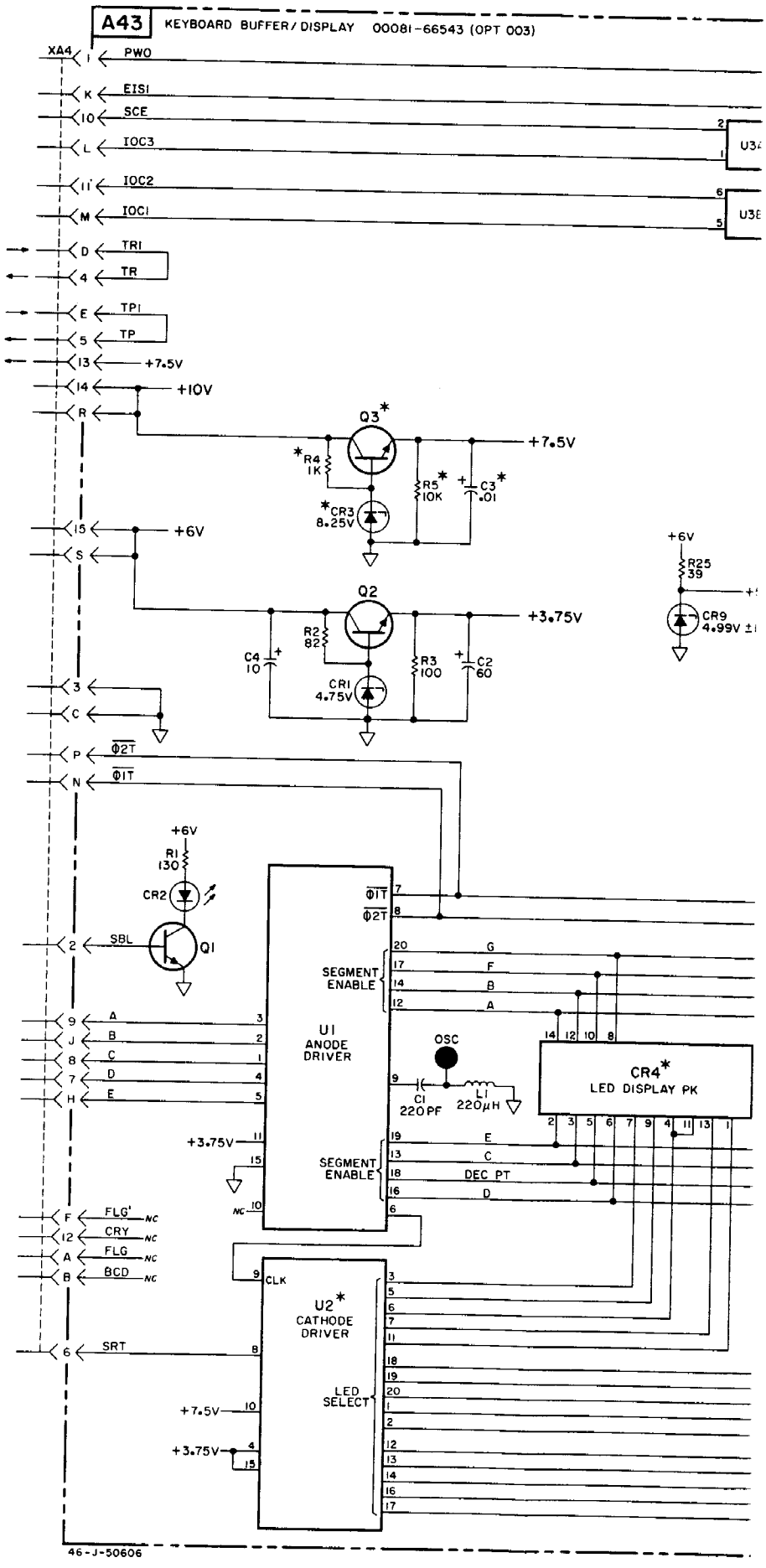
9*	1	20	8*
10*	2	19	7*
11*	3	18	6*
+4V	4	17	5*
12*	5	16	4*
13*	6	15	+4V
14*	7	14	3*
START	8	13	2*
CLK	9	12	1*
+7.5V	10	11	15*

*DIGIT ENABLE SIGNALS

LED

DIGIT 5 SELECT	1	14	A
E	2	13	DIGIT 4 SELECT
C	3	12	B
DIGIT 3 SELECT	4	11	DIGIT 3 SELECT
DP	5	10	F
D	6	9	DIGIT 2 SELECT
DIGIT 1 SELECT	7	8	G

6-49/50


A43 KEYBOARD BUFFER/DISPLAY 00081-66543 (OPT 003)
XA4
PWO
EISI
SCE
IOC3
IOC2
IOC1
TRI
TR
TPI
TP
+7.5V
+10V
+6V
+3.75V
Q3*
R4 1K
R5 10K
C3 .01
CR3 8.25V
Q2
R2 82
R3 100
C2 60
C4 10
CR1 4.75V
R25 39
CR9 4.99V
ΦIT
Φ2T
R1 130
CR2
Q1
SBL
U1 ANODE DRIVER
SEGMENT ENABLE
OSC
C1 220PF
L1 220μH
CR4* LED DISPLAY PK
U2* CATHODE DRIVER
LED SELECT
FLG'
CRY
FLG
BCD
SRT
CLK
46-J-50606

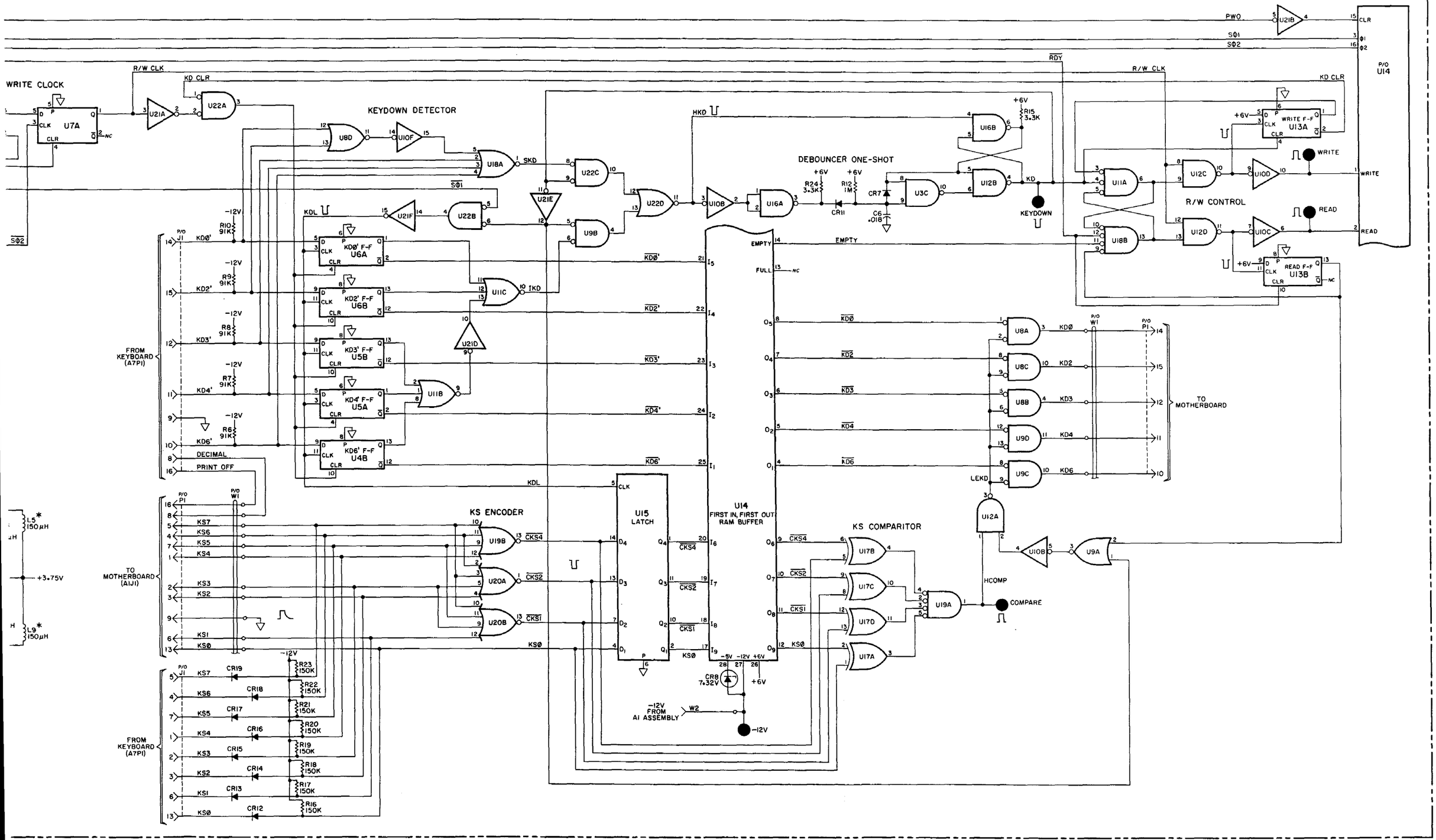
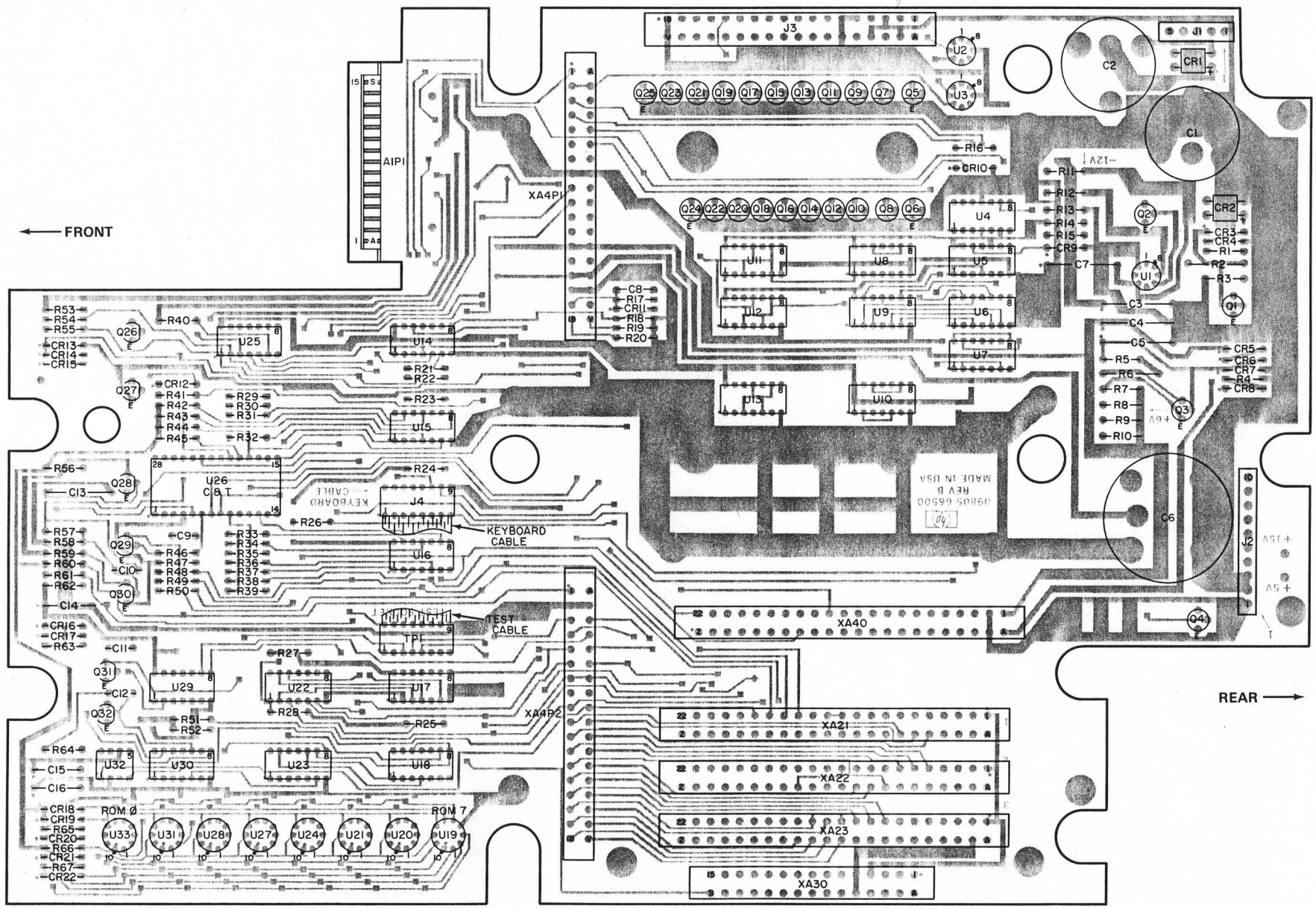


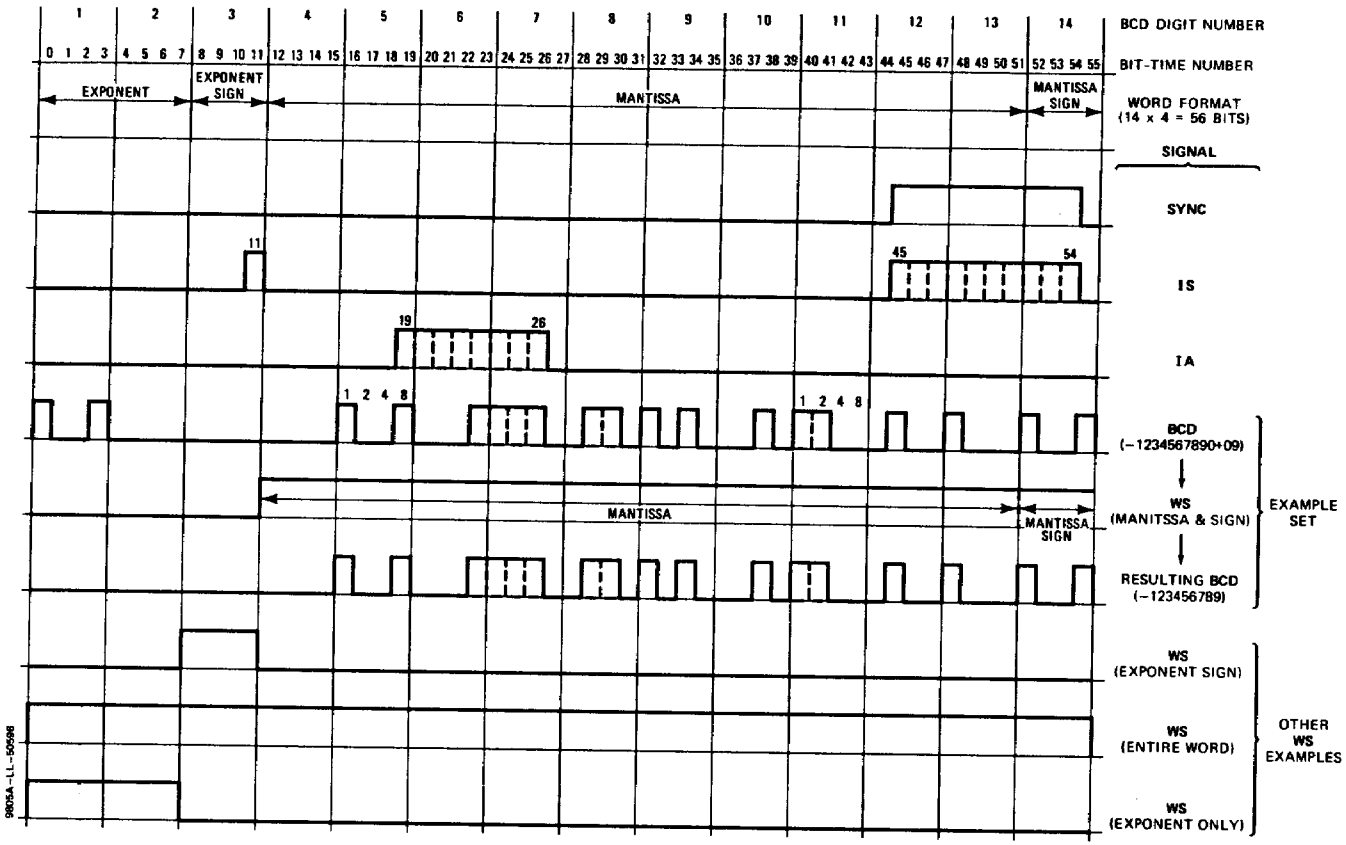
Figure 6-13. Model 81 Keyboard Buffer (A42 & A43) Schematic



COMPONENT SIDE

A1

-hp- Part No. 09805–66500 Rev B



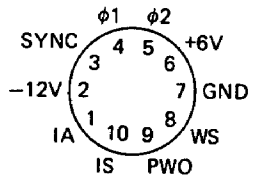
CLOCK DRIVER

$\phi 2^{in}$	1	8	$\phi 2^{out}$
GND	2	7	NC (INHIBIT)
−12V	3	6	+6V
$\phi 1^{in}$	4	5	$\phi 1^{out}$

C & T

+6V	1	28	WS
$\phi 1$	2	27	NC (LRN)
$\phi 2$	3	26	FLG
GND	4	25	SYN
PWO	5	24	NC (UNUSED)
IA	6	23	EXT
CARRY	7	22	KD6
KS5	8	21	KD4
KS1	9	20	KD3
KS7	10	19	KD2
KS6	11	18	KDØ
KS2	12	17	−12V
KS3	13	16	KSØ
KS4	14	15	IS

ROM



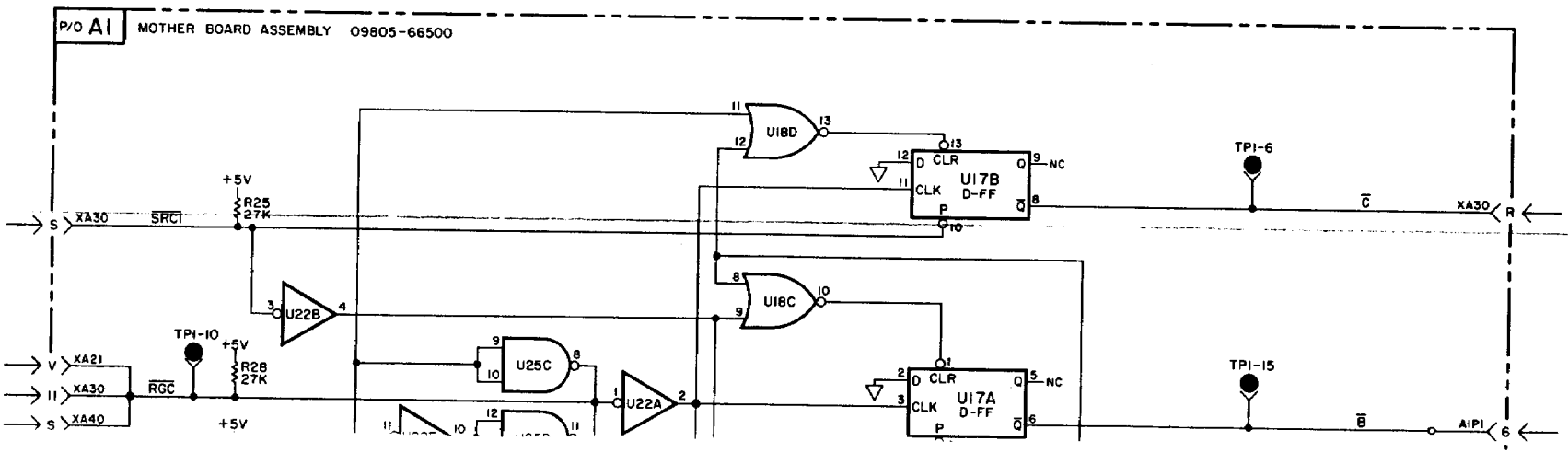
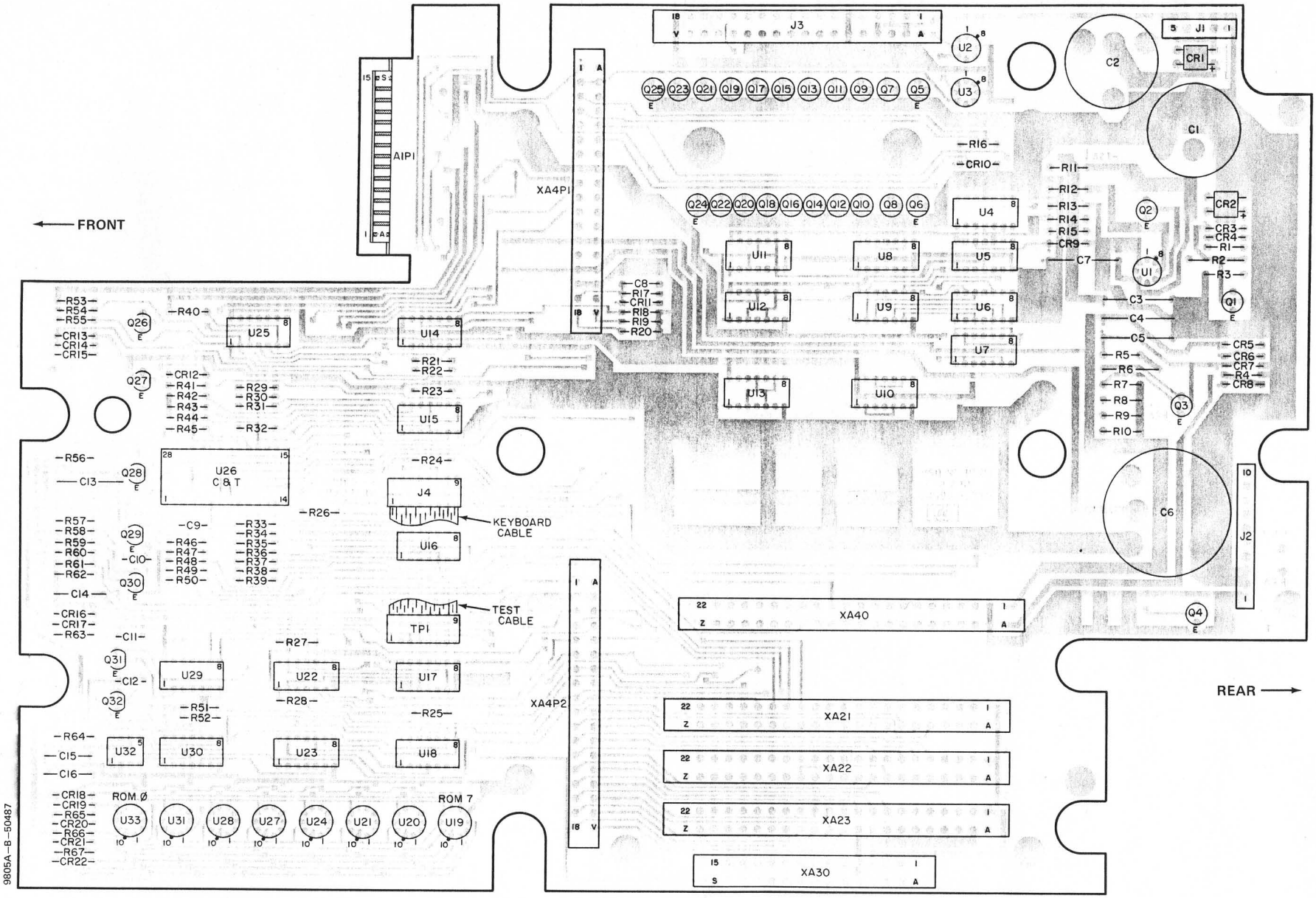


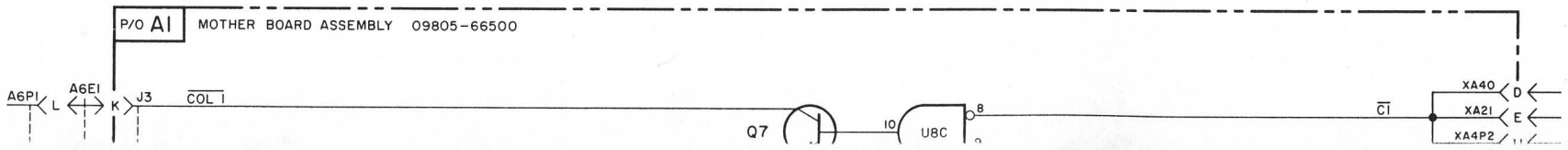
Figure 6-14. 9805A Motherboard Schematic (A1) — Sheet 1

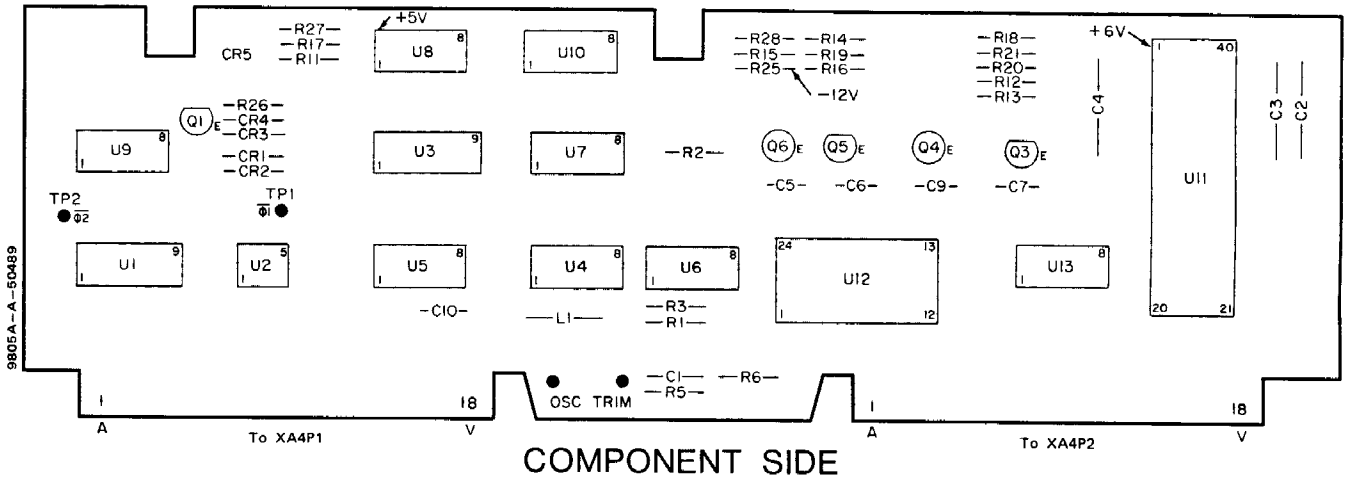


COMPONENT SIDE

A1

-hp- Part No. 09805-66500 Rev B





COMPONENT SIDE

A4

-hp- Part No. 09805-66540 Rev A

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A & R

$\phi 1$	1	16	$\phi 2$
GND	2	15	GND
IS	3	14	−12V
SYN	4	13	E
WS	5	12	D
CARRY	6	11	C
BCD	7	10	B
START	8	9	A

DATA STORAGE

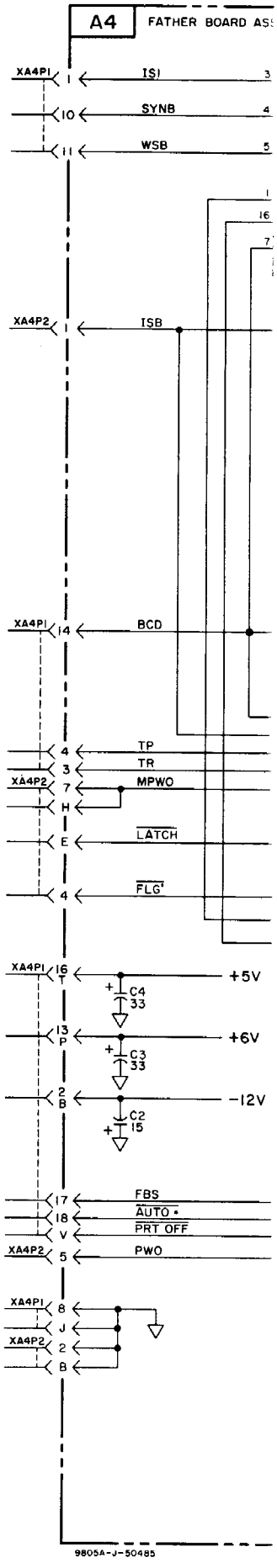
+6V	1	16	IS
GND	2	15	FLG
A2	3	14	BCD
A1	4	13	$\phi 2$
B1	5	12	$\phi 1$
B2	6	11	−12V
B3	7	10	BDE
B4	8	9	SRT

I/O PROCESSOR

+6V	1	40	−12V
BCD	2	39	C1
EXT	3	38	C2
LATCH	4	37	C3
FLG'	5	36	C4
$\phi 2$	6	35	C5
$\phi 1$	7	34	C6
START	8	33	C7
FLG	9	32	C8
PWO	10	31	C9
TP	11	30	C10
TR	12	29	C11
C20	13	28	C12
C19	14	27	C13
EIS1	15	26	C14
IS	16	25	C15
SCE	17	24	GND
IOC3	18	23	C16
IOC2	19	22	C17
IOC1	20	21	C18

CLOCK DRIVER

$\phi 2^{in}$	1	8	$\phi 2^{out}$
GND	2	7	NC (INHIBIT)
−12V	3	6	+6V
$\phi 1^{in}$	4	5	$\phi 1^{out}$



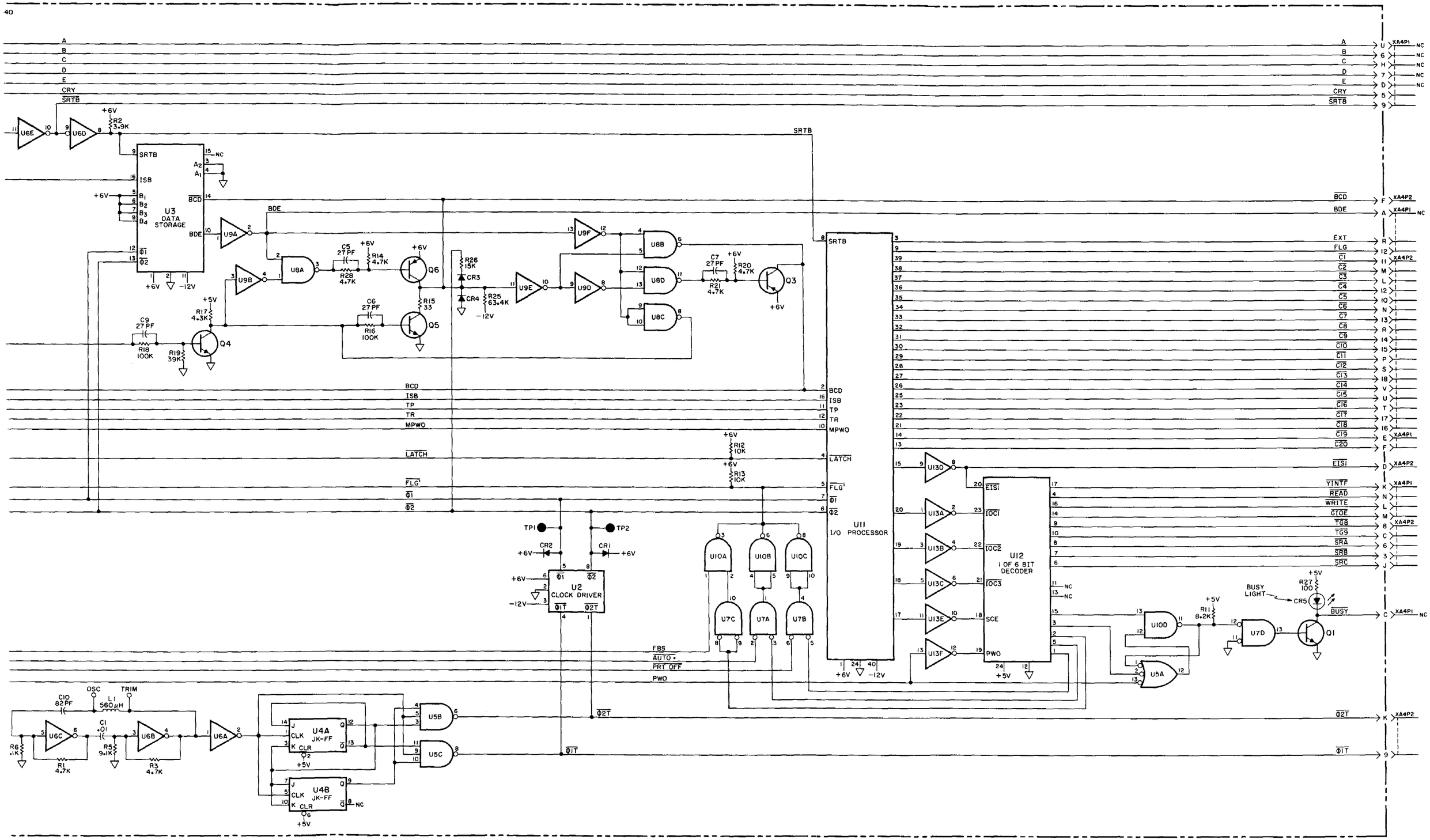


Figure 6-16. 9805A Fatherboard (A4) Schematic

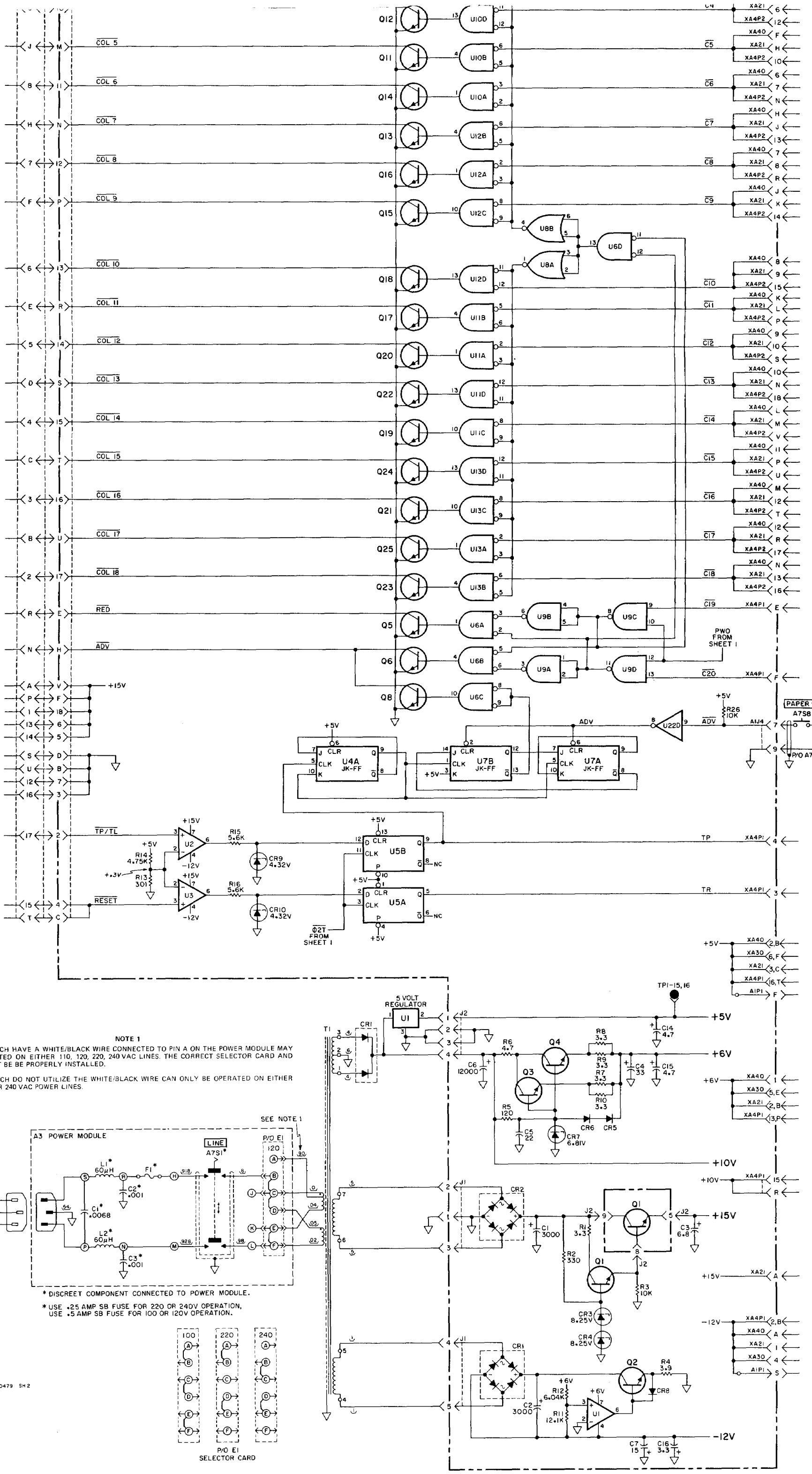
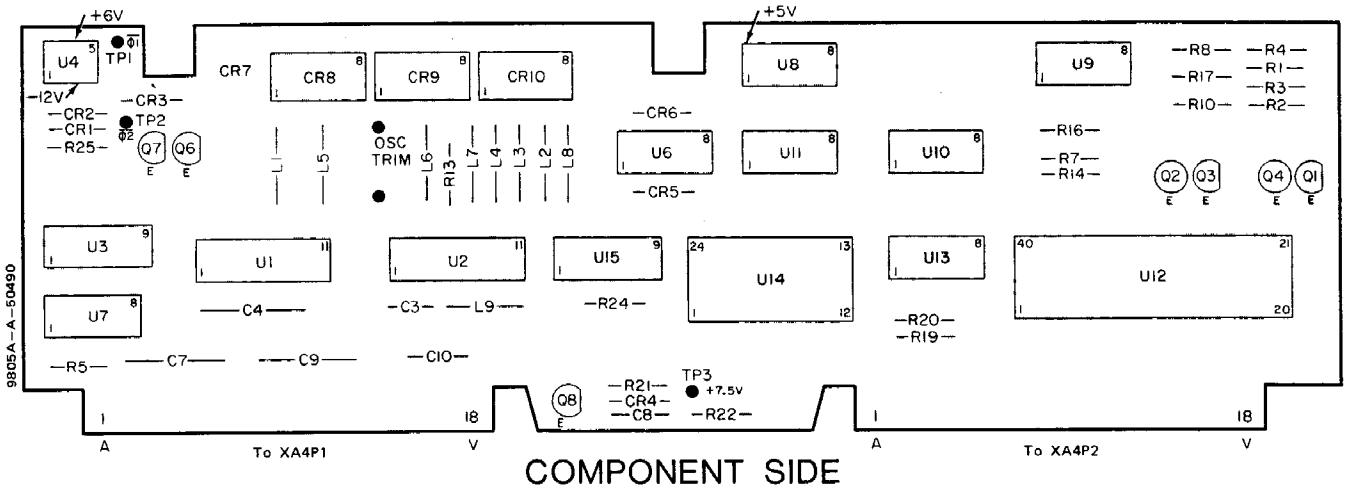


Figure 6-15. 9805A Motherboard Schematic (A1) — Sheet 2



COMPONENT SIDE

A5

-hp- Part No. 09805-66541 Rev A

ANODE DRIVER

c	1	20	SG*
b	2	19	SE*
a	3	18	SDP*
d	4	17	SF*
e	5	16	SD*
SHIFT-CLK	6	15	GND
$\phi 1$	7	14	SB*
$\phi 2$	8	13	SC*
CAP	9	12	SA*
(TRIM) NC	10	11	+4V

*SEGMENT ENABLE SIGNALS

CLOCK DRIVER

$\phi 2^{in}$	1	8	$\phi 2^{out}$
GND	2	7	NC (INHIBIT)
-12V	3	6	+6V
$\phi 1^{in}$	4	5	$\phi 1^{out}$

LED

DIGIT 5 SELECT	1	14	A
E	2	13	DIGIT 4 SELECT
C	3	12	B
DIGIT 3 SELECT	4	11	DIGIT 3 SELECT
DP	5	10	F
D	6	9	DIGIT 2 SELECT
DIGIT 1 SELECT	7	8	G

A & R

$\phi 1$	1	16	$\phi 2$
GND	2	15	GND
IS	3	14	-12V
SYN	4	13	E
WS	5	12	D
CARRY	6	11	C
BCD	7	10	B
START	8	9	A

DATA STORAGE

+6V	1	16	IS
GND	2	15	FLG
A2	3	14	BCD
A1	4	13	$\phi 2$
B1	5	12	$\phi 1$
B2	6	11	-12V
B3	7	10	BDE
B4	8	9	SRT

I/O PROCESSOR

+6V	1	40	-12V
BCD	2	39	C1
EXT	3	38	C2
LATCH	4	37	C3
FLG'	5	36	C4
$\phi 2$	6	35	C5
$\phi 1$	7	34	C6
START	8	33	C7
FLG	9	32	C8
PWO	10	31	C9
TP	11	30	C10
TR	12	29	C11
C20	13	28	C12
C19	14	27	C13
EIS1	15	26	C14
IS	16	25	C15
SCE	17	24	GND
IOC3	18	23	C16
IOC2	19	22	C17
IOC1	20	21	C18

CATHODE DRIVER

9*	1	20	8*
10*	2	19	7*
11*	3	18	6*
+4V	4	17	5*
12*	5	16	4*
13*	6	15	+4V
14*	7	14	3*
START	8	13	2*
CLK	9	12	1*
+7.5V	10	11	15*

*DIGIT ENABLE SIGNALS

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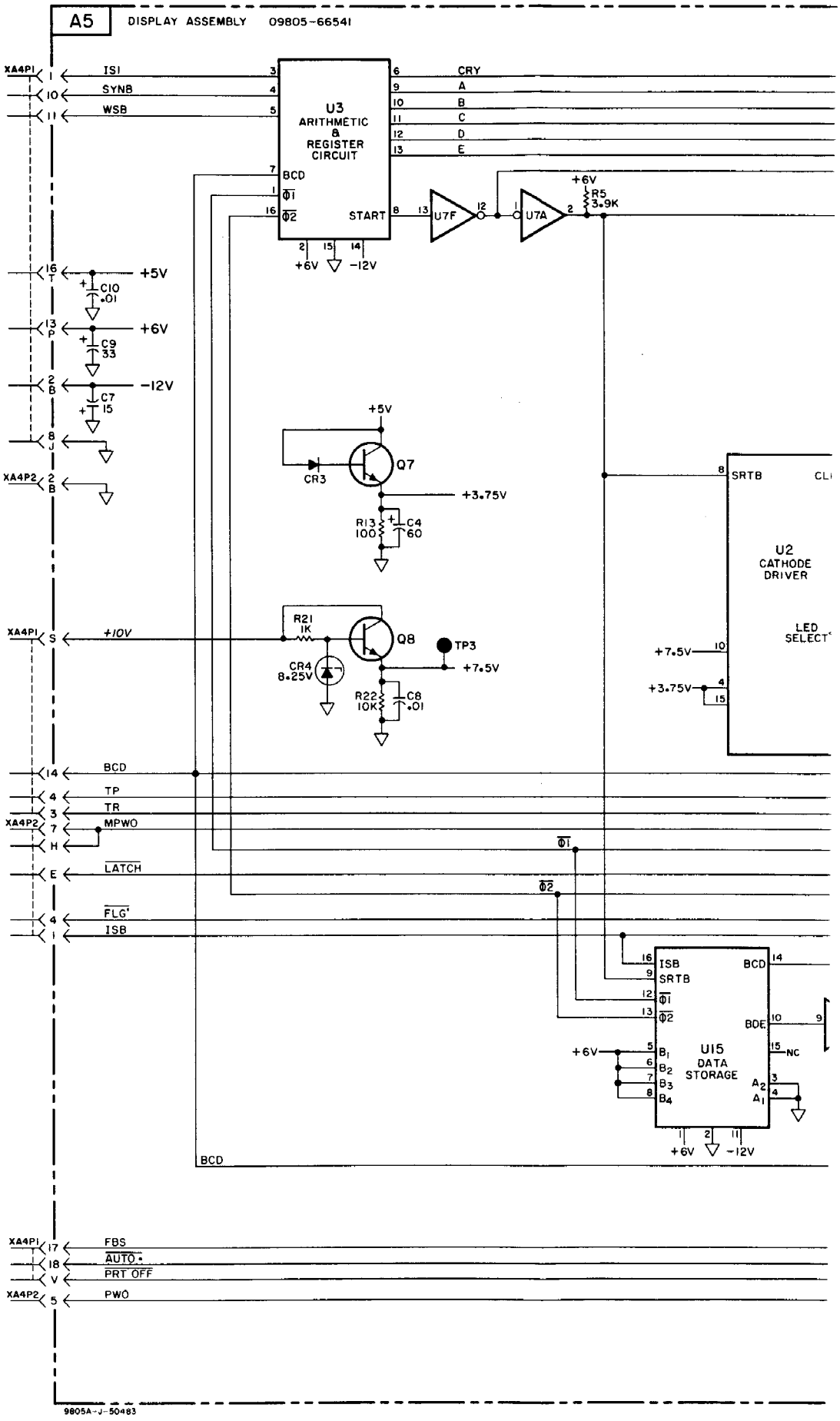

A5
DISPLAY ASSEMBLY 09805-66541
U3
ARITHMETIC & REGISTER CIRCUIT
U7F
U7A
R5 3.9K
+6V
U2
CATHODE DRIVER
LED SELECT
SRTB
Q7
CR3
+3.75V
R13 100
C4 60
Q8
TP3
+7.5V
R21 1K
CR4 8.25V
R22 10K
C8 .01
C10 .01
C9 33
C7 15
+5V
+10V
U15
DATA STORAGE
ISB
SRTB
BDE
NC
BCD
TP
TR
MPWO
LATCH
FLG'
ISB
FBS
AUTO.
PRT OFF
PWO
XA4P1
XA4P2
9805A-J-50483

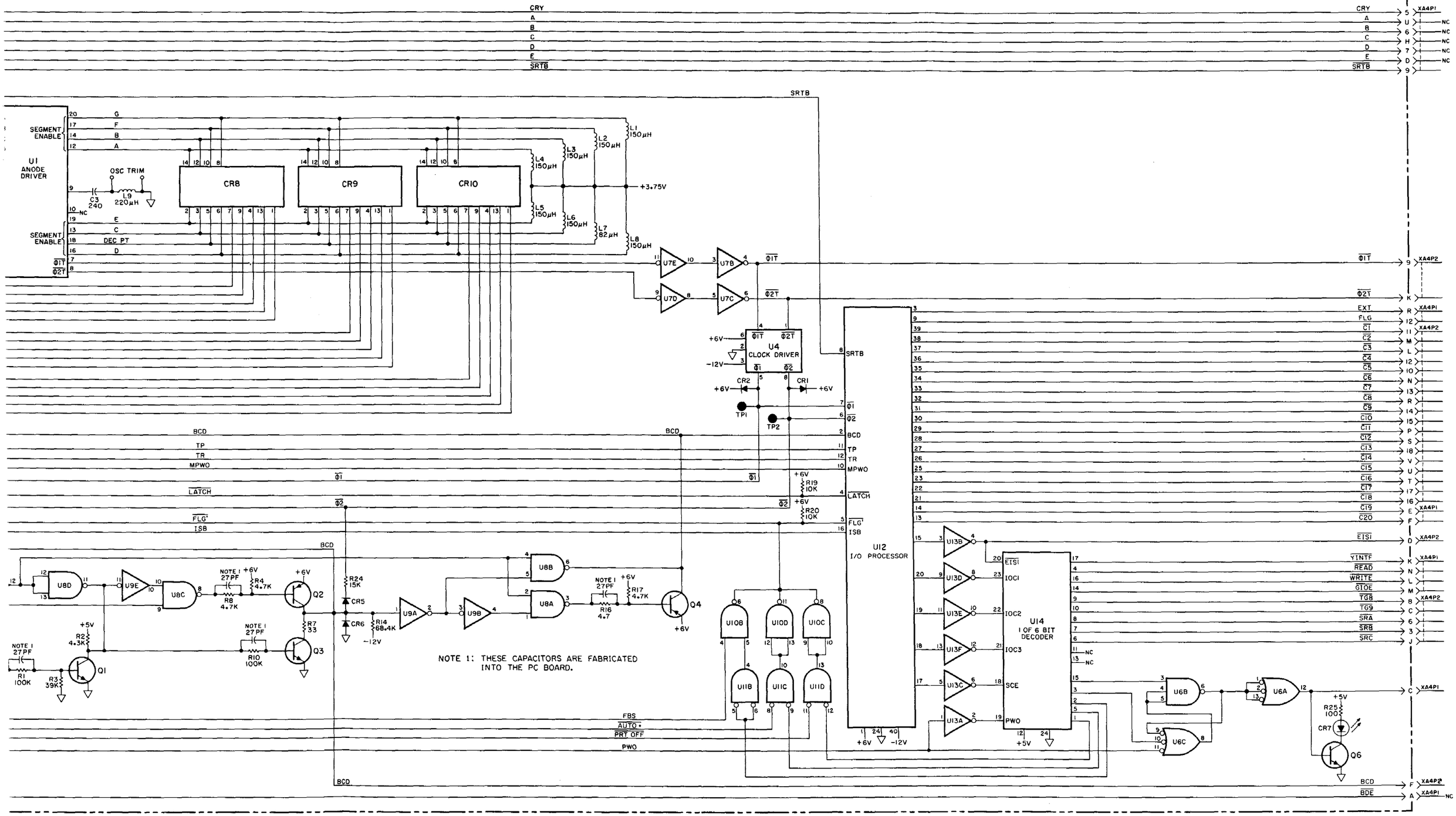
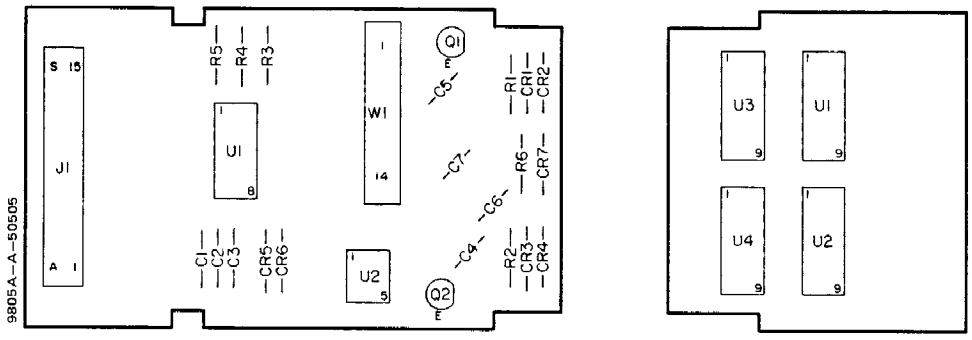


Figure 6-17. 9805A Display (A5) Schematic



COMPONENT SIDE

A10

-hp- Part No. 5060–9173 Rev A

A10A1

-hp- Part No. 5060–9175 Rev A

CLOCK DRIVER

$\phi 2^{in}$	1	8	$\phi 2^{out}$
GND	2	7	NC (INHIBIT)
−12V	3	6	+6V
$\phi 1^{in}$	4	5	$\phi 1^{out}$

DATA STORAGE

+6V	1	16	IS
GND	2	15	FLG
A2	3	14	BCD
A1	4	13	$\phi 2$
B1	5	12	$\phi 1$
B2	6	11	−12V
B3	7	10	BDE
B4	8	9	SRT

QUAD ROM

+6V	1	16	NC
NC	2	15	IA
NC	3	14	WS
GND	4	13	+6V
PWO	5	12	$\phi 1$
IS	6	11	−12V
SYN	7	10	$\phi 2$
NC	8	9	+6V

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Rev A

ROM

16	NC
15	IA
14	WS
13	+6V
12	ϕ1
11	−12V
10	ϕ2
9	+6V

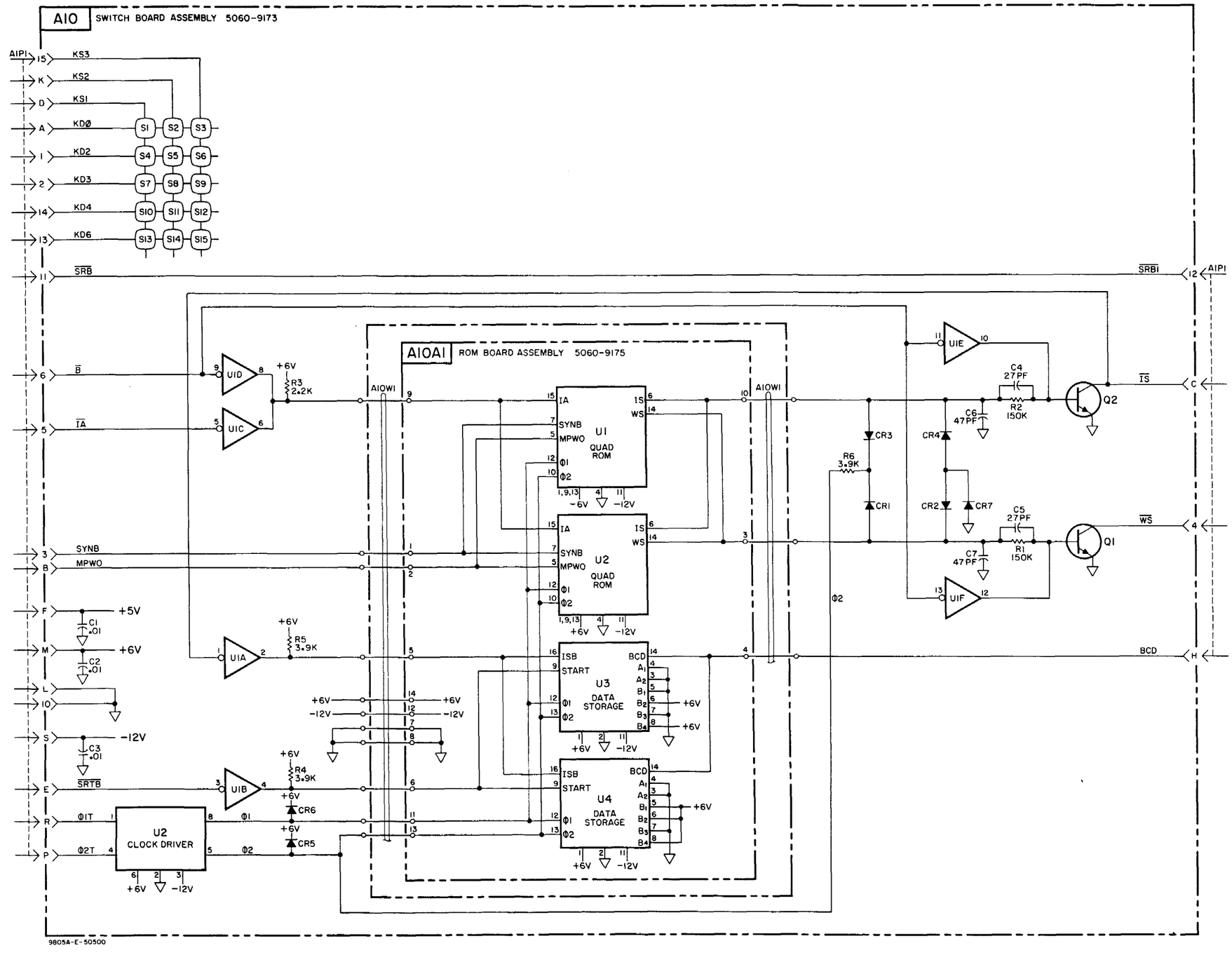
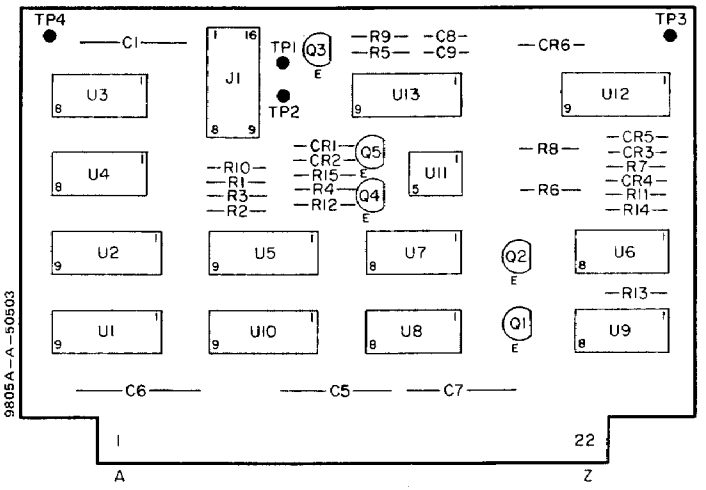


Figure 6-18. 9805A Keyblock (A10) Schematic



COMPONENT SIDE

A21

-hp- Part No. 11357-66501 Rev B

CLOCK DRIVER

$\phi 2^{in}$	1	8	$\phi 2^{out}$
GND	2	7	NC (INHIBIT)
−12V	3	6	+6V
$\phi 1^{in}$	4	5	$\phi 1^{out}$

DATA STORAGE

+6V	1	16	IS
GND	2	15	FLG
A2	3	14	BCD
A1	4	13	$\phi 2$
B1	5	12	$\phi 1$
B2	6	11	−12V
B3	7	10	BDE
B4	8	9	SRT

QUAD ROM

+6V	1	16	NC
NC	2	15	IA
NC	3	14	WS
GND	4	13	+6V
PWO	5	12	$\phi 1$
IS	6	11	−12V
SYN	7	10	$\phi 2$
NC	8	9	+6V

6-61/62

−12V	3	6	+6V
$\phi 1^{in}$	4	5	$\phi 1^{out}$

A2	3	14	BCD
A1	4	13	$\phi 2$
B1	5	12	$\phi 1$
B2	6	11	−12V
B3	7	10	BDE
B4	8	9	SRT

NC	3	14	WS
GND	4	13	+6V
PWO	5	12	$\phi 1$
IS	6	11	−12V
SYN	7	10	$\phi 2$
NC	8	9	+6V

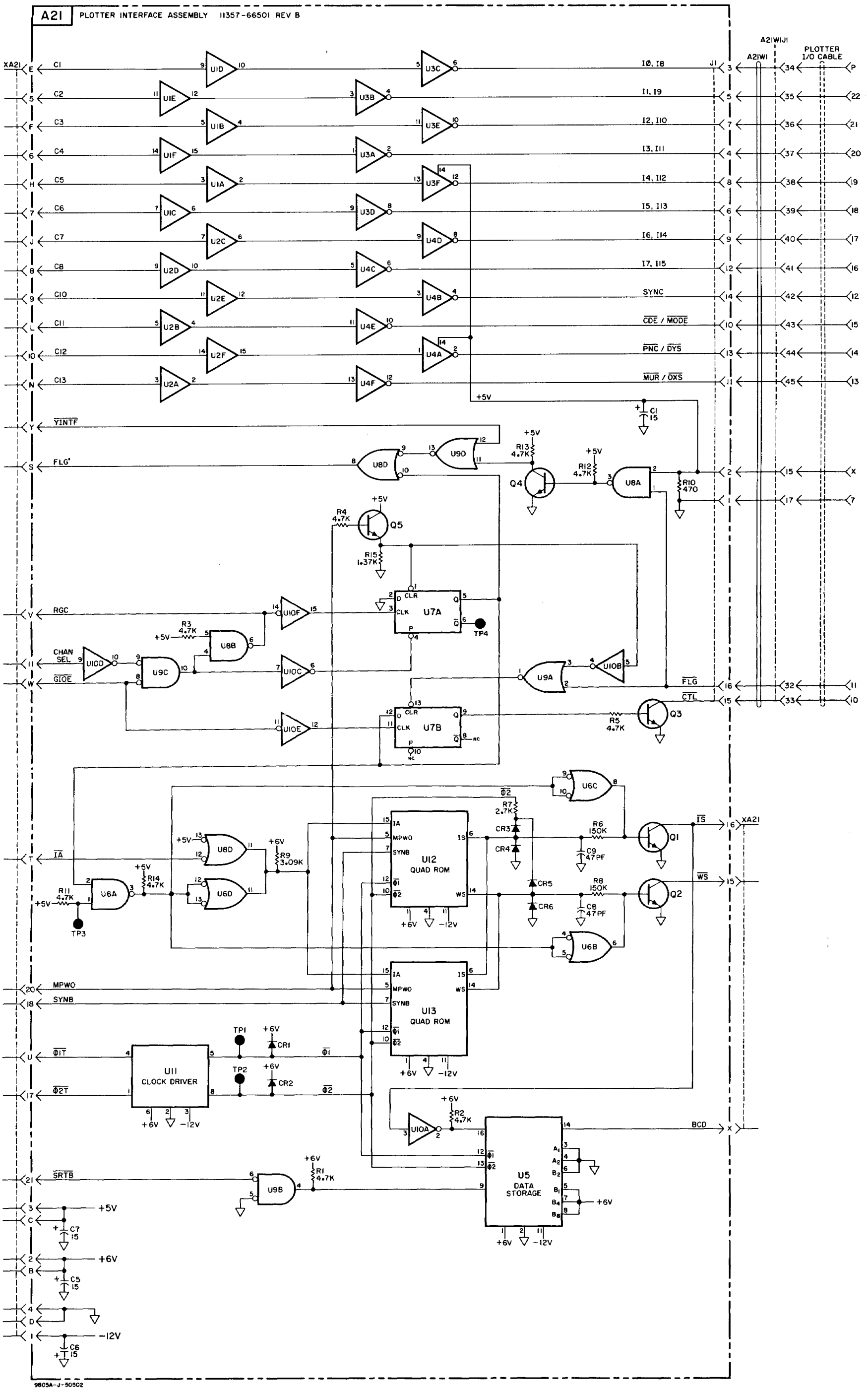
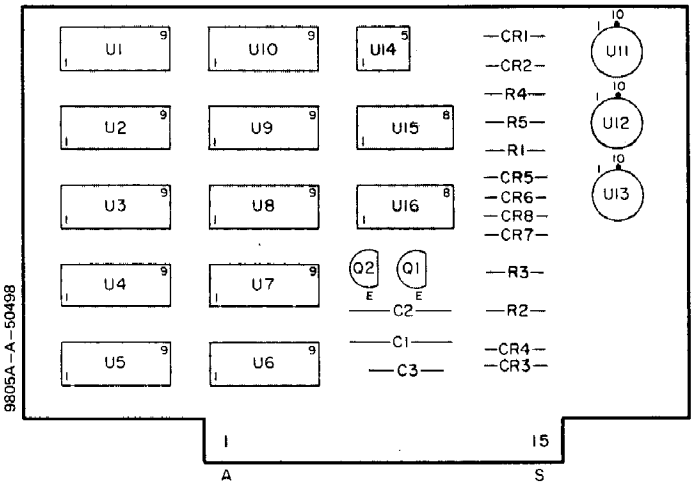


Figure 6-19. 9805A Plotter Interface (A21) Schematic



COMPONENT SIDE

A30

-hp- Part No. 11366-66501 Rev B

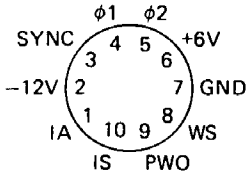
CLOCK DRIVER

$\phi 2^{in}$	1	8	$\phi 2^{out}$
GND	2	7	NC (INHIBIT)
−12V	3	6	+6V
$\phi 1^{in}$	4	5	$\phi 1^{out}$

DATA STORAGE

+6V	1	16	IS
GND	2	15	FLG
A2	3	14	BCD
A1	4	13	$\phi 2$
B1	5	12	$\phi 1$
B2	6	11	−12V
B3	7	10	BDE
B4	8	9	SRT

ROM



A30 OPTION DATA STORAGE ASSEMBLY 11366-67901 (30 DATA REGISTERS)

NOTE: U4 THRU U10 ARE NOT LOADED.

XA30 14 SRC (BOARD PRESENT) → SRC1 S

15 SRTB

12 BCD

13 FLG

P ISB

+6V R1 3.3K

U16C

SRTB, BCD, FLG, ISB, Φ2, Φ1 distributed to:

U1 REGISTERS 0-9
U2 REGISTERS 10-19
U3 REGISTERS 20-29
U4 REGISTERS 30-39
U5 REGISTERS 40-49
U6 REGISTERS 50-59
U7 REGISTERS 60-69
U8 REGISTERS 70-79
U9 REGISTERS 80-89
U10 REGISTERS 90-99

(each: ISB, FLG, BCD, Φ2, Φ1, SRTB; A2, A1, B1, B2, B3, B4; −12V, +6V)

CIRCUIT ADDRESS

Φ2 R5 1.5K

U16B ENABLE

CR4 CR3

9 IA

R (GROUP C ENABLE)

U15A U15C U15D +6V R4 1.5K

ROM GROUP C

U11: IA, MPWO, SYNB, Φ1, Φ2 → IS, WS (+6V, −12V)

CR5 CR6 CR7 CR8

C* R2 150K Q1 → IS K

C* R3 150K Q2 → WS J

U16A ENABLE

C* DENOTES CAPACITANCE MADE BY USING PC BOARD PLATING.

N MPWO

M SYNB

U12: IA, MPWO, SYNB, Φ1, Φ2 → IS, WS (+6V, −12V)

6 F +5V C3 4.7

5 E +6V C1 15

7 H

4 −12V C2 15

U13: IA, MPWO, SYNB, Φ1, Φ2 → IS, WS (+6V, +12V)

10 Φ1T

L Φ2T

U14 CLOCK DRIVER (+6V, −12V)

+6V CR2 Φ1

+6V CR1 Φ2

9805A-J-50492

Figure 6-20. 9805A Data Storage (A30) Schematic

CHAPTER 7
REPLACEMENT PARTS

INTRODUCTION

This chapter provides the information necessary for you to order replacement parts from either Customer Service Center (CSC) or Part Center Europe (PCE), whichever is more appropriate. Separate replacement parts lists are provided for each calculator.

SPECIAL ORDERING INFORMATION

Display Units

Replacement display units should be ordered using the part number for the particular intensity you require (3 ea.). An alpha code is provided on the back of each display unit which specifies the luminous-intensity of that unit; alpha code F specifies the lowest available luminous intensity, whereas code K is for the highest intensity. The replacement parts lists each contain the part number for each intensity.

C&T, A&R, and Clock Driver Units

The part numbers for the most recent designs of the C&T, A&R, and clock driver ICs is provided in the parts lists. Please replace defective units with replacement parts obtained by using the part numbers provided in this manual.

Printers

The printer in each model calculator (e.g., Model 46 or Model 81) is unique to that calculator. Do not replace the printer from one calculator with the printer from a different model calculator. The printer is a Blue Strip Exchange item.

CHAPTER 7
REPLACEMENT PARTS

Table 7-1. 9805A Replaceable Parts

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
A1		09805-66500			MOTHER BOARD ASSEMBLY		
	C1,C2	0180-2565		2	C-F: 3000 UF 30V		
	C3	0180-0116		1	C-F: 6.8 UF 35V		
	C4	0180-0229		3	C-F: 33 UF 10V		
	C5	0180-0228		1	C-F: 22 UF 15V		
	C6	0180-2566		1	C-F: 12000 UF 15V		
	C7	0180-1746		2	C-F: 15 UF 20V		
	C8	0160-3847		2	C-F: .01 UF 25V		
	C9-C12	0160-2306		8	C-F: 27 PF 300V		
	C13	0180-0106		1	C-F: 60 UF 6V		
	C14, C15	0180-0309		2	C-F: 4.7 UF 10V		
	C16	0180-0210		1	C-F: 3.3 UF 15V		
	CR1, CR2	1906-0023		2	DIO: SI, 200V		
	CR3, CR4	1902-3139		2	DIO: BKDN, 8.25V		
	CR5, CR6	1901-0040		14	DIO: SI, .05A 30V		
	CR7	1902-0052		2	DIO: BKDN, 6.81V		
	CR8	1901-0040			DIO: SI, .05A 30 V		
	CR9, CR10	1902-3073		2	DIO: BKDN, 4.32V		
	CR11	1901-0040			DIO: SI, .05A 30V		
	CR12	1902-0052			DIO: BKDN, 6.81V		
	CR13-CR17	1901-0040			DIO: SI, .05A 30V		
	CR18, CR19	1910-0016		4	DIO: GE, 60V		
	CR20-CR22	1901-0040			DIO: SI, .05A 30V		
	Q1, Q2	1854-0039		2	TSTR: SI, NPN		
	Q3, Q4	1854-0053		2	TSTR: 2N2218		
	Q5-Q25	1854-0087		21	TSTR: SI, NPN		
	Q26-Q32	1854-0071		10	TSTR: SI, NPN		
	R1	0683-0335		5	R-F: 3.3 OHM 5%		
	R2	0687-3311		1	R-F: 330 OHM 10%		
	R3	0684-1031		7	R-F: 10K 10% ¼W		
	R4	0683-0395		1	R-F: 3.9 OHM 5%		
	R5	0684-1211		1	R-F: 120 OHM 10%		
	R6	0698-0001		1	R-F: 4.7 OHM 5%		
	R7-R10	0683-0335			R-F: 3.3 OHM 5%		
	R11	0757-0444		1	R-F: 12.1K 1%		
	R12	0698-3497		1	R-F: 6.04K 1%		
	R13	0757-0410		1	R-F: 301 OHM 1%		
	R14	0757-0437		1	R-F: 4.75K 1%		
	R15, R16	0684-5621		2	R-F: 5.6K 10%		
	R17	0757-0433		1	R-F: 3.32K 1%		
	R18	0757-0280		1	R-F: 1K 1%		
	R19, R20	0684-1031			R-F: 10K 10% ¼W		
	R21-R24	0684-2231		11	R-F: 22K 10% ¼W		
	R25	0684-2731		3	R-F: 27K 10% ¼W		
	R26	0684-1031			R-F: 10K 10% ¼W		
	R27, R28	0684-2731			R-F: 27K 10% ¼W		
	R29-R32	0684-2231			R-F: 22K 10% ¼W		
	R33-R39	0698-3280		8	R-F: 63.4K 1%		
	R40	0684-3321		6	R-F: 3.3K 10%		
	R41	0684-2231			R-F: 22K 10% ¼W		
	R42-R45	0684-3321			R-F: 3.3K 10%		
	R46	0684-1541		4	R-F: 150K 10% ¼W		
	R47	0684-1041		4	R-F: 100K 10% ¼W		
	R48	0684-1821		2	R-F: 1.8K 10%		
	R49	0684-2221		1	R-F: 2.2K 10%		
	R50	0684-1821			R-F: 1.8K 10%		
	R51,R52	0684-6811		6	R-F: 680 OHM 10%		
	R53	0684-4721		7	R-F: 4.7K 10%		

Table 7-1. 9805A Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	R54,R55	0684-2231			R-F: 22K 10% ¼W		
	R56	0684-6811			R-F: 680 OHM 10%		
	R57	0684-1541			R-F: 150K 10% ¼W		
	R58	0684-1041			R-F: 100K 10% ¼W		
	R59	0684-1031			R-F: 10K 10% ¼W		
	R60	0684-6811			R-F: 680 OHM 10%		
	R61	0684-3321			R-F: 3.3K 10%		
	R62	0684-3331		1	R-F: 33K 10% ¼W		
	R63, R64	0684-1541			R-F: 150K 10% ¼W		
	R65	0684-2721		1	R-F: 2.7K 10%		
	R66, R67	0684-6811			R-F: 680 OHM 10%		
	U1-U3	1820-0203		3	IC: OPR AMPL		
	U4	1820-0595		3	IC: DM 74L73N; J-K FLIP-FLOP		
	U5	1820-0596		3	IC: DM 74L74N; D FLIP-FLOP		
	U6	1820-0584		8	IC: SN74L02; NOR GATE		
	U7	1820-0595			IC: DM 74L74N; J-K FLIP-FLOP		
	U8	1820-0584			IC: SN 74L02; NOR GATE		
	U9	1820-0583		2	IC: DM 74L00; NAND GATE		
	U10-U13	1820-0584			IC: SN 74L02; NOR GATE		
	U14	1820-0589		1	IC: DIGITAL; 8-input NAND GATE		
	U15	1820-0583			IC: DM 74L00; NAND GATE		
	U16	1820-0586		5	IC: DM 74L04N; HEX INVERTER		
	U17	1820-0596			IC: DM 74L74N; D FLIP-FLOP		
	U18	1820-0584			IC: SN 74L02; NOR GATE		
	U19	1818-0048		1	IC: ROM 7		
	U20	1818-0047		1	IC: ROM 6		
	U21	1818-0046		1	IC: ROM 5		
	U22	1820-0586			IC: DM 74L04N; HEX INVERTOR		
	U23	1820-0596			IC: DM 74L74; D FLIP-FLOP		
	U24	1818-0045		1	IC: ROM 4		
	U25	1820-0585		3	IC: DM 74L03N; O.C. NAND GATE		
	U26	1818-0078		1	IC: C&T		
	U27	1818-0044		1	IC: ROM 3		
	U28	1818-0043		1	IC: ROM 2		
	U29,U30	1820-0577		2	IC: SN 7416N; O.C. HEX INVERTER		
	U31	1818-0042		1	IC: ROM 1		
	U32	1820-1127		2	IC: CLOCK DRIVER		
	U33	1818-0041		1	IC: ROM 0		
					MISCELLANEOUS PARTS		
		09805-27301		1	FLEX CABLE, 16 CONDUCTOR		
	J4,TP1	1200-0423		2	IC SOCKET, 16 PIN		
	J2	1251-0523		1	MALE CONNECTOR, 15 PIN		
	J1	1251-0526		1	MALE CONNECTOR, 10 PIN		
	XA21, XA40	1251-1365		4	PC CONNECTOR, 2x22 PIN		
	XA4, J3	1251-2026		3	PC CONNECTOR, 2X18 PIN		
	XA30	1251-2035		1	PC CONNECTOR, 2X15 PIN		
		1205-0011		3	HEAT SINK, TSTR		
		5040-7420		4	PAD, PRINTER SUPPORT		
		5040-7436		1	CABLE CLAMP		
A4		**09805-66540**			**PC ASSY FATHER BOARD**		
	C1	0160-3847			C-F: .01 UF, 25V		
	C2	0180-1746			C-F: 15 UF, 20V		
	C3,C4	0180-0229			C-F: 33 UF, 10V		
	C5-C7, C9	0160-2306			C-F: 27 PF, 300V		

Table 7-1. 9805A Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	C10	0140-0193		1	C-F: 82 PF, 300V		
	CR1, CR2	1910-0016			DIO: GE, 60V		
	CR3, CR4	1901-0040			DIO: SI, .05A 30V		
	LED 1	1900-0410		1	DIO: LIGHT EMITTING		
	L1	9100-1648		1	L-F: 560 UH		
	Q1	1854-0071			TSTR: SI, NPN		
	Q3	1853-0010		2	TSTR: SI, PNP		
	C4, Q5	1854-0071			TSTR: SI, NPN		
	Q6	1853-0010			TSTR: SI, PNP		
	R2	0684-3921		1	R-F: 3.9K, 10%		
	R3, R4	0684-4721			R-F: 4.7K, 10%		
	R5, R6	0683-9125		2	R-F: 9.1K, 5%		
	R11	0684-8221		1	R-F: 8.2K, 10%		
	R12, R13	0684-1031			R-F: 10K, 10% ¼W		
	R14	0684-4721			R-F: 4.7K, 10%		
	R15	0698-5101		1	R-F: 33 OHM, 10%		
	R16	0684-1041			R-F: 100K, 10% ¼W		
	R17	0683-4325		1	R-F: 4.3K, 5%		
	R18	0684-1041			R-F: 100K, 10% ¼W		
	R19	0684-3931		1	R-F: 39K, 10% ¼W		
	R20, R21	0684-4721			R-F: 4.7K, 10%		
	R25	0698-3280			R-F: 63.4K, 1%		
	R26	0684-1531		1	R-F: 15K, 10% ¼W		
	R27	0684-1011		1	R-F: 100 OHM, 10%		
	R28	0684-4721			R-F: 4.7K, 10%		
	U1	1820-1169		1	IC: A&R		
	U2	1820-1127			IC: CLOCK DRIVER		
	U3	1820-0993		1	IC: DATA STORAGE		
	U4	1820-0595			IC: DM 74L73N; J-K FLIP-FLOP		
	U5	1820-0587		1	IC: 74L10N; 3 INPUT NAND GATE		
	U6	1820-0586			IC: DM 74L04N; HEX INVERTER		
	U7	1820-0584			IC: SN 74L02; NOR GATE		
	U8	1820-0585			IC: DM 74L03N; O.C. NAND GATE		
	U9	1820-0586			IC: DM 74L04N; HEX INVERTER		
	U10	1820-0585			IC: DM 74L03N; O.C. NAND GATE		
	U11	1820-0994		1	IC: I/O PROCESSOR		
	U12	1820-0702		1	IC: SL 17303; 1 of 6 DECODER		
	U13	1820-0586			IC: DM 74L04N; HEX INVERTER		
		0380-0059		1	SPACER-CAPTIVE		
A5		09805-66541			**PC ASSY DISPLAY**		
	C3	0140-0222		1	C-F: 240 PF		
	C4	0160-3847		1	C—F: 60 UF, 6V		
	C7	0180-1746		1	C-F: 15 UF, 20V		
	C8	0160-3847		2	C-F: .01 UF, 25V		
	C9	0180-0229		1	C-F: 33 UF, 10V		
	C10	0160-3847			C-F: .01 UF, 25V		
	CR1-CR3	1910-0016		3	DIO: GE, 60V		
	CR4	1902-3139		1	DIO: BKDN, 8.25V		
	CR5, CR6	1901-0040		2	DIO: SI, .05A 30V		
	CR8-CR10	1990-0335		3	DISPLAY **FAMILY**		
	CR8-CR10	1990-0421*			DISPLAY; F INTENSITY		
	CR8-CR10	1990-0422*			DISPLAY; G INTENSITY		
	CR8-CR10	1990-0423*			DISPLAY; H INTENSITY		
	CR8-CR10	1990-0424*			DISPLAY; I INTENSITY		
	CR8-CR10	1990-0425*			DISPLAY; J INTENSITY		
	CR8-CR10	1990-0426*			DISPLAY: K INTENSITY		

*See 'Introduction' in this chapter.

Table 7-1. 9805A Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	CR7	1990-0410		1	DIO: LIGHT EMITTING		
	L1-L6	9100-1639		7	L-F: 150 UH		
	L7	9140-0238		1	L-F: COIL-CHOKE		
	L8	9100-1639			L-F: 150 UH		
	L9	9140-0129		1	L-F: 220 UH		
	Q1	1854-0071		5	TSTR: SI, NPN		
	Q2	1853-0010		2	TSTR: SI, PNP		
	Q3	1854-0071			TSTR: SI, NPN		
	Q4	1853-0010			TSTR: SI, PNP		
	Q6-Q8	1854-0071			TSTR: SI, NPN		
	R1	0684-1041		2	R-F: 100K, 10% ¼W		
	R2	0683-4325		1	R-F: 4.3K, 5%		
	R3	0684-3931		1	R-F: 39K, 10% ¼W		
	R4	0684-4721		4	R-F: 4.7K, 10%		
	R5	0684-3921		1	R-F: 3.9K, 10% ¼W		
	R7	0698-5101		1	R-F: 33 OHM, 10%		
	R8	0684-4721			R-F: 4.7K, 10%		
	R10	0684-1041			R-F: 100K, 10% ¼W		
	R13	0684-1011		2	R-F: 100 OHM, 10%		
	R14	0698-3280		1	R-F: 63.4K, 1%		
	R16, R17	0684-4721			R-F: 4.7K, 10%		
	R19, R20	0684-1031		3	R-F: 10K, 10% ¼W		
	R21	0684-1021		1	R-F: 1K, 10%		
	R22	0684-1031			R-F: 10K, 10% ¼W		
	R24	0684-1531		1	R-F: 15K, 10% ¼W		
	R25	0684-1011			R-F: 100 OHM, 10%		
	U1	1820-1029		1	IC: ANODE DRIVER		
	U2	1820-1226		1	IC: CATHODE DRIVER		
	U3	1820-1169		1	IC: A&R		
	U4	1820-1127		1	IC: CLOCK DRIVER		
	U6	1820-0587		1	IC: DM 74L10N; 3 INPUT NAND GATE		
	U7	1820-0586		3	IC: DM 74L04N; HEX INTERTER		
	U8	1820-0585		2	IC: DM 74L03N; O.C. NAND GATE		
	U9	1820-0586			IC: DM 74L04N; HEX INVERTER		
	U10	1820-0585			IC: DM 74L03N; O.C. NAND GATE		
	U11	1820-0584		1	IC: SN 74L02; NOR GATE		
	U12	1820-0994		1	IC: I/O PROCESSOR		
	U13	1820-0586			IC: 74L04N; HEX INVERTER		
	U14	1820-0702		1	IC: SL 17303; 1 of 6 DECODER		
	U15	1820-0993		1	IC: DATA STORAGE		
		0380-0059		1	SPACER-CAPTIVE		
A7		**09805-67930**			**KEYBOARD ASSY**		
		0380-0065		3	SPACER-CAPTIVE		
		0380-0945		5	STANDOFF		
		0380-1029		1	STANDOFF-RIVET ON		
		09805-00103		1	PLATE-KEYBOARD		
		09805-23701		1	SCREW-CAPTIVE		
		09805-26530		1	PC BOARD-KEYBOARD		
		1460-0519		1	SPRING COIL		
		3101-1745		31	SWITCH-KEYBOARD		
		3101-1746		2	SWITCH-KEYBOARD		
		8120-0539		1	CABLE ASSEMBLY		
		09805-90002		2	OPERATING GUIDE		
		09805-90003		2	INSTRUCTION BOOKLET		
		09805-90004		2	EXP OPERATING GUIDE		

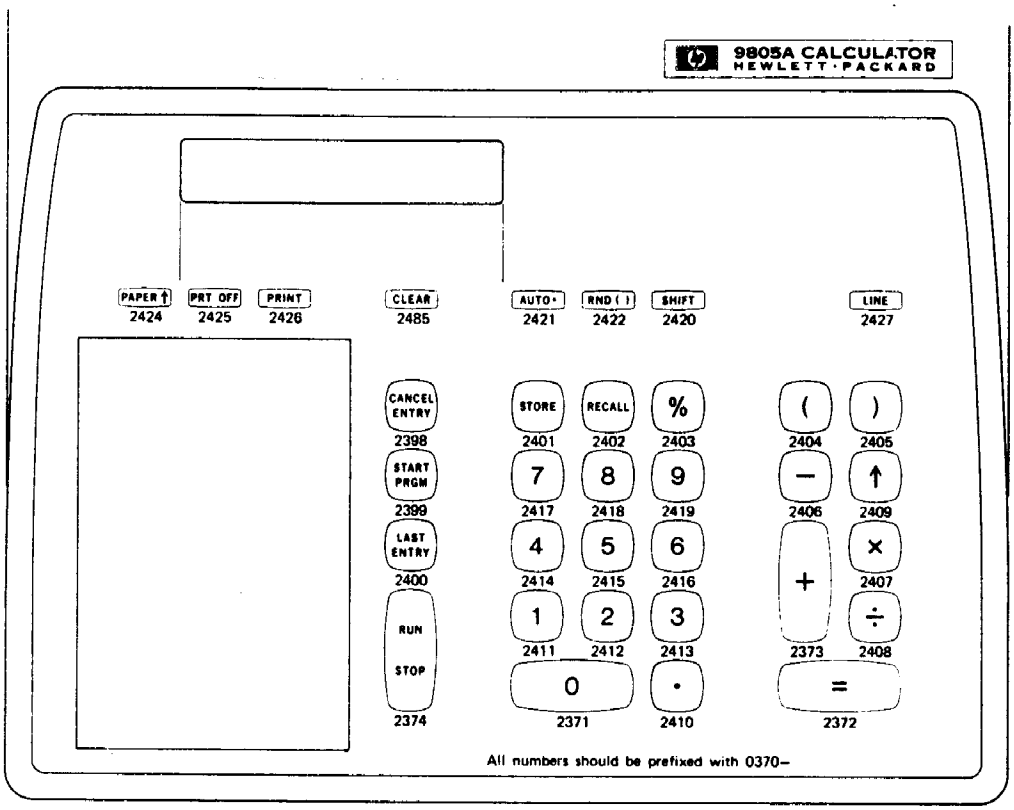


Figure 7-1. 9805A Keycap Part Numbers

Table 7-1. 9805A Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
A10		09805-67901			KEYBLOCK STAT		
		0370-0501		1	KEYCAP, HISTO		
		0370-0502		1	KEYCAP, LINEAR		
		0370-0503		1	KEYCAP, PARA		
		0370-0504		1	KEYCAP, STAT RECALL		
		0370-0505		1	KEYCAP, EVAL		
		0370-0506		1	KEYCAP, t		
		0370-0507		1	KEYCAP, BASIC STAT		
		0370-0508		1	KEYCAP, PLOT		
		0370-0509		1	KEYCAP, CHAR#		
		0370-0510		1	KEYCAP, AXES		
		0370-0511		1	KEYCAP, CHANGE SAMPLE		
		0370-0512		1	KEYCAP, DELETE		
		0370-0513		1	KEYCAP, VAR#		
		0370-0514		1	KEYCAP, OFFSET/WIDTH		
		0370-0515		1	KEYCAP, DATA ENTRY		
		0520-0246		4	SCREW-MACHINE		
		0520-0247		1	SCREW-MACHINE		
		11331-27301		1	CABLE-FLEX		
		3101-1745		15	SWITCH-KEYBOARD		
		5040-5959		1	BOX-FUNCTION BLOCK		
		5040-5960		1	LID-FUNCTION BLOCK		
		5040-7388		2	LATCH		
		5040-7473		1	CLAMP-FLEX CABLE		
A10		5060-9173		1	PC ASSY-STAT SWITCH		
	C1-C3	0160-3847		3	C-F: .01 UF, 25V		
	C4,C5	0160-0378		2	C-F: 27 PF, 500V		
	C6,C7	0140-0204		2	C-F: 47 PF, 500V		
	CR1-CR4	1901-0040		5	DIO: SI, .05A 30V		
	CR5,CR6	1901-0016		2	DIO: GE, 60V		
	CR7	1901-0040			DIO: SI, .05A 30V		
	R1,R2	0684-1541		2	R-F: 150K, 10%		
	R3	0684-2221		1	R-F: 2.2K, 10%		
	R4-R6	0684-3921		3	R-F: 3.9K, 10%		
	Q1,Q2	1854-0071		2	TSTR: SI, PNP		
	U1	1820-0577		1	IC: SN 7416N; HEX INVERTER		
	U2	1820-1127		1	IC: CLOCK DRIVER		
		0380-1010		4	STDF-CAPTIVE		
		0570-0510		3	STUD-PRESS IN		
A10	A1	5060-9175		1	PC ASSY-STAT ROM		
	U1	1818-0049		1	IC: QUAD-ROM		
	U2	1828-0050		1	IC: QUAD-ROM		
	U3,U4	1820-0993		2	IC: DATA STORAGE		
		0380-1011			SPACER: CAPTIVE		
		7120-3552			LABEL, PC ASSY		
A20		11357-67901			I/O ASSY-PLOTTER		
	C1	0180-1746		4	C-F: 15 UF, 20V		
	C5-C7	0180-1746			C-F: 15 UF, 20V		
	C8,C9	0140-0204		2	C-F: 47 PF, 500V		
	CR1,CR2	1910-0016		2	DIO: GE, 60V		
	CR3-CR6	1901-0040		4	DIO: SI, .05A 30V		
	Q1-Q5	1854-0071		5	TSTR: SI, NPN		
	R1-R5	0684-4721		9	R-F: 4.7K, 10%		
	R6	0684-1541		2	R-F: 150K, 10% ¼W		
	R7	0684-2721		1	R-F: 2.7K, 10%		
	R8	0684-1541			R-F: 150K, 10% ¼W		

Table 7-1. 9805A Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	R9	0698-4438		1	R-F: 3.09K, 1%		
	R10	0684-4711		1	R-F: 470 OHM, 10%		
	R11-R14	0684-4721			R-F: 4.7K, 10%		
	R15	0698-4423		1	R-F: 1.37K, 1%		
	U1,U2	1820-0980		2	IC: DIGITAL; BUFFER-DRIVER		
	U3,U4	1820-0174		2	IC: SN 7404N; HEX INVERTER		
	U5	1820-0993		1	IC: DATA STORAGE		
	U6	1820-0585		2	IC: DM 74L03N; O.C. NAND GATE		
	U7	1820-0596		1	IC: DM 74L74N; D FLIP-FLOP		
	U8	1820-0585			IC: DM 74L03N; O.C. NAND GATE		
	U9	1820-0584		1	IC: SN 74L02; NOR GATE		
	U10	1820-0979		1	IC: CD 4009AE; HEX INVERTER		
	U11	1820-1127		1	IC: CLOCK DRIVER		
	U12	1818-0052		1	IC: QUAD-ROM		
	U13	1818-0053		1	IC: QUAD-ROM		
		11357-61601		1	CABLE-OUTPUT		
		11357-66501		1	PC ASSY-PLOTTER		
		7120-3566		1	LABEL-ID		
A30		**11366-67901**			**DATA STORAGE ASSY**		
	C1,C2	0180-1746		2	C-F: 15 UF, 20V		
	C3	0180-0309		1	C-F: 4.7 UF, 10V		
	CR1,CR2	1910-0016		2	DIO: GE, 60V		
	CR3-CR8	1901-0040		6	DIO: SI, .05A 30V		
	Q1,Q2	1854-0071		2	TSTR: SI, NPN		
	R1	0684-3321		1	R-F: 3.3K, 10%		
	R2,R3	0684-1541		2	R-F: 150K, 10% ¼W		
	R4,R5	0684-1521		2	R-F: 1.5K, 10%		
	U1	1820-0585		2	IC: DM 74L03N; O.C. NAND GATE		
	U2	1820-1127		1	IC: CLOCK DRIVER		
	U3	1818-0038		1	IC: ROM		
	U4	1818-0039		1	IC: ROM		
	U5	1818-0040		1	IC: ROM		
	U8-U10	1820-0993		3	IC: DATA STORAGE		
	U18	1820-0585			IC: DM 74L03N; O.C. NAND GATE		
		09805-60301		1	**REAR PANEL ASSY**		
		3040-0416		1	INSTULATOR, TSTR		
		0340-0527		2	WASHER		
		0380-0093		2	STAND OFF		
		09805-01224		1	SHIELD		
		09805-21101		1	HEAT SINK		
		09805-61603		1	PWR MODULE		
		1251-0524		1	CONNECTOR, 5 PIN SHELL		
		1251-0525		1	CONNECTOR, 10 PIN SHELL		
	U1	1820-0480		1	IC: 5V REGULATOR		
	Q1	1854-0072		1	TSTR: 2N3054		
	CR1,CR2	1901-1001		2	DIO: BRDG RECT. ASSY		
		2260-0001		6	NUT, HEX		
		3101-1720		1	SWITCH, ON/OFF		
		5060-7442		1	BACK PANEL		
		7120-3640		1	LINE MODULE DECAL		
		9100-3299		1	POWER TRANSFORMER		

Table 7-1. 9805A Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
		09805-64401		**1**	**TOP CABINET ASSY**		
		4040-0925			KEYBOARD PANEL		
		4040-0970			TOP CABINET		
		5040-7402			DISPLAY WINDOW		
		7120-3220			NAMEPLATE		
		2200-0778		4	SCREW, MACHINE		
					MISCELLANEOUS PARTS		
A40		11376-67901			STATISTICS PROM ASSY		
A6		09805-69479			PRINTER, SEIKO (Rebuilt)		
		09805-04101			BOTTOM COVER		
		09805-23751			PAPER SHAFT		
		09805-61220			STORAGE ASSY BRACKET		
		4040-0983			PAPER BUCKET		
		5040-7406			KEYBLOCK BASKET		
		5040-7407			CABINET GASKET		
		5061-0707			CARRYING CASE		
		4040-0979			DUST COVER		
		4040-0971			BOTTOM CABINET		
		4040-0926			PRINTER COVER		
		2360-0322		13	SCREW		
		2360-0321		7	SCREW		
		2260-0001		6	HEX NUT		
		0515-0003		4	HEX SCREW, PRINTER		
	F1	2110-0201			FUSE: .25A SB (250V)		
	F1	2110-0202			FUSE: .50V SB (250V)		
		09805-26520			INTRA-CONNECT BD, PRINTER		
		09805-26531			INTRA-CONNECT BK, KEYBLOCK		
		9281-0415			PRINTER PAPER		
		9282-0511			PRINTER RIBBON		
		7120-3569			PAPER LOAD DECAL		
		7120-3570			RIBBON LOAD DECAL		
		7120-3571			ERROR NOTE DECAL, 9805A		
		7120-3627			ERROR NOTE DECAL, STAT		
		09805-90031			**SYSTEM TEST PROM**		

Table 7-2. Model 46 Replaceable Parts

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
A1		00046-66500			PC ASSY-MOTHER		
	C1	0180-2565		1	C-F: 3000 UF, 30V		
	C2	0180-0116		1	C-F: 6.8 UF, 35V		
	C3	0180-0228		2	C-F: 22 UF, 15V		
	C4	0180-1985		1	C-F: 500 UF, 30V		
	C5	0180-2187		1	C-F: 2500 UF, 15V		
	C6	0160-3847		8	C-F: .01 UF, 25V		
	C7	0160-0939		1	C-F: 430 PF, 300V		
	C8	0180-0228		2	C-F: 22 UF, 15V		
	C10-C13	0160-3847			C-F: .01 UF, 25V		
	C14	0180-1746		1	C-F: 15 UF, 20V		
	C16-C18	0160-3847			C-F: .01 UF, 25V		
	CR1	1906-0023		2	DIO: SI, 200V		
	CR2	1902-3139		2	DIO: BKDN 8.25V		
	CR3	1906-0023			DIO: SI, 200V		
	CR4	1901-0040		7	DIO: SI, .05A 30V		
	CR5	1902-3139			DIO: BKDN 8.25V		
	CR6,CR7	1901-0045		2	DIO: SI, .75A 100V		
	CR8	1901-0040			DIO: SI, .05A 30V		
	CR9	1902-3188		1	DIO: BKDN, 12.7V		
	CR10-CR13	1901-0040			DIO: SI, .05A, 30V		
	CR14,CR15	1910-0016		2	DIO: GE, 60V		
	CR16	1902-3128		1	DIO: BKDN, 7.32V		
	CR17	1901-0040			DIO: SI, .05A 30V		
	CR18	1902-0048		1	DIO: BKDN, 6.81V		
	J1	1200-0423		1	SOCKET-IC, 16 PIN		
	J2	1251-0526		1	CONN-10 PIN		
	Q1	1854-0063		1	TSTR: 2N3055		
	Q2-Q6	1854-0087		20	TSTR: SI, NPN		
	Q7	1853-0020		3	TSTR: SI, PNP		
	Q8-Q12	1854-0087			TSTR: SI, NPN		
	Q13	1853-0020			TSTR: SI, PNP		
	Q14-Q18	1854-0087			TSTR: SI, NPN		
	Q19	1853-0020			TSTR: SI, PNP		
	Q20	1854-0039		1	TSTR: SI, NPN		
	Q21	1854-0071		4	TSTR: SI, NPN		
	Q22-Q26	1854-0087			TSTR: SI, NPN		
	Q27	1853-0012		1	TSTR: 2N2904A		
	Q28	1854-0072		1	TSTR: 2N3054		
	Q29-Q31	1854-0071			TSTR: SI, NPN		
	R1,R2	0684-1031		11	R-F: 10K 10% ¼W		
	R5	0686-5115		1	R-F: 510 OHM 5%		
	R6	0684-2231		2	R-F: 22K 10% ¼W		
	R7	0684-5631		1	R-F: 56K 10% ¼W		
	R8	0684-2711		1	R-F: 270 OHM 10%		
	R9	0699-0003		1	R-F: 8.2 OHM 10%		
	R10,R11	0684-1031			R-F: 10K 10% ¼W		
	R12	0698-4445		1	R-F: 5.76K 1%		
	R13	0684-1021		2	R-F: 1K 10%		
	R14	0684-1031			R-F: 10K 10% ¼W		
	R15	0684-1021			R-F: 1K 10%		
	R16	0684-1031			R-F: 10K 10% ¼W		
	R17	0684-4721		2	R-F: 4.7K 10%		
	R18	0684-1031			R-F: 10K 10% ¼W		
	R19	0684-8211		1	R-F: 820 OHM 10%		
	R20	0684-3901		1	R-F: 39 OHM 10%		

Table 7-2. Model 46 Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	R21	0757-0410		1	R-F: 301 OHM 1%		
	R22	0684-1031			R-F: 10K 10% ¼W		
	R23	0684-2221		1	R-F: 2.2K 10%		
	R24	0684-1031			R-F: 10K 10% ¼W		
	R25	0684-4721			R-F: 4.7K 10%		
	R26	0684-2231			R-F: 22K 10% ¼W		
	R27	0684-1031			R-F: 10K 10% ¼W		
	R28	0684-3931		1	R-F: 39K 10% ¼W		
	R29	0684-1031			R-F: 10K 10% ¼W		
	R30,R31	0684-1041		2	R-F: 100K 10% ¼W		
	U1,U2	1820-0203		2	IC: OPR AMPL		
	U3	1820-0943		1	IC: CD 4023AE (CMOS)		
	U4,U5	1820-0946		5	IC: CD 4001AE (CMOS)		
	U6	1820-1127		1	IC: CLOCK DRIVER		
	U7	1820-0939		2	IC: CD 4013AE (CMOS)		
	U8-U10	1820-0946			IC: CD 4001AE (CMOS)		
	U11	1820-1169		1	IC: A&R		
	U12	1818-0078		1	IC: C&T		
	U13	1820-0994		1	IC: I/O PROCESSOR		
	U14	1820-0981		1	IC: DIGITAL (CMOS)		
	U15	1820-0993		1	IC: DATA STORAGE		
	U17	1818-0060		1	IC: ROM (4)		
	U18	1820-0939			IC: CD 4013AE (CMOS)		
	U23	1818-0087		1	IC: QUAD ROM (5-8)		
	U24	1818-0058		1	IC: QUAD ROM (0-3)		
	AX4	1251-2035		1	CONN-PC 30(2x15)		
		00046-69583		1	PRINTER-SEIKO (Rebuilt)		
		5040-7420		4	PAD-PRINTER SUPPORT		
A4		**00046-66540**		**1**	**PC BOARD-FATHER**		
	C1	0140-0235		1	C-F: 2250 PF, 300V		
	C2	0160-0207		1	C-F: .0I UF, 200V		
	C3	0150-0121		1	C-F: .1 UF, 50V		
	C4	0180-0374		1	C-F: 10 UF, 20V		
	CR1	1990-0410		1	DIO: LIGHT EMITTING (Busy)		
	L1	9100-1624		1	COIL-CHOKE, 30 UH		
	Q1, Q3	1854-0071		2	TSTR: SI, NPN		
	Q2	1853-0020		1	TSTR: SI, PNP		
	R1, R3	0683-5125		2	R-F: 5.1K, 5%		
	R2	0684-1011		1	R-F: 100 OHM, 10%		
	R4	0683-2015		1	R-F: 200 OHM, 5%		
	R5	0684-1021		1	R-F: 1K, 10%		
	R6	0683-1315		1	R-F: 130 OHM, 5%		
	U1	1820-0939		1	IC: CD 4013 AE (CMOS)		
	U2	1820-0943		1	IC: CD 4023 AE (CMOS)		
A5		**00046-66541**			**PC ASSY-DISPLAY**		
	C1	0160-0952		1	C-F: 220 PF, 300V		
	C2	0180-0106		1	C-F: 60 UF, 6V		
	C3	0160-3847		1	C-F: .01 UF, 25V		
	C4	0180-0309		1	C-F: 4.7 UF, 10V		
	CR1	1902-3085		1	DIO: BKDN, 4.75V		
	CR2	1990-0410		1	DIO: LIGHT EMITTING (Busy)		
	CR3	1902-3139		1	DIO: BKDN, 8.25V		

Table 7-2. Model 46 Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	CR4-CR6	1990-0335		3	DISPLAY, LED FAMILY		
		1990-0421*			DISPLAY; F INTENSITY		
		1990-0422*			DISPLAY; G INTENSITY		
		1990-0423*			DISPLAY; H INTENSITY		
		1990-0424*			DISPLAY; I INTENSITY		
		1990-0425*			DISPLAY; J INTENSITY		
		1990-0426*			DISPLAY; K INTENSITY		
	L1	9140-0129		1	L-F: 220 UH		
	L2-L7	9100-1639		7	COIL-CHOKE, 150 UH		
	L8	9140-0238		1	COIL-MLD CHOKE		
	L9	9100-1639			COIL-CHOKE, 150 UH		
	Q1-Q3	1854-0071		3	TSTR-SI, NPN		
	R1	0683-1315		1	R-F: 130 OHM, 5%		
	R2	0684-8201		1	R-F: 82 OHM, 10%		
	R3	0684-1011		1	R-F: 100 OHM, 10%		
	R4	0684-1021		1	R-F: 1K, 10%		
	R5	0684-1031		1	R-F: 10K, 10% ¼W		
	U1	1820-1029		1	IC: ANODE DRIVER		
	U2	1820-1226		1	IC: CATHODE DRIVER		
A7		**00046-67930**			**KEYBOARD ASSEMBLY**		
		00046-00130		1	PLATE-KEYBD		
		0380-0065		3	SPACER-CAPTIVE		
		0380-0945		4	STANDOFF		
		0380-1029		1	STDF-RIVET ON		
		09805-23701		1	SCREW-CAPTIVE		
	PS2	1251-3170		1	CONN-PLUG BODY		
		1460-0519		1	SPRING COIL		
		2260-0001		2	NUT HEX		
	S1	3101-1720		1	SWITCH-PUSHBUTTON		
		3101-1745		40	SWITCH-KEYBOARD		
		3101-1746		1	SWITCH-KEYBOARD		
		00046-61901		1	POWER SWITCH CABLE ASSY		
		00046-60301			**BACK PANEL ASSY**		
		00046-00201			BACK PANNEL		
	P1	1251-0525		1	CONNECTOR, ON/OFF CABLE		
	P2	1251-3169		1	CONNECTOR, XFORMER PWR		
	A1	5060-9422			POWER MODULE		
		7120-3664			PWR MOD. DECAL		
		8120-0593			SHIELDED CABLE		
		9100-3416			POWER TRANSFORMER		
		2200-0778		4	XFORMER SCREW		
		00046-64401			**TOP CABINET ASSY**		
		4040-0970			TOP CABINET		
		4040-0511			KEYBOARD PANEL		
		5040-7402			DISPLAY WINDOW		
		2200-0778		4	SCREW, COVER		
		7120-3628			NAME PLATE		

*See 'Introduction' in this chapter.

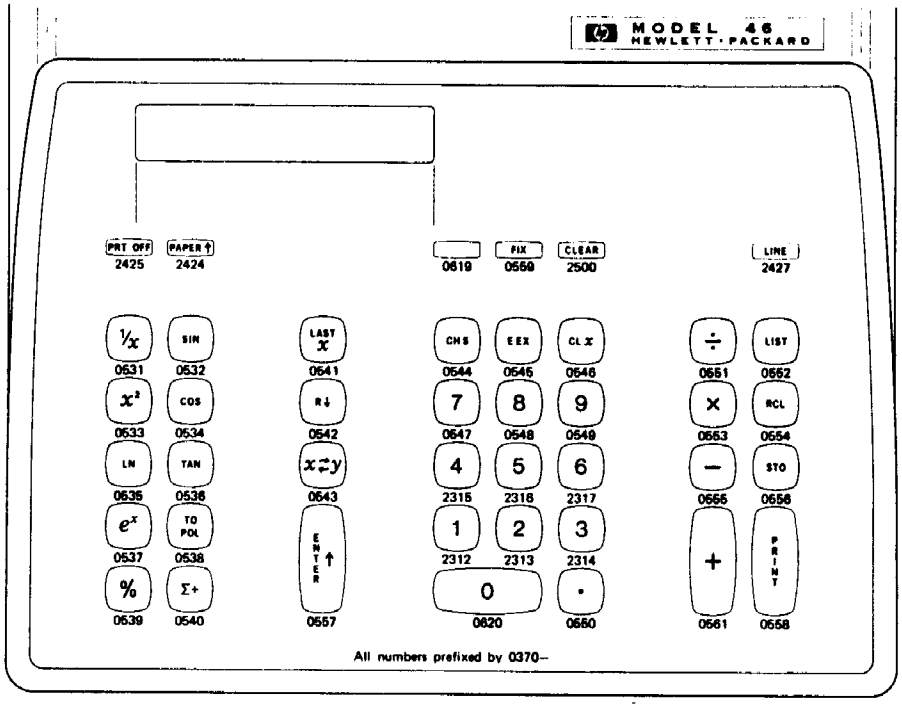


Figure 7-2. Model 46 Keycap Part Numbers

Table 7-3. Model 81 Replaceable Parts

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
A1	A1	00081-66500			PC ASSY-MOTHER		
	C1	0180-2565		1	C-F: 3000 UF, 30V		
	C2	0180-0116		1	C-F: 6.8 UF, 35V		
	C3	0180-0228		2	C-F: 22 UF, 15V		
	C4	0180-1985		1	C-F: 500 UF, 30V		
	C5	0180-2187		1	C-F: 2500 UF, 15V		
	C6	0160-3847		8	C-F: .01 UF, 25V		
	C7	0160-0939		1	C-F: 430 PF, 300V		
	C8	0180-0228			C-F: 22 UF, 15V		
	C10-C13	0160-3847			C-F: .01 UF, 25V		
	C14	0180-1746		1	C-F: 15 UF, 20V		
	C16-C18	0160-3847			C-F: .01 UF, 25V		
	CR1	1906-0023		2	DIO: SI, 200V		
	CR2	1902-3139		2	DIO: BKDN, 8.25V		
	CR3	1906-0023			DIO: SI, 200V		
	CR4	1901-0040		7	DIO: SI, .05A 30V		
	CR5	1902-3139			DIO: BKDN, 8.25V		
	CR6, CR7	1901-0045		2	DIO: SI, .75A 100V		
	CR8	1901-0040			DIO: SI, .05A 30V		
	CR9	1902-3188		1	DIO: BKDN, 12.7V		
	CR10-CR13	1901-0040			DIO: SI, .05A 30V		
	CR14, CR15	1910-0016		2	DIO: GE 60V		
	CR16	1902-3128		1	DIO: BKDN 7.32V		
	CR17	1901-0040			DIO: SI .05A 30V		
	CR18	1902-0048		1	DIO: BKDN 6.81V		
	J1	1200-0432		1	SOCKET - IC		
	J2	1251-0526		1	CONN-10 PIN		
	Q1	1854-0063		1	TSTR: 2N3055		
	Q2-Q6	1854-0087		20	TSTR: SI, NPN		
	Q7	1853-0020		3	TSTR: SI, PNP		
	Q8-Q12	1854-0087			TSTR: SI, NPN		
	Q13	1853-0020			TSTR: SI, PNP		
	Q14-Q18	1854-0087			TSTR: SI, NPN		
	Q19	1853-0020			TSTR: SI, PNP		
	Q20	1854-0039		1	TSTR: SI, NPN		
	Q21	1854-0071		4	TSTR: SI, NPN		
	Q22-Q26	1854-0087			TSTR: SI, NPN		
	Q27	1853-0012		1	TSTR: 2N2904A		
	Q28	1854-0072		1	TSTR: 2N3054		
	Q29-Q31	1854-0071			TSTR: SI, NPN		
	R1, R2	0684-1031		11	R-F: 10K, 10% ¼W		
	R5	0686-5115		1	R-F: 510 OHM, 5%		
	R6	0684-2231		2	R-F: 22K, 10% ¼W		
	R7	0684-5631		1	R-F: 56K, 10% ¼W		
	R8	0684-2711		1	R-F: 270 OHM, 10%		
	R9	0699-0003		1	R-F: 8.2 OHM, 10%		
	R10, R11	0684-1031			R-F: 10K, 10% ¼W		
	R12	0698-4445		1	R-F: 5.76K, 1%		
	R13	0684-1021		2	R-F: 1K, 10%		
	R14	0684-1031			R-F: 10K, 10% ¼W		
	R15	0684-1021			R-F: 1K, 10%		
	R16	0684-1031			R-F: 10K, 10% ¼W		
	R17	0684-4721		2	R-F: 4.7K, 10%		
	R18	0684-1031			R-F: 10K, 10% ¼W		
	R19	0684-8211		1	R-F: 820 OHM, 10%		

Table 7-3. Model 81 Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	R20	0684-3901		1	R-F: 39 OHM, 10%		
	R21	0757-0410		1	R-F: 301 OHM, 1%		
	R22	0684-1031			R-F: 10K, 10% ¼W		
	R23	0684-2221		1	R-F: 2.2K, 10%		
	R24	0684-1031			R-F: 10K, 10% ¼W		
	R25	0684-4721			R-F: 4.7K, 10%		
	R26	0684-2231			R-F: 22K, 10% ¼W		
	R27	0684-1031			R-F: 10K, 10% ¼W		
	R28	0684-3931		1	R-F: 39K, 10% ¼W		
	R29	0684-1031			R-F: 10K, 10% ¼W		
	R30, R31	0684-1041		2	R-F: 100K, 10% ¼W		
	U1, U2	1820-0203		2	IC: OPR AMPL		
	U3	1820-0943		1	IC: CD 4023AE (CMOS)		
	U4, U5	1820-0946		5	IC: CD 4001AE (CMOS)		
	U6	1820-1127		1	IC: CLOCK DRIVER		
	U7	1820-0939		2	IC: CD 4013AE (CMOS)		
	U8 thru U10	1820-0946			IC: CD 4001AE (CMOS)		
	U11	1820-1169		1	IC: A&R		
	U12	1818-0078		1	IC: C&T		
	U13	1820-0994		1	IC; I/O PROCESSOR		
	U14	1820-0981		1	IC: DIGITAL		
	U15, U16	1820-0993		2	IC: DATA STORAGE		
	U18	1820-0939			IC: CD 4013AE (CMOS)		
	U19	1818-0072		1	IC: QUAD ROM (20-23)		
	U20	1818-0071		1	IC: QUAD ROM (16-19)		
	U21	1818-0070		1	IC: QUAD ROM (12-15)		
	U22	1818-0069		1	IC: QUAD ROM (4-7)		
	U25	1818-0068		1	IC: QUAD ROM (0-3)		
	U26	1818-0067		1	IC: QUAD ROM (8-11)		
	XA4	1251-2035		1	CONN-PC 30(2x15)		
		5040-7420		4	PAD-PRINTER SUPPORT		
		7120-3638		1	LABEL (00081-66500)		
A4	**A4**	**00081-66540**		1	**PC BOARD-FATHER**		
	C1	0140-0235		1	C-F: 2250 PF, 300V		
	C2	0160-0207		1	C-F: .01 UF, 200V		
	C3	0150-0121		1	C-F: .1 UF, 50V		
	C4	0180-0374		1	C-F: 10 UF, 20V		
	CR1	1990-0410		1	DIO-LIGHT EMITTING (Busy)		
	L1	9100-1624		1	COIL-CHOKE, 30 UH		
	Q1, Q3	1854-0071		2	TSTR: SI, NPN		
	Q2	1253-0020		1	TSTR: SI, PNP		
	R1, R3	0683-5125		2	R-F: 5.1K, 5%		
	R2	0684-1011		1	R-F: 100 OHM, 10%		
	R4	0683-2015		1	R-F: 200 OHM, 5%		
	R5	0684-1021		1	R-F: 1K, 10%		
	R6	0683-1315		1	R-F: 130 OHM, 5%		
	U1	1820-0939		1	IC: CD 4013AE (CMOS)		
	U2	1820-0943		1	IC: CD 4023AE (CMOS)		
A5	**A5**	**00081-66541**			**PC ASSY-DISPLAY**		
	C1	0160-0952		1	C-F: 220 PF, 300V		
	C2	0180-0106		1	C-F: 60 UF, 6V		
	C3	0160-3847		1	C-F: .01 UF, 25V		
	C4	0180-0309		1	C-F: 4.7 UF, 10V		

Table 7-3. Model 81 Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	CR1	1902-3085		1	DIO: BKDN, 4.75V		
	CR2	1940-0410		1	DIO: LIGHT EMITTING (Busy)		
	CR3	1902-3139		1	DIO: BKDN, 8.25V		
	CR4-CR6	1990-0335		3	DISPLAY, LED **FAMILY**		
		1990-0421*			DISPLAY; F INTENSITY		
		1990-0422*			DISPLAY; G INTENSITY		
		1990-0423*			DISPLAY; H INTENSITY		
		1990-0424*			DISPLAY; I INTENSITY		
		1990-0425*			DISPLAY; J INTENSITY		
		1990-0426*			DISPLAY; K INTENSITY		
	L1	9140-0129		1	L-F: 220 UH		
	L2-L7	9100-1639		7	COIL-CHOKE, 150 UH		
	L2	9140-0238		1	COIL-MLD CHOKE		
	L9	9100-1639			COIL-CHOKE, 150 UH		
	Q1-Q3	1854-0071		3	TSTR: SI, NPN		
	R1	0683-1315		1	R-F: 130 OHM, 5%		
	R2	0684-8201		1	R-F: 82 OHM, 10%		
	R3	0684-1011		1	R-F: 100 OHM, 10%		
	R4	0684-1021		1	R-F: 1K, 10%		
	R5	0684-1031		1	R-F: 10K, 10% ¼W		
	U1	1820-1029		1	IC: ANODE DRIVER		
	U2	1820-1226		1	IC: CATHODE DRIVER		
A42		**00081-66542**			**KEYBOARD BUFFER, FATHER; Opt 002**		
		00081-61601			CABLE ASSY		
		1251-2615			RIBBON CONNECTOR; 16 PIN		
	C1	0160-0952		1	C-F: 220 PF, 300V		
	C2	0180-0106		1	C-F: 60 UF, 6V		
	C4	0180-0374		1	C-F: 10 UF, 20V		
	C6	0160-3517		1	C-F: .018 UF, 50V		
	CR1	1902-3085		1	DIO: BKDN, 4.75V		
	CR2	1990-0410		1	BUSY LIGHT		
	CR7	1901-0033		2	DIO: SI		
	CR8	1902-3128		1	DIO: BKDN; 7.32V, .05A		
	CR9	1902-3092		1	DIO: BKDN; 4.99V, 1%		
	CR11	1901-0033			DIO: SI		
	CR12-CR19	1910-0016		8	DIO: GE, 60V		
	L1	9140-0129		1	L-F: 220 UH		
	Q1-Q2	1854-0071		2	TSTR: SI, NPN		
	R2	0684-8201		1	R-F: 82 OHM, ¼W 10%		
	R3	0684-1011		1	R-F: 100 OHM, ¼W 10%		
	R4	0684-1021		1	R-F: 1K, ¼W 10%		
A42	R6-R10	0683-9135		5	R-F: 91K, ¼W 5%		
	R12	0683-1055		1	R-F: 1M, ¼W 5%		
	R13-R15	0683-3325		4	R-F: 3.3K, ¼W 5%		
	R16-R23	0683-1545		8	R-F: 150K, ¼W 5%		
	R24	0683-3325			R-F: 3.3K, ¼W 5%		
	R25	0683-3905		1	R-F: 39 OHM, ¼W 5%		
	U1	1820-1029		1	IC: ANODE DRIVER		
	U3	1820-0949		2	IC: CMOS NAND GATE, CD 4011AE		
	U4-U7	1820-0939		5	IC: CMOS D F-F, CD 4013AE		
	U8-U9	1820-0946		3	IC: CMOS NOR GATE, CD 4001AE		
	U10	1820-1145		2	IC: CMOS INVERTOR, CD 4049AE		
	U11	1820-0944		1	IC: CMOS, 3-INPUT NOR; CD 4025AE		
	U12	1820-0949			IC: CMOS NAND GATE, CD 4011AE		
	U13	1820-0939			IC: CMOS, D F-F, CD 4013AE		
	U14	1820-1174		1	IC: MOS 9X64 RAM BUFFER		

*See 'Introduction' in this chapter.

Table 7-3. Model 81 Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
	U15	1820-0958		1	IC: CMOS LATCH, CD 4042AE		
	U16	1820-0583		1	IC: TTL NAND GATE, DM 74L00		
	U17	1820-0947		1	IC: CMOS EXCL OR, CD 4030AE		
	U18-U20	1820-0948		3	IC: CMOS 4-INPUT NOR; CD 4002AE		
	U21	1820-1145			IC: CMOS INVERTOR, CD 4049AE		
	U22	1820-0946			IC: CMOS NOR GATE, CD 4001AE		
		1200-0473		1	SOCKET, IC		
		1251-1636		1	CONNECTOR, SINGLE CONTACT		
		7120-3632			LABEL, OPT I.D.		
A43		**00081-66543**			**BUFFERED KEYBOARD; DISPLAY Opt 003**		
		00081-61601			CABLE ASSY		
		1251-2615			RIBBON CONNECTOR; 16 PIN		
	C1	0160-0952		1	C-F: 220 PF, 300V		
	C2	0180-0106		1	C-F: 60 UF, 6V		
	C3	0160-3847		1	C-F: .01 UF, 25V		
	C4	0180-0374		1	C-F: 10 UF, 20V		
	C6	0160-3517		1	C-F: .018 UF, 50V		
	CR1	1902-3085		1	DIO: BKDN, 4.75V		
	CR2	1990-0410		1	BUSY LIGHT		
	CR3	1902-3139		1	DIO: BKDN, 8.25V		
	CR4-CR6	1990-0335		3	DISPLAY LED, **FAMILY**		
		1990-0421		*	DISPLAY; F INTENSITY		
		1990-0422		*	DISPLAY; G INTENSITY		
		1990-0423		*	DISPLAY; H INTENSITY		
		1990-0424		*	DISPLAY; I INTENSITY		
		1990-0425		*	DISPLAY; J INTENSITY		
		1990-0426		*	DISPLAY; K INTENSITY		
	CR7	1901-0033		2	DIO: SI		
	CR8	1902-3128		1	DIO: BKDN; 7.32V, .05A		
	CR9	1902-3092		1	DIO: BKDN; 4.99V, 1%		
	CR11	1901-0033			DIO: SI		
	CR12-CR19	1910-0016		8	DIO: GE, 60V		
	L1	9140-0129		1	L-F: 220 UH		
	L2-L7	9100-1639		7	L-F: 150 UH		
	L8	9140-0238		1	L-F: MLD CHOKE; 150 UH		
	L9	9100-1639			L-F: 150 UH		
	Q1-Q3	1854-0071		3	TSTR: SI, NPN		
	R1	0683-1315		1	R-F: 130 OHM, ¼W 5%		
	R2	0684-8201		1	R-F: 82 OHM, ¼W 10%		
	R3	0684-1011		1	R-F: 100 OHM, ¼W 10%		
	R4	0684-1021		1	R-F: 1K, ¼W 10%		
	R5	0684-1031		1	R-F: 10K, ¼W 10%		
A43	R6-R10	0683-9135		5	R-F: 91K, ¼W 5%		
	R12	0683-1055		1	R-F: 1M, ¼W 5%		
	R13-R15	0683-3325		4	R-F: 3.3K, ¼W 5%		
	R16-R23	0683-1545		8	R-F: 150K, ¼W 5%		
	R24	0683-3325			R-F: 3.3K, ¼W 5%		
	R25	0683-3905		1	R-F: 39 OHM, ¼W 5%		
	U1	1820-1029		1	IC: ANODE DRIVER		
	U2	1820-1226		1	IC: CATHODE DRIVER		
	U3	1820-0949		2	IC: CMOS NAND GATE, CD 4011AE		
	U4-U7	1820-0939		5	IC: CMOS D F-F, CD 4013AE		
	U8,U9	1820-0946		3	IC: CMOS NOR GATE, CD 4001AE		

*See 'Introduction' in this chapter.

Table 7-3. Model 81 Replaceable Parts (Cont'd)

	REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO
	U10	1820-1145		2	IC: CMOS INVERTOR, CD 4049AE		
	U11	1820-0944		1	IC: CMOS, 3-INPUT NOR; CD 4025AE		
	U12	1820-0949			IC: CMOS NAND GATE, CD 4011AE		
	U13	1820-0939			IC: CMOS D F-F, CD 4013AE		
	U14	1820-1174		1	IC: MOS 9X64 RAM BUFFER		
	U15	1820-0958		1	IC: CMOS LATCH, CD 4042 AE		
	U16	1820-0583		1	IC: TTL NAND GATE, DM 74L00		
	U17	1820-0947		1	IC: CMOS EXCL. OR, CD 4030AE		
	U18-U20	1820-0948		3	IC: CMOS 4-INPUT NOR; CD 4002AE		
	U21	1820-1145			IC: CMOS INVERTOR, CD 4049AE		
	U22	1820-0946			IC: CMOS NOR GATE, CD 4001AE		
		1200-0473		1	SOCKET, IC		
		1251-1636		1	CONNECTOR, SINGLE CONTACT		
		7120-3631			LABEL, OPT I.D.		
A7		**00081-67930**			**KEYBOARD ASSEMBLY**		
		00081-64401			TOP CABINET ASSY		
		2200-0778		4	SCREW, MACHINE-PRINTER		
		4040-0511			KEYBOARD PANEL		
		5040-7402			DISPLAY WINDOW		
		7120-3629			FRONT NAMEPLATE		
		00081-69564		1	PRINTER, SEIKO; (Rebuilt)		
		00081-00130		1	PLATE-KEYBOARD		
		00081-26530		1	PC BD KEYBOARD		
		0380-0065		3	SPACER-CAPTIVE		
		0380-0945		4	STANDOFF		
		0380-1029		1	STANDOFF RIVET ON		
		09805-23701		1	SCREW-CAPTIVE		
	PS2	1251-3170		1	CONN-PLUG BODY		
		1460-0519		1	SPRING COIL		
		2260-0001		2	NUT-HEX		
	S1	3101-1720		1	SWITCH PUSHBUTTON		
		3101-1745		40	SWITCH-KEYBOARD		
		3101-1746		2	SWITCH-KEYBOARD		
		00081-61901		1	POWER SWITCH CABLE ASSY		
					MISCELLANEOUS		
		09805-90031			SERVICE PROM		
		00081-90032			SERVICE TEST CASSETTE		
		11369A			MODELS 46 & 81 OPT 001 ACCESSORY		
		11370A			MODEL 81 OPT 002 ACCESSORY		
		11371A			MODEL 81 OPT 003 ACCESSORY		
		09805-90030			9805A ON-SITE SERVICE MANUAL		
		00046-90032			MODELS 46 & 81 ON-SITE SERVICE MANUAL		
		09805-90029			MODELS 46 & 81, AND 9805A REPAIR MANUAL		
		09805-90010			ET 7083 OPERATING & SERVICE MANUAL		
		00081-90030			ET 7074 OPERATING & SERVICE MANUAL		

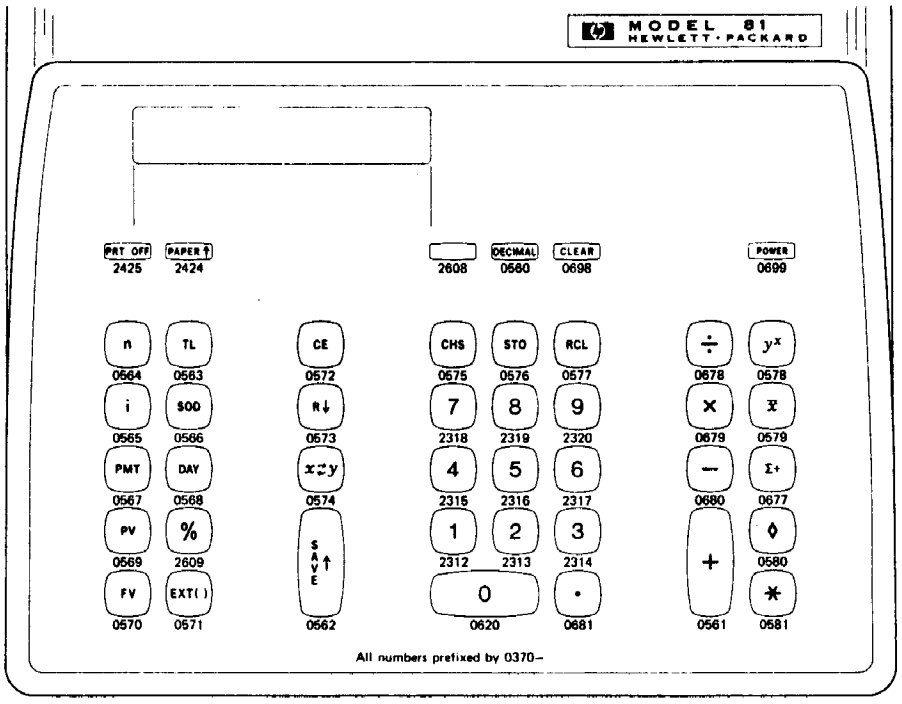


Figure 7-3. Model 81 Keycap Part Numbers