The Data Storage Circuit - 1820-0993 for Use with the HP-35 Processor

General Description

The data storage circuit contains ten 56 bit shift registers and miscellaneous logic on a 158 mil by 149 mil chip. The MOS process used is P-channel with ion implantation.

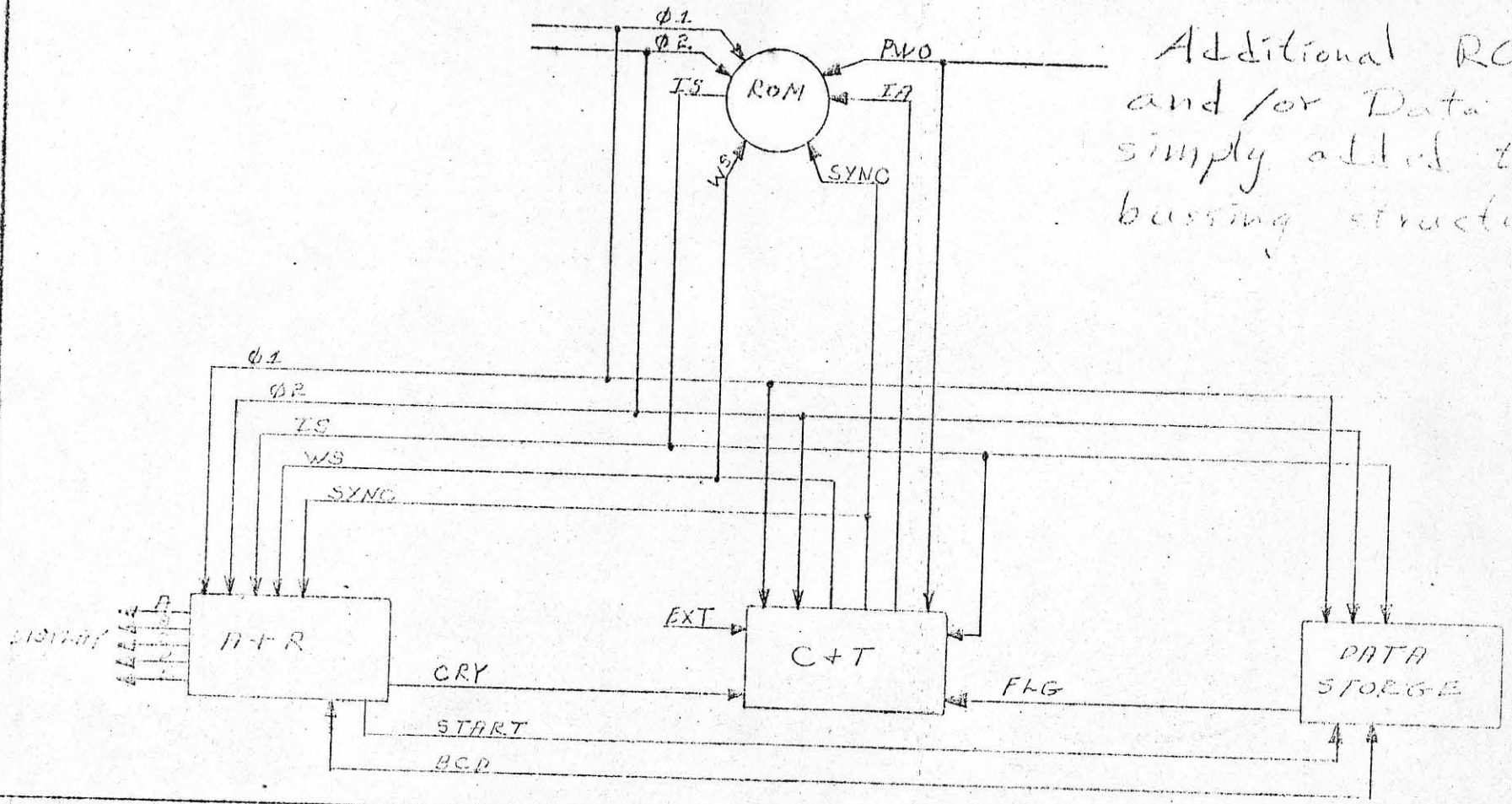
The availability of ten or more data storage registers for use by the A & R chip greatly increases the scope of problems solvable with the HP-35 Processor. Up to three Data Storage Chips can be tied directly to the A & R chip, which fixes a maximum of 30 registers. If a bi-directional buffer is placed between the A & R and the Data Storage Chips, then up to 25 units can be paralleled, giving a maximum of 250 registers.

Figure 1 illustrates how the Data Storage Chip fits into the processor circuits.

The timing between the Data Storage Chip(s) and the CPU is taken care of by the START line from the A & R chip and the "ROM is present" pulse that occurs on the Is line at bit time 11.

Data is transferred to the Data Storage Chip from the A & R chip via the BCD line. This data is either read as a register address or as a data word to be stored. The BCD line is bi-directional and is also to transfer data words to the A & R chip.

M	REVISIONS	APPROVED	DAT



Additional ROM's and/or Data Storage simply added to the bussing structure.

ENG. RESP. — DIV.	ITEM	QTY	DESCRIPTION	PART NO.	DWG. NO.	MAT'L SPEC.
UNLESS OTHERWISE NOTED — TOLERANCES — 0.XX ±0.02 0.XXX ±0.005 ANGULAR ± MACHINED SURFACES 63 — DO NOT SCALE —						

DRAWN	DATE	TITLE		
J.A. REA	10-9-72	Processor with Data Storage		HEWLETT hp PACKARD
ENGINEER Don Morris	10-10-72			LABORATORY INSTRUMENTS
APPROVED				NEXT ASSY.
SUPERSEDES		FINISH	SCALE	A - - -

PRINTED ON DIEPO 1020-10

There are three instructions recognized by the Data Storage Chip, which are received directly from the ROMs via the Is line. These instructions are:

ATDS: Address from C register to Data Storage
DTDS: Data from C register to Data Storage
DSTC: Read from D.S. into C register

The contents of the C register is continuously being displayed on the BCD line, except when one of the "Data into C register" instructions is executed. DSTC is one of these instructions. Therefore, it can be seen that the instructions ATDS and DTDS are ignored by the CPU (and the I/O chip if one is used) and are decoded and executed by any Data Storage Chip in the system. The instruction DSTC is executed by the A & R and any Data Storage Chip which has previously been enabled. The "enabling" of a chip is covered in the next section.

Register Addressing

When a data transfer command occurs, either DTDS or DSTC, the command will only be executed if and only if there exists at least one data storage register which has previously been enabled. Once enabled, a register will remain enabled until another ATDS is given which addresses a different register.

The numbering of each register is done in two portions. Internally, the registers are numbered 0,1, ... 8,9. The chips themselves are numbered 0,1,... 62, 63. The actual chip number, assigned to given unit, is determined externally to the chip. The coding for all 64 combinations is allowable for any chip, therefore there will not be a whole family of different chips to be used. The chip address inputs are:

B1 Least significant bit
B2
B3
B4
A1
A2 Most significant bit

If B1, B2, B3 and B4 is taken as a hexadecimal number, then only ten of the sixteen combinations are legal BCD characters. As far as the D.S. Chip is concerned, all are legal. Normal addresses are those utilizing the ten legal BCD codes for the number "B". The special addresses are the remaining unused combinations. Normal register addresses will be given by $0 \leq D_3 D_2 D_1 \leq 399$ where all three digits are legal BCD numbers.

If D_2 is restricted to the hexadecimal numbers ten through sixteen then 240 special addresses are available. These addresses are not readily generated by the HP-35 Processor.

In order to "tell a Data Storage Chip its address" it is necessary to enter the binary (or BCD) code of the appropriate chip number into the A and B inputs. For example, to establish the register addresses for a chip as 130 through 139 would mean that the chip should be identified as chip 13. The code (BCD) for 13 is 01 0011.
Therefore:

A2 = 0 = 0 volts
A1 = 1 = 6 volts
B4 = 0 = 0 volts
B3 = 0 = 0 volts
B2 = 1 = 6 volts
B1 = 1 = 6 volts

The address decoding logic of the Data Storage Chips is capable of handling floating point addresses. Under certain special conditions, these addresses need not be normalized.

In order for an address to be legally accepted by a Data Storage Chip the exponent must be +0, +1 or +2. Due to an error in logic design, an exponent of +3 must not be given, because the logic would then enable chip zero, register zero. Except for addresses with an exponent of +3, all illegal addresses will be indicated by the Data Storage Chip(s) as either an illegal address or the address of a register not found (see next section).

The sign of the mantissa is always ignored by the Data Storage Chips. Also, the addresses are truncated to the next lower whole number. For example, the numbers:

-3.79

3.1854

+3.00

-3.00

would, as addresses, enable register three.

If an exponent of zero is given, then only the most significant digits of the mantissa will be interrogated to determine a register number ranging from 0 → 9.

If an exponent of +1 is found, then the two most significant digits of the mantissa are interrogated to determine a register number in the range 0 → 99; being as 0 → 9 is included in this field, then these numbers are not strictly required to be normalized.

When an exponent of +2 is encountered in an address, the three most significant digits of the mantissa, are interrogated and checked for a number in the range 0 → 399. Obviously, the numbers in the range 0 → 99 would not have been normalized.

Data Storage Flags

When an address is given (ATDS) and that address is legal and exists (some register was actually enabled), then a flag is generated by the chip which contains the enabled register. This feature can be ignored by simple leaving the flag output unused. For one to three registers, these flag lines can be hooked directly to the flag input of the Control and Timing chip. If more than three Data Storage Chips are tied to the flag input of the C & T, then the flag output of the I/O chip (1820-0994) must be used. The I/O chip has a gated pull-down device that can turn-off the additional capacitance of the Data Storage Chips

Use of a Bi-Directional Buffer

If more than three Data Storage Chips are to be used in a system, then the A & R chip BCD driver is unable to handle the capacitive load. In this case a bi-directional amplifier is required. A sample amplifier is shown in Figure 2. In order to control the "direction" of this amplifier a steering signal is required. This is supplied by the Data Storage Chips themselves, by the BDE output. Each chip will recognize the command DSTC independently of whether or not it was enabled.

BDE $\geq$ 6 volts $\geq$ DSTC

BDE $\leq$ 0 volts $\geq$ Data Storage is listening

Using Data Storage Instructions

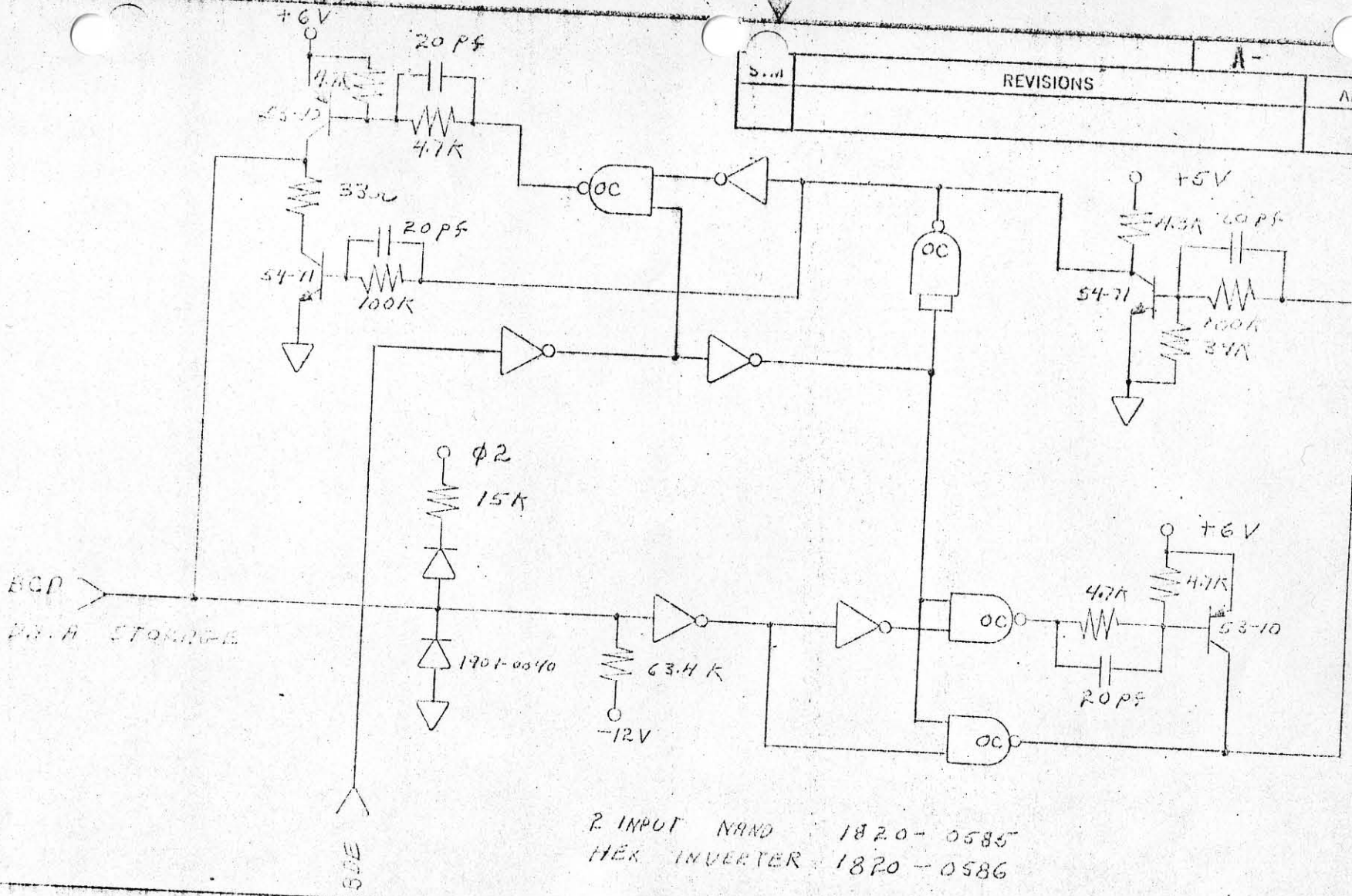
The bit patterns for the three instructions are:

ATDS = 1001110000

DTDS = 1011110000

DSTC = 1011111000

The desired address for a register should be placed in the C-register of the A & R, and then ATDS given. The enabled register will remain enabled until another ATDS is given. Neither of the data transfer instructions can follow an ATDS instruction directly, at least one other instruction must be executed. This instruction might or might not be a NOP.



2 INPUT NAND 1820-0585
HEX INVERTER 1820-0586

REVISIONS	APPROVED	DATE

ENG. RESP. — DIV. _____

UNLESS OTHERWISE NOTED
— TOLERANCES —
0.XX ±0.02 0.XXX ±0.005
ANGULAR ± _____
MACHINED SURFACES 63
— DO NOT SCALE —

ITEM	QTY	DESCRIPTION	PART NO.	DWG. NO.	MAT'L SPEC.

DRAWN J. A. REA — DATE 10-10-72
ENGINEER Don Morris — 10-10-72
APPROVED
SUPERSEDES

TITLE
BCD BIDIRECTIONAL BUFFER

FINISH
SCALE

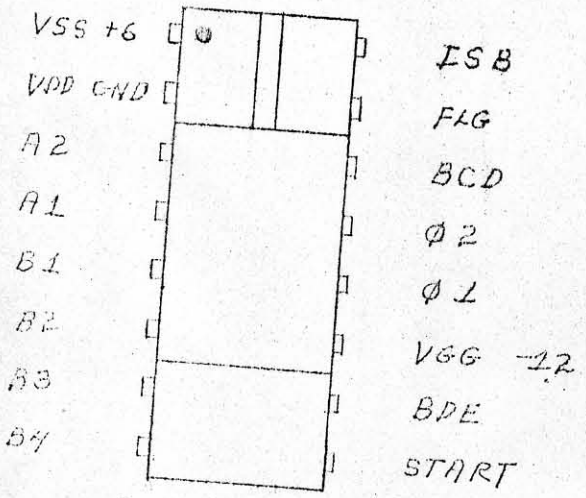
HEWLETT-PACKARD
LABORATORY INSTRUMENTS

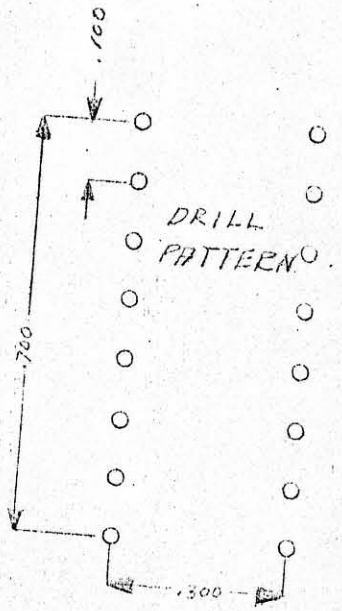
NEXT ASSY.

A -

PRINTED ON DITTO 1025-10

SYM	REVISIONS	APPROVED





ENG. RESP. — DIV.					
UNLESS OTHERWISE NOTED — TOLERANCES — 0.XX ±0.02 0.XXX ±0.005 ANGULAR ± MACHINED SURFACES 63 — DO NOT SCALE —	ITEM	QTY	DESCRIPTION	1820-0773 PART NO.	DWG. NO. / MAT'L SPEC.
	DRAWN T. A. REA	DATE 10-9-72	TITLE DATA STORAGE		
	ENGINEER Don Morris	10-10-72			
	APPROVED				
	SUPERSEDES		FINISH		

HEWLETT hp PACKARD

LABORATORY INSTRUMENTS

MOSTEK

2-1-72

DATA STORAGE CIRCUIT

ELECTRICAL SPECIFICATIONS

Preliminary Spec's Only

Absolute Maximum Ratings

Supply Voltage V_{DD} ..... V_{ss} -10.0V

Supply Voltage V_{GG} ..... V_{ss} -21.0V

Voltage at any input or output ..... V_{ss} +0.3V to V_{ss} -10V

Operating free-air temperature range ..... 0 °C to 65 °C

Storage temperature range ..... -55 °C to 125 °C

Humidity ..... 0 to 90%

	PARAMETER		MIN	MAX	UNIT	COMMENTS
Power Supply	V_{DD}	Supply Voltage	0.0	0.0	V.	
	V_{ss}	Supply Voltage	+5.0	+7.0	V.	Supply Voltages do not necessarily track
	V_{GG}	Supply Voltage	-10.0	-14.0	V.	
	I_{DD}	Supply Current (V_{DD})	-	TBD	mA	→ 1.3 @ 70°; 1.8 @
	I_{GG}	Supply Current (V_{GG})	-	TBD	mA	→ 2.4 @ 70°C; 2.73 @
	P_T	*Total Chip Power	-	~~30~~ P ≥ 71	mW	At 0 °C with max voltages and max frequenc
External Clock Description	$V_\phi(0)$	Clock "0" level	V_{ss}-.8	V_{ss}	V	
	$V_\phi(1)$	Clock "1" level	V_{GG}	V_{GG}+.7	V	
	f	Operating Frequency	50	210	KC	
	tpw	Clock Pulse Width	625	1000	ns	See Timing Diagram
	t_d	Clock Delay Time	625	1000	ns	Figure 1
	t_{rt}	Clock Pulse Rise Time	50	150	ns	
	t_{ft}	Clock Pulse Fall Time	50	150	ns	

*This spec is a design goal.

	PARAMETER		MIN	MAX	UNIT	COMMENTS
Input Description (Note 1)	$V_{in}(0)$	Input Voltage-Logic "0"	V_{ss}-1.0	V_{ss}+.3	V.	See Figure 2
	$V_{in}(1)$	Input Voltage-Logic "1"	-	V_{ss}-4.0	V.	
	t_{in}	Time at which input data is valid (before the ϕ1 clock)				See Timing Diagram Figure 1
		Inputs: Start	.250		µs	
		ISB	0.0		µs	
		A1, A2	3.0		µs	
		B1, B2, B3, B4	3.0		µs	
		BCD	0.0		µs	
	C_{in} *	Input Capacitance				
		Inputs: ϕ1		20	pf	
		ϕ2		20	pf	
		Start		6	pf	
		ISB		5	pf	
		A1, A2		5	pf	
		B1, B2, B3, B4		5	pf	
		BCD		10	pf	
Output Description (See Note 3)	FLG OUTPUT					See Figure 3
	$V_{out}(0)$	Logical "0" output Voltage	Open Source		V	The "Flg" output is implemented using an open source buffer capable of driving the load to an MOS "1" level but presenting a high impedance (floating output) during the "0" state.
	$V_{out}(1)$	Logical "1" output Voltage		V_{ss}-4.5	V	
	$t_{dv}(1)$	Time from Bit Time 2 at which "1" level data is valid		12	µs	
	I_{sink}	DC current load during the "1" state		1.0	mA	
	C_L	Capacitive load		300	pf	
	BDE OUTPUT					See Figure 4
	$V_{TTL}(0)_{out}$	Logical "0" output Voltage	V_{DD}+2.4		V.	The "BDE" output is implemented using a push pull low-power-TTL compatible output buffer.
	$V_{TTL}(1)_{out}$	Logical "1" output Voltage		V_{DD}+.3	V.	
	t_{dv}	Time at which output data is valid		2.5	µs	$V_{out}(0)$, t_{dv}, I_{source} and R_s values are valid only when device is operated with $5.6 \leq V_{ss} \leq 6.5V$.
	I_{sink}	DC current load during the "1" state		360	µA	

*This spec is a design goal

	PARAMETER		MIN	MAX	UNIT	COMMENTS
Output Description (continued)	I_{source}	DC current load during the "0" state		50	µA	
	C_L	Capacitance load		30	pf	
	R_s	Buffer output resistance during a "0" state output	1.5	-	K Ω	
	BCD OUTPUT					See Figure 5
	$V_{out}(0)$	Logical "0" Output Voltage	V_{ss}-.5			The "BCD" output is implemented using a pr charge load device capable of pre-chargin to a "1" level all int nal and pin capacitanc and a driver capable o discharging a 400 pf load to an MOS "0" level.
	$V_{out}(1)$	Logical "1" Output Voltage		V_{ss}-4.5		
	t_{dv}	Time at which output is valid		3.3	µs	
	C_L	Capacitive load		400	pf	

TES:

1. All device pads will be provided with static discharge protection devices. In addition, inputs ISB, Start, A1, A2, B1, B2, B3 and B4 will be protected as per the requirements of Appendix C (Static Gate Protection Requirements).

2. All logic levels referred to within this document are negative logic levels:

   "0" level = High Voltage

   "1" level = Low Voltage

3. All output buffers will be provided with internal test points which when externally forced to V_{DD} will cause the buffer to go into a high output impedance state (floating output). Test pad size: 1 X 1 millinch (Gate protection cannot be provided on these test points.)

4. The logic design of the Data Storage Circuit requires that for proper input or output of data on the BCD line, instruction types I_2 or I_3 must not directly follow an I_1 instruction on the ISB line.

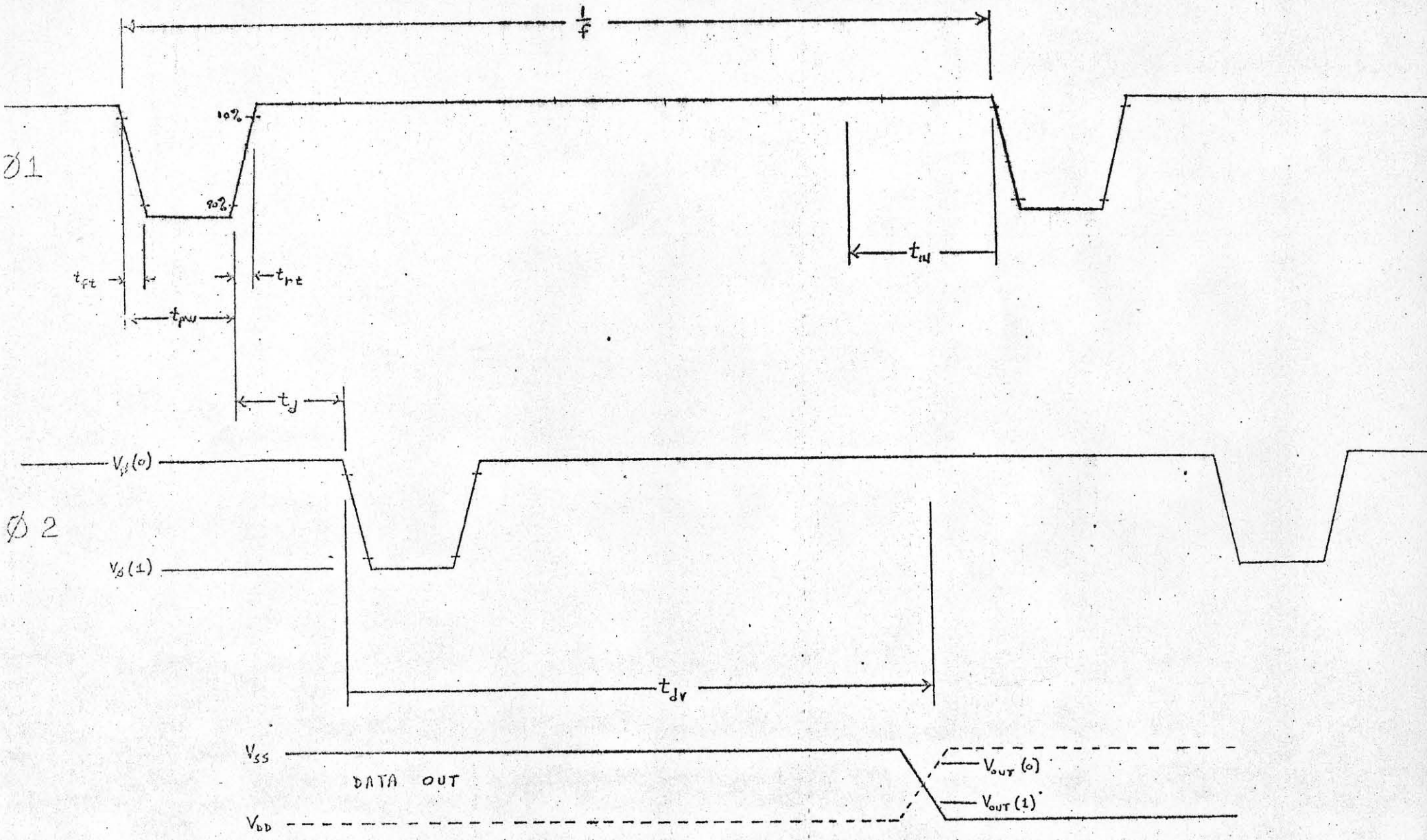


FIGURE I

TIMING DIAGRAM

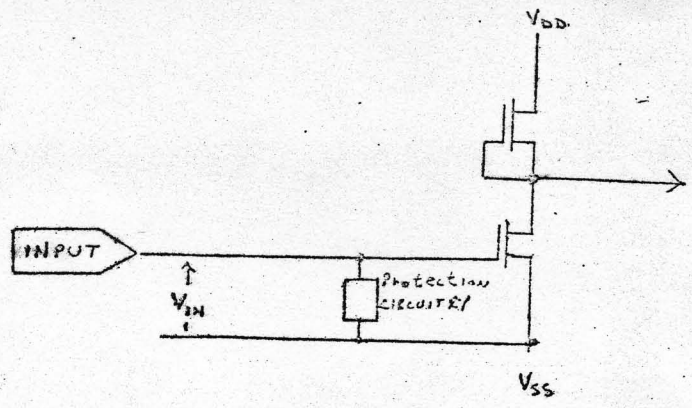


Figure 2

Typical Input Circuit

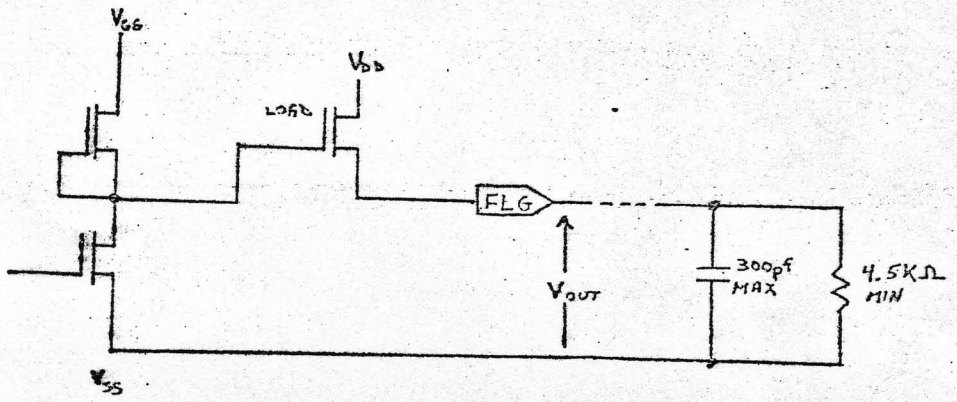


Figure 3

"FLG" Output Buffer

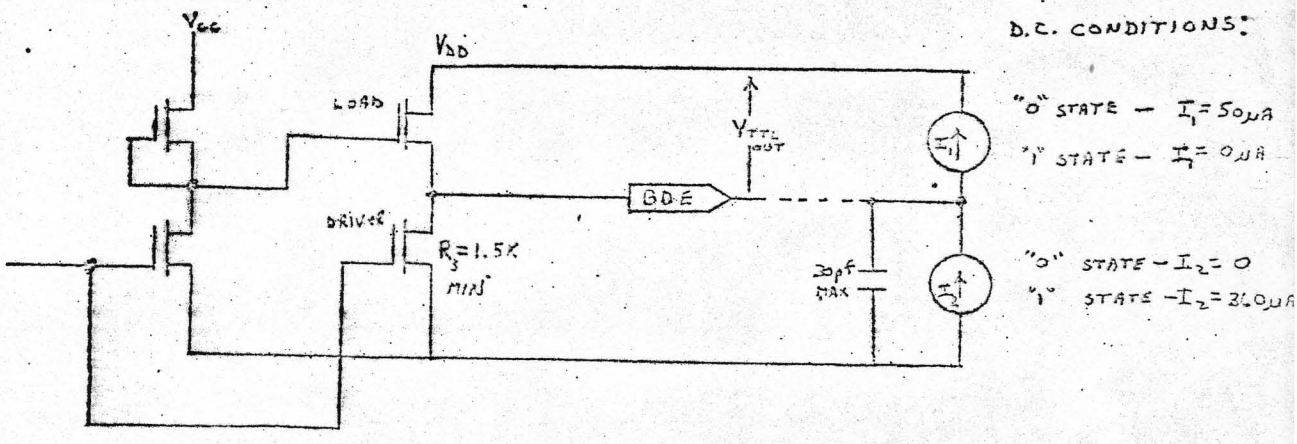


Figure 4

"BDE" Output Buffer

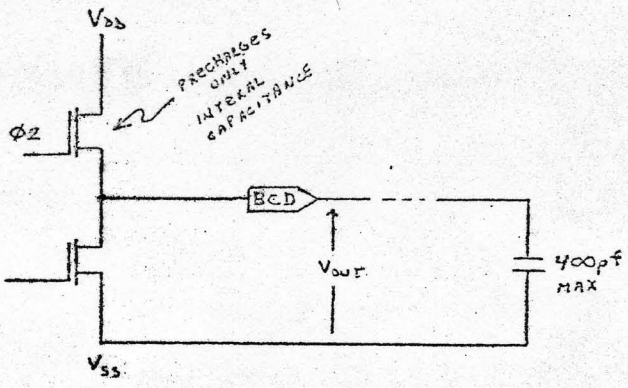


Figure 5

BCD Output Buffer