Don Morris
11-17-72

I/O and Binary Processor Chip

1820-0994

LIO n

GENERAL DESCRIPTION

The I/O and binary processor chip was designed to implement several functions in conjunction with the processor and ROM circuits developed for the HP-35A. This circuit is basically an I/O chip for the other processor chips; also included, though, is the ability to do binary arithmetic and drive a Seiko Model 102 printer.

In order to describe the operation of this device, the instructions capable of being performed will be described sequentially. The circuitry of the chip will be described only as needed to explain the particular instructions under consideration.

INSTRUCTION SET SWITCHING

In order to implement this circuit, more instructions were needed than were available in the instruction set of HP-35A processor. Therefore, an instruction set switching scheme is utilized.

The I_S lines of the ROMs are tied directly to the I_S input of the I/O chip. Coming from the I/O chip is a signal called "EISI." When EISI~6v. the I_S lines of the ROM's are fed to the I_S line going to the C & T and A & R chips. When EISI~0v., the I_S line going to the C & T and A & R chips is held low (given NOP's). Therefore, if EISI is low the I/O chip is able to be given instructions with the same bit patterns as used normally by the regular processor chips.

The I/O chip doesn't try to execute instructions in the main (ISI) instruction set. This is accomplished by the fact that the I/O chip "remembers" which instruction set it is in. The power-on (PWO) input to the I/O chip insures that the I/O chip always powers up into the main instruction set (IS1).

ISI	1001000000	All
IS2	0101000000	All
IS3	1101000000	All

ISI:Enable ISI
IS2:Enable IS2
IS3:Enable IS3

When ISI is executed, the internal IS2 instruction qualifier flip-flop is "reset." which implies that EISI will go high and the I/O chip will only accept those instructions classified as "ALL." "ALL" means that the given bit pattern means the same thing in all instruction sets.

When IS2 is executed, EISI will go low and the IS2 instruction qualifier flip-flop will be "set." The execution of an IS3 instruction will cause EISI to go low and the IS2 qualifier to be reset. IS3 is not utilized at present, but could be used to extend the instruction set for use by another, as yet undefined, purpose.

DATA TRANSFER AND BINARY ARITHMETIC:

The I/O chip contains a 56 bit shift register, this data register is called the T-register. The data transfer commands are:

TTC	T → C, T unchanged
CTT	C → T, C unchanged

The bit-by-bit binary operators are:

XOR	Exclusive OR, T⊻C → T
IOR	Inclusive OR, T∨C → T
AND	Logical AND, T∧C → T

The binary word operators are:

ADD	Binary Add T⊕C → T
SLT	Shift T-reg. left one bit
SRT	Shift T-reg. right one bit
TINC	Increment T by one (binary)
TDEC	Decrement T by one (binary)
YBC	Interrogate Binary Carry

When either ADD or TINC are executed, it is possible for a carry beyond the word to be generated. If such a carry is generated, and if the second instruction following the original ADD or TINC is a YBC then status bit 11 will be set.

Example:

```
IS2
ADD
NOP
YBC
IS1
 :
```

If a carry was generated, then status bit 11 of the C & T will have been set. The carry is available only for YBC at the time shown, afterwards the information is unavailable. The NOP could be any instruction except IS1 or IS3.

If TDEC is executed when the contents of the T-register is zero, then a borrow outside the word will result. The flag sense of the TDEC "borrow" is opposite to that of a carry.

The two possibilities are:

1) T-register = 0

```
IS2
TDEC
NOP
YBC
 :
```

Status bit 11 will <u>not</u> be set by this operation.

2) T-register ≠ 0

```
TDEC
NOP
YBC
 :
```

Status bit 11 will be set.

A useful method of testing T = 0 for any binary word in T is:

```
IS2
TDEC
TINC
YBC
IS1
BRN      (→T = 0)
RS11
 ↓
(T ≠ 0)
```

Note that the contents of "T" has not been modified.

THE PROGRAM COUNTER (P-REGISTER):

There is a fourteen bit register in the I/O chip which can be used for data storage for such uses as a program counter. Therefore, it is designated as the "P-register." The fourteen least significant bits in the T-register can be loaded into the P-register (TTP), without changing the contents of the T-register. The contents of the P-register can be loaded into the fourteen least significant bits of the T-register with the instruction "PTT." In this case, the forty-two most significant bits of the T-register and the contents of the P-register are unchanged.

The instruction "PINC" performs a binary increment of the number stored in the P-register. Not only is the incremented binary number placed in the P-register, but also the ten least significant bits of the incremented number is loaded sequentially on the output lines C9 through C18. The instruction "PDEC" is similar to PINC except that the binary number stored in the P-register is decremented by one. The commands PINC and PDEC have a common restriction; that is, that if the number exceeds 1,023 (represented in binary) the number displayed on the lines C9 through C18 will not only have a insufficient number of bits, but also the bit displayed on C18 will always be a logic "1."

SRI
LIO

DATA INPUT:

The parallel data output lines C1 through C18 are low power TTL compatible if V_{SS} for the I/O chip is in the range of 5.6 to 6.5 volts. The outputs C9 through C18 are outputs only, whereas the lines C1 through C8 are for either output or input.

There is an input on the I/O circuit called "LATCH"; this input when held at V_{SS} ($\approx$ 6v.) will cause C1 through C8 to be outputs. If LATCH is pulled low (within 0.8 volts of V_{DD}) the internal pull-up resistors on C1 through C8 will be turned on. Also, the data found on C1 through C8 when LATCH is held low is transferred into the output buffer register. After releasing LATCH the data loaded will remain as an output on C1 to C8.

Data should not be forced onto C1 to C8 until at least three bit times after LATCH is pulled. The LATCH pulse must be at least three bit times long, it need not be synchronous with the system clocks. Data can be forced onto C1 through C8 after LATCH is released because the internal data would be the same as the external data. LATCH requires an external pull-up resistor.

The data in the low eight significant bits of the I/O register (C1 through C8) can be operated on by two different instructions, "EERA" and "IXT." The instruction EERA is understood by both the Control and Timing circuit and the I/O circuit. When the instruction EERA is executed the eight bit word in the I/O register, bits C1 through C8, is sent serially out the EXT output of the I/O circuit and in the same time slot as the addresses are sent to the ROM's. The C & T circuit recognizes the EERA command and transfers the data from its EXT input to its 1A output. In this way, the next ROM address is obtained from the I/O register. After executing EERA bits C1 through C8 will contain the same data (either zeros or ones) as in C9.

The instruction IXT exchanges the lowest eight significant bits of the I/O register, C1 to C8, with the eight most significant bits of the T-register. All the remaining bits of the T-register and the I/O register are left unchanged.

EERA	0001010000	1
IXT	0100101000	2

PRINTER COMMANDS:

The I/O circuit contains logic and memory for driving the Seiko Model 102 digital printing head. This printer has eighteen columns and a choice of thirteen characters per column. This printer has a rotating print drum with thirteen sectors (0-12). Two timing signals are required from the printer as positive true signals, TP and TR. These two signals should be clocked with phase two of the clocks.

There are five instructions which are directly associated with the printer. These are:

CCS: Compare C-register with sector counter
TCS: Compare T-register with sector counter
PRE: Printer Enable
ADV: Paper Advance (also disables printer)
RED: Prepare for Red Print

During operation of the machine the print drum in continually rotating, the current sector of the printer is maintained by the sector counter of the I/O circuit. While the printer is enabled (following PRE until the next ADV instruction) the end of each sector is marked by a flag pulse which sets status bit 11 in the C & T circuit.

The method of obtaining a print begins with the construction of a printer mask in the C-register and the T-register. The columns 1 through 14 of the printer (right to left) are printed according to the data in the C-register. Each digit position is filled with a hexadecimal number (0 through 15) which represents the sector to be printed. A hexadecimal 13, 14 or 15 will leave a blank in the given column position. Printing is easier to accomplish when the numeric entries on the drum coincide with their respective sector number. The least significant four digits of the T-register are loaded in like manner for columns 15 through 18.

If a red print is desired, then the command "RED" should precede the print subroutine. The RED command shifts the ribbon into the red printing position. The ribbon will remain in that position until a paper advance occurs. The following print subroutine can be varied so long as the basic timing structure (with respect to the returning flags) remains constant. This routine assumes

that the data words in the C-register and T-register has previously been constructed. Note that the paper advance command ADV is the only method of terminating a print sequence.

```
          (RED)
            ↓
          PTØ
          PRE
PRT1      YS11
          BRN     PRT1
          RS11
          CCS
          TCS
          PLS
          YP13
          BRN     PRT1
PRT2      YS11
          BRN     PRT2
          RS11
          ADV
            ↓
```

The following is sample paper advance sequence:

```
          PRE
PRT2      YS11
          BRN     PRT2
          ADV
            ↓
```

CCS:	1111110000	A11
TCS:	1101110000	A11
PRE:	0101110000	A11
ADV:	0011110000	A11
RED:	0001110000	A11

The output format for driving the printer is such that during the printer enabled period a logic zero (low voltage) on C1 through C18 means that the column solenoid under consideration should be energized.

The outputs from C19 and C20 control the printer modes of operation.

C19	C20	Mode
Low	Low	Printer Standby
Low	High	Energize Ribbon Solenoid
High	Low	Energize Paper Solenoid
High	High	Enable Printing Solenoids

THE DATA READY COMMANDS:

In order to utilize the I/O circuit in the outputting of data, some form of a "data ready" signal is required. The I/O circuit has a combination "mode control" and "data ready" system for determining the required peripheral or function needing data.

There is a family of commands called the TIGER commands which are directly executable in either IS1 or IS2.

The general TIGER instruction is given by:

TIGER x x x 0100000 A11

where the three don't care bits are loaded directly on the output lines IOC1, IOC2 and IOC3. In this way it is possible to initiate eight distinct operations by running these inputs into a three-to-eight decoder. Since this family of commands is independent of the instruction set, if EIS1 is considered as a decoder input, a 1 of 16 decoder can by used. This means that the same TIGER bit pattern would have a different meaning, depending upon whether it was executed in IS1 or IS2.

The output of the decoder could very likely show spurious outputs while the outputs IOC1, IOC2 and IOC3 are changing. Therefore the output SCE is a strobe to be used for enabling the decoder. The outputs IOC1, IOC2 and IOC3 change to their new states between bit time 1 and bit time 2. Following a TIGER instruction SCE will give an output pulse from bit time 3 until time 48 (inclusive). In this way, the data on the three IOC lines can be settled by the initiation of the SCE pulse.

THE INPUT FLAG:

The FLG' input is the input flag to the I/O circuit. A flag signal received at the FLG' input is transmitted through this circuit to the C & T by means of the FLG output. The reason for using this input is that there is a great deal of special timing required upon entering the C & T in order to guarantee that the flag (status bit 11) is set at least once, but not more than once.

The FLG' input need not be synchronous with the system clocks; but it must last at least three clock periods in duration. (the FLG input is sampled only once every third bit time). It is the trailing edge of the FLG' signal that initiates the flag signal. As long as FLG' is held low all output flags are inhibited, even those generated internally.

The FLG' input has no internal pull-up resistor.

THE OUTPUT FLAG:

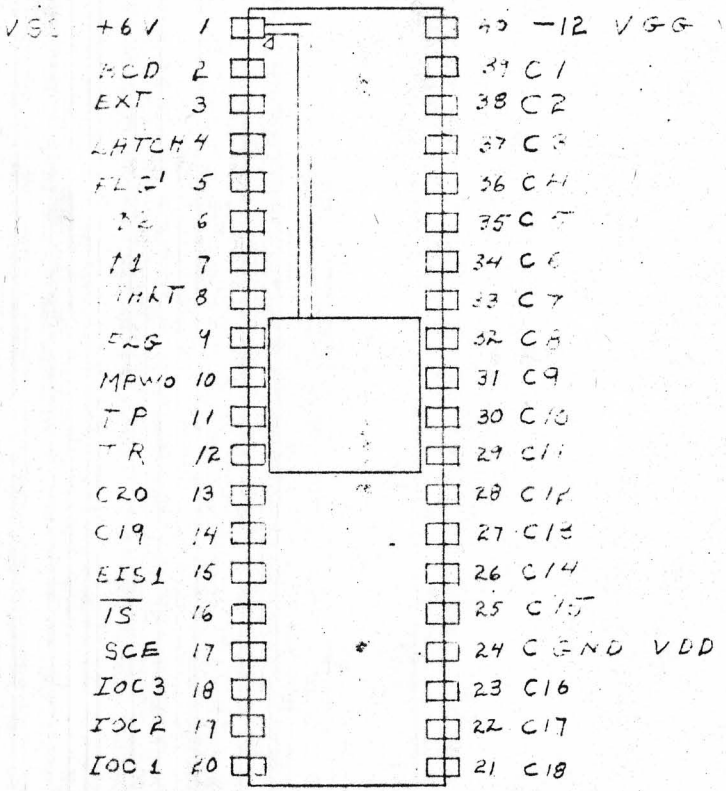
The output FLG of the I/O circuit ties directly to the FLG input of the C & T circuit. This device has an additional purpose when it is "WIRE-OR'ed" to the FLG input of the C & T with the flag signals coming from a data storage circuit (s). The I/O circuit furnishes a clocked pull-down resistor which is designed to work in conjuntion with the data storage flag output. The data storage flag output lacks the pull down drive capability to handle more than approximately 30 pf.

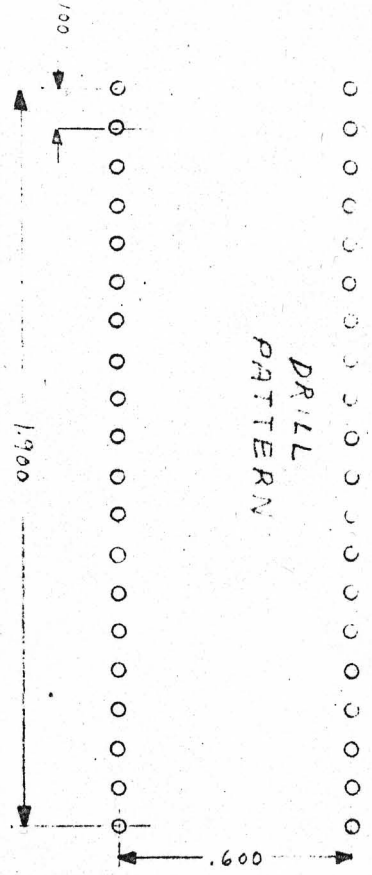
ENGINEERING RESPONSIBILITY ☐ SEPIA ☐

0	1	2	3	4	5	6	7	8	9	10	11	12	14	15	
16	17	18	19	20	21	22			33	34	38		42	43	
		83			90			93							

SYM	REVISIONS	APPROV	DATE

A - - -





ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED.
DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY J. A. REA DATE 5-1-72

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

AUXILIARY PROCESSOR
TITLE

NEXT ASSEMBLY

FINISH SCALE 2:1

HEWLETT PACKARD

PART NUMBER 1820-0994

A - - -

MOSTEK

BINARY PROCESSOR & I/O CIRCUIT

ELECTRICAL SPECIFICATIONS

Preliminary Data

Absolute Maximum Ratings

Supply Voltage V_{DD} ..... V_{SS} -10.0V

Supply Voltage V_{GG} ..... V_{SS} -21.0V

Voltage at any input or output ..... V_{SS} +0.3V to V_{SS} -10V

Operating free-air temperature range ..... 0 ℃ to 65 ℃

Storage temperature range ..... -55 ℃ to 125 ℃

Humidity ..... 0 to 90%

	PARAMETER		MIN	MAX	UNIT	COMMENTS
Power Supply	V_{DD}	Supply Voltage	0.0	0.0	V.	
	V_{SS}	Supply Voltage	+5.6	+6.5	V.	Supply voltages do not necessarily track
	V_{GG}	Supply Voltage	-11.0	-13.0	V.	
	I_{DD}	Supply Current (V_{DD})	-	TBD	mA	
	I_{GG}	Supply Current (V_{GG})	-	TBD	mA	
	P_T	*Total Chip Power	-	200	mW	At 0 ℃ with max voltages and max frequency
External Clock Description	$V\phi(0)$	Clock "0" level	V_{SS}-.8	V_{SS}	V	See Timing Diagram Figure 1
	$V\phi(1)$	Clock "1" level	V_{GG}	V_{GG}+.7	V	
	f	Operating Frequency	50	210	KC	
	tpw	Clock Pulse Width	595		ns	See note 4
	t_D	Clock Delay Time	595		ns	
	t_{rt}	Clock Pulse Rise Time	50	150	ns	
	t_{ft}	Clock Pulse Fall Time	50	150	ns	
		*This spec is a design goal.				

Input Description	t_{IN} Time at which input data is valid (before the ϕ1 clock)	0.0		μs	See Timing Diagram Figure 1
	C_{IN} *Input Capacitance				Inputs C1 to C8 become valid 20 μs after LATCH switches to a logic "1"
	ϕ1 ϕ2				
	BCD, FLG′, LATCH, C1-C8		15	pf	
	I_{ss}, PWO, START, T_R, T_P		10	pf	
			5	pf	
	MOS LEVEL INPUTS (No V_{ss} Resistor)				
	Applies to: PWO, START, BCD				Inputs FLG′ and LATCH are assumed to be asynchronous. See Note 3
	$V_{IN}(0)$ Input Voltage - Logic "0"	V_{ss}-1.0	V_{ss}+.3	V.	
	$V_{IN}(1)$ Input Voltage - Logic "1"	-	V_{ss}-4.0	V.	
	TTL LEVEL INPUTS (No V_{ss} Resistor)				
	Applies to: I_{ss}, FLG′, LATCH				The FLG′ and LATCH inputs are sampled every 3rd bit
	$V_{IN}(0)$ Input Voltage - Logic "0"	V_{ss}-1.5	V_{ss}+.3	V.	
	$V_{IN}(1)$ Input Voltage - Logic "1"	-	V_{DD}+.8	V.	
	TTL LEVEL INPUTS (With V_{ss} Resistor)				
	Applies to: $\overline{TR}$, $\overline{TP}$, C1 to C8				
	$V_{IN}(0)$ Input Voltage - Logic "0"	V_{ss}-1.5	V_{ss}+.3	V.	
	$V_{IN}(1)$ Input Voltage - Logic "1"		V_{DD}+.8	V.	
	R_{IN} Resistance to V_{ss}	4.5K	60.0K	Ω	
Output Description	MOS LEVEL OUTPUTS				
	Applies to: EXT, FLG, BCD				
	$V_{OUT}(0)$ Logical "0" Output Voltage	V_{ss}-.5		V.	
	$V_{OUT}(1)$ Logical "1" Output Voltage		V_{ss}-4.5	V.	
	EXT OUTPUT				Push-Pull Buffer
	*t_{dV} Time at which output is valid		625	ns	
	C_L Capacitive load		35	pf	
	*This spec is a design goal				

	PARAMETER	MIN	MAX	UNITS	COMMENTS
FLG OUTPUT					Modified Source Follower Output
t_{dV}	Time from Bit Time 0 at which "1" level data is valid		12	µs	
C_L	Capacitive Load		400	pf	The FLG output will be held at a logic zero from Bit Time 6 to Bit Time 49.
I_{sink}	DC current load during the "1" state		.2	mA	
R_{sus}	Resistance of sustaining resistor at V_{OUT} = 1.0 volt		100K	Ω	
BCD OUTPUT					Tristate Output
t_{dV}	Time at which output is valid		3.3	µs	The BCD Buffer is forced into the tri-state during the first 1 µs of every bit time.
C_L	Capacitive Load		100	pf	
t_{TRI}	Time for buffer to switch from the active state to the tristate		100	ns	
t_{ACT}	Time for buffer to switch from the tristate into the active state		1.0	µs	
TTL OUTPUT BUFFERS					
Applies to:	C1 to C8 C9 to C20 IOC1, IOC2, IOC3 EIS1, SCE				Outputs C1 to C8 are forced into the tristate mode when LATCH = logic "1".
$V_{OUT}^{TTL}(0)$	Logical "0" output voltage	V_{DD}+2.4		V.	All other buffers listed are Push-Pull
$V_{OUT}^{TTL}(1)$	Logical "1" output voltage		V_{DD}+.3	V.	
t_{dV}	Time at which output data is valid		5.0	µs	
I_{sink}	DC current load during the "1" state	200		µA	
I_{source}	DC current load during the "0" state	20		µA	
R_S	Buffer output resistance during a "0" state output	1.5K		Ω	
C_L	Capacitive Load				
	C1 to C8		50	pf	
	All others		30	pf	

NOTES:

1. All logic levels referred to within this document are negative logic levels:

   "0" level = High Voltage

   "1" level = Low Voltage

2. All devices will be provided with static discharge protection devices. In addition, inputs PWO, START, IS, FLG', and LATCH will be protected as per the requirements of Appendix C (Static Gate Protection Requirements).

3. Inputs FLG' and LATCH will be provided with internal sync circuitry. The input will be sampled on every 3 rd bit time and gated synchronously into the chip's logic on the next bit time.

4. Clock pulse width, (t_{pw}), and clock delay time, (t_D) are assumed to be generated by digitally dividing the operating period by 8.0.

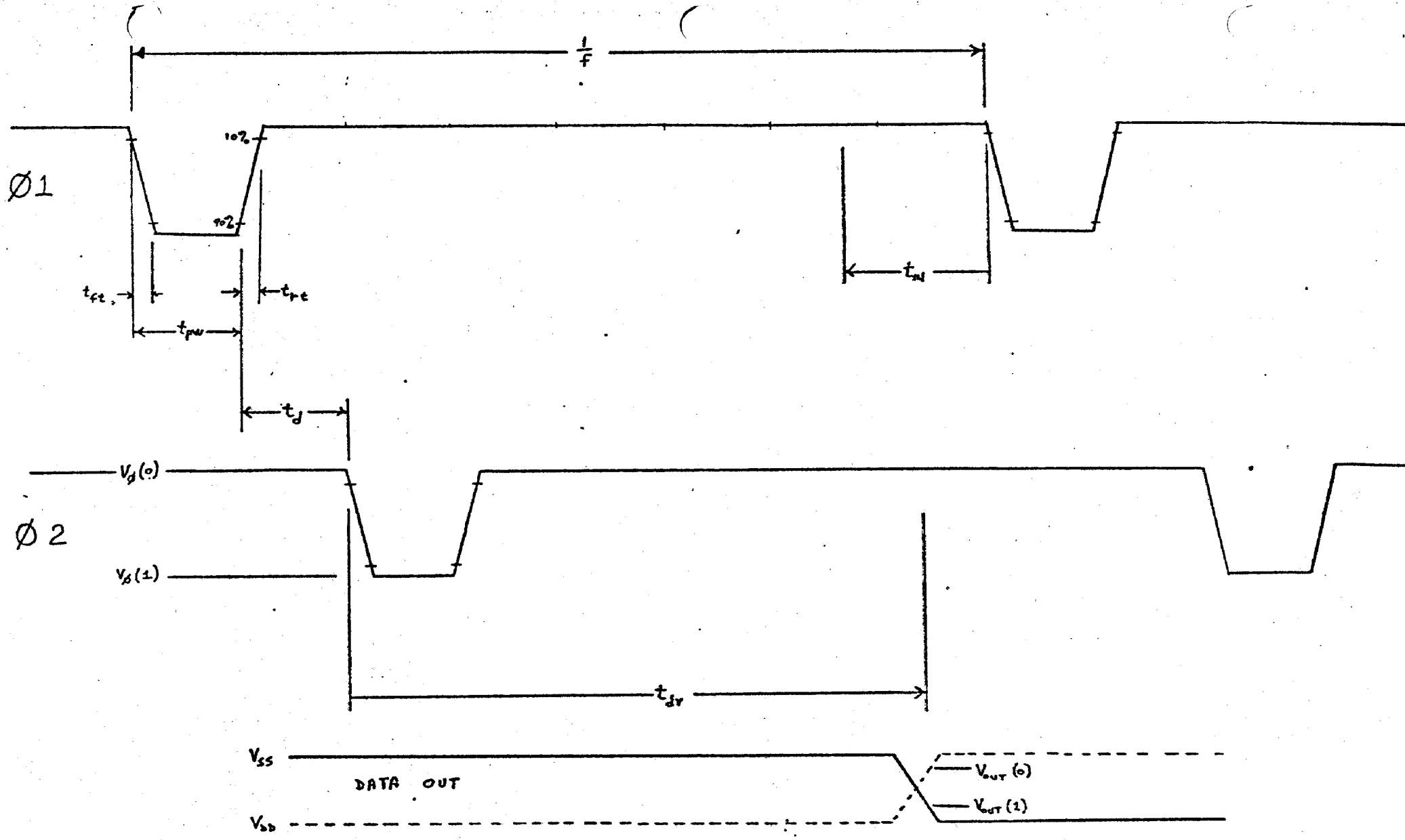


FIGURE I

TIMING DIAGRAM